SONY

ICX432DQ

Diagonal 6.67mm (Type 1/2.7) Frame Readout CCD Image Sensor with a Square Pixel for Color Cameras

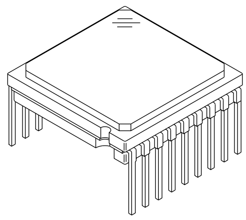
Description

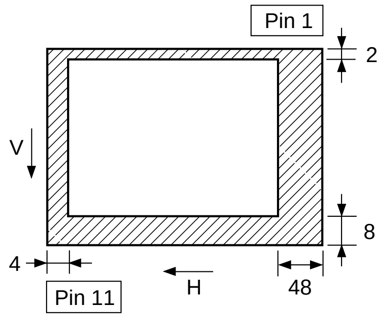
The ICX432DQ is a diagonal 6.67mm (Type 1/2.7) interline CCD solid-state image sensor with a square pixel array and 3.24M effective pixels. Adoption of a 3-field readout system ensures small size and high performance. This chip features an electronic shutter with variable charge-storage time.

R, G, B primary color mosaic filters are used as the color filters, and at the same time high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

This chip is suitable for applications such as electronic still cameras, etc.

18 pin DIP (Plastic)





Optical black position
(Top View)

Features

- Supports frame readout system
- High horizontal and vertical resolution
- Supports high frame rate readout mode : 30 frames/s,
  AF mode : 60 frames/s, 50 frames/s
- Square pixel
- Horizontal drive frequency: 24.3MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- R, G, B primary color mosaic filters on chip
- High sensitivity, low dark current
- Continuous variable-speed shutter
- Excellent anti-blooming characteristics
- 18-pin high-precision plastic package

Device Structure

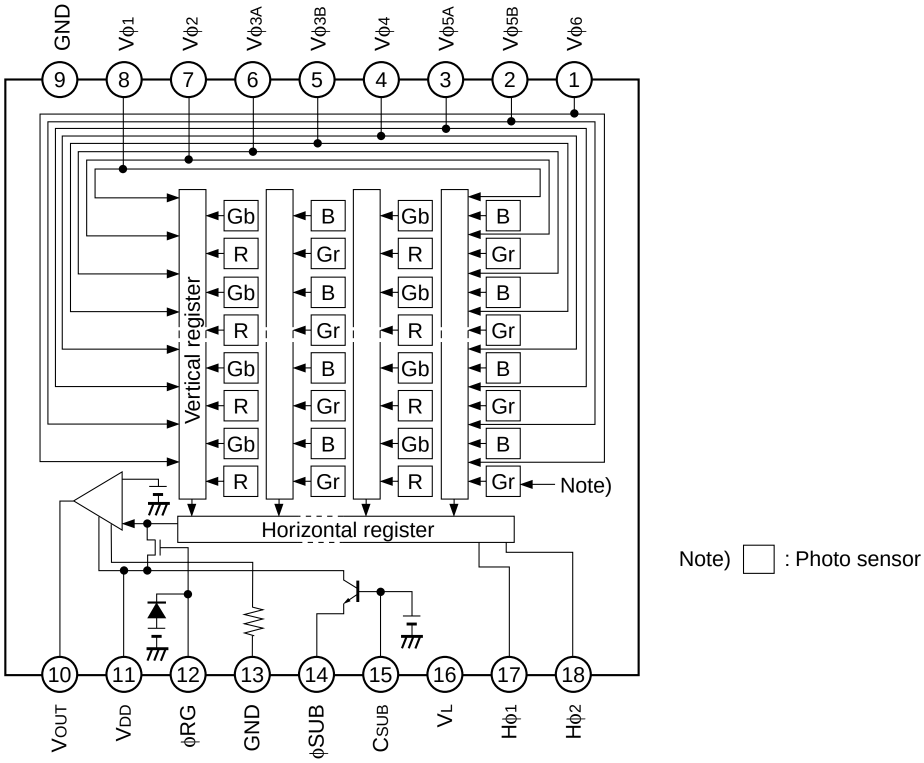
- Interline CCD image sensor
- Total number of pixels: 2140 (H) × 1560 (V) approx. 3.34M pixels
- Number of effective pixels: 2088 (H) × 1550 (V) approx. 3.24M pixels
- Number of active pixels: 2080 (H) × 1542 (V) approx. 3.21M pixels diagonal 6.667mm
- Number of recommended recording pixels:
  2048 (H) × 1536 (V) approx. 3.15M pixels diagonal 6.592mm aspect ratio 4:3
- Chip size: 6.10mm (H) × 4.95mm (V)
- Unit cell size: 2.575μm (H) × 2.575μm (V)
- Optical black: Horizontal (H) direction: Front 4 pixels, rear 48 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 28
  Vertical 1 (3rd field only)
- Substrate material: Silicon

Super **HAD CCD** TM

* Super HAD CCD is a trademark of Sony Corporation. The Super HAD CCD is a version of Sony's high performance CCD HAD (Hole-Accumulation Diode) sensor with sharply improved sensitivity by the incorporation of a new semiconductor technology developed by Sony Corporation.

Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi_{6}$	Vertical register transfer clock	10	V_{OUT}	Signal output
2	$V\phi_{5B}$	Vertical register transfer clock	11	V_{DD}	Supply voltage
3	$V\phi_{5A}$	Vertical register transfer clock	12	φRG	Reset gate clock
4	$V\phi_{4}$	Vertical register transfer clock	13	GND	GND
5	$V\phi_{3B}$	Vertical register transfer clock	14	φSUB	Substrate clock
6	$V\phi_{3A}$	Vertical register transfer clock	15	C_{SUB}	Substrate bias *1
7	$V\phi_{2}$	Vertical register transfer clock	16	V_{L}	Protective transistor bias
8	$V\phi_{1}$	Vertical register transfer clock	17	$H\phi_{1}$	Horizontal register transfer clock
9	GND	GND	18	$H\phi_{2}$	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against ϕSUB	V_{DD}, V_{OUT}, ϕRG – ϕSUB	–40 to +12	V	
	$V\phi_1$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{5A}$, $V\phi_{5B}$ – ϕSUB	–50 to +15	V	
	$V\phi_2$, $V\phi_4$, $V\phi_6$, V_L – ϕSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – ϕSUB	–40 to +0.3	V	
	C_{SUB} – ϕSUB	–25 to	V	
Against ϕGND	V_{DD}, V_{OUT}, ϕRG, C_{SUB} – GND	–0.3 to +22	V	
	$V\phi_1$, $V\phi_2$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_4$, $V\phi_{5A}$, $V\phi_{5B}$, $V\phi_6$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +6.5	V	
Against ϕV_L	$V\phi_1$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_{5A}$, $V\phi_{5B}$ – V_L	–0.3 to +28	V	
	$V\phi_2$, $V\phi_4$, $V\phi_6$, $H\phi_1$, $H\phi_2$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–6.5 to +6.5	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_6$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24V (Max.) when clock width < 10μs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	ϕSUB	*2				
Reset gate clock	ϕRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

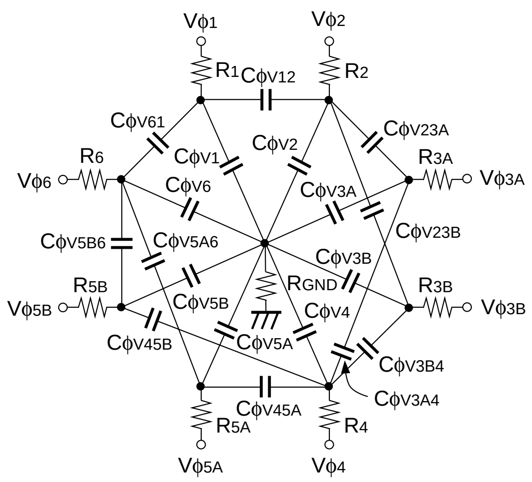
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}	5.0	7.0	9.0	mA	

Clock Voltage Conditions

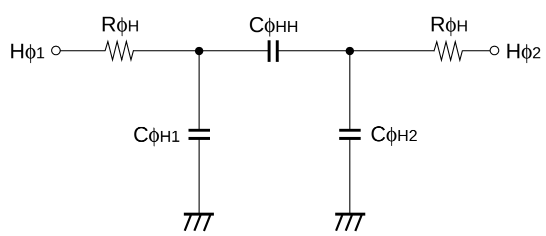
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2} V_{VH3}, V_{VH4}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2} + V_{VH3} + V_{VH4})/2$
	V_{VH5}, V_{VH6}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}, V_{VL5}, V_{VL6}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL5} + V_{VL6})/2$
	$V_{\phi V}$	6.8	7.5	8.05	V	2	$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 6)
	$V_{VH5} - V_{VH}$	–0.25		0.1	V	2	
	$V_{VH6} - V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.8	V	2	High-level coupling
	V_{VHL}			0.9	V	2	High-level coupling
	V_{VLH}			0.9	V	2	Low-level coupling
	V_{VLL}			0.8	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	3.0	3.3	3.6	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.5	1.65		V	3	Cross-point voltage
Reset gate clock voltage	$V_{\phi RG}$	3.0	3.3	3.6	V	4	
	$V_{RGLH} - V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	21.5	22.5	23.5	V	5	

Clock Equivalent Circuit Constants

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$		1280		pF	
	$C\phi_{V3A}$, $C\phi_{V3B}$, $C\phi_{V5A}$, $C\phi_{V5B}$		640		pF	
	$C\phi_{V2}$, $C\phi_{V4}$, $C\phi_{V6}$		400		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$		510		pF	
	$C\phi_{V23A}$, $C\phi_{V23B}$, $C\phi_{V45A}$, $C\phi_{V45B}$		50		pF	
	$C\phi_{V3A4}$, $C\phi_{V3B4}$, $C\phi_{V5A6}$, $C\phi_{V5B6}$		260		pF	
	$C\phi_{V61}$		100		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		40		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		70		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		8		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		1000		pF	
Vertical transfer clock series resistor	R_1, R_2, R_4, R_6		60		Ω	
	R_{3A}, R_{5A}		240		Ω	
	R_{3B}, R_{5B}		80		Ω	
Vertical transfer clock ground resistor	R_{GND}		18		Ω	
Horizontal transfer clock series resistor	$R\phi_H$		13		Ω	



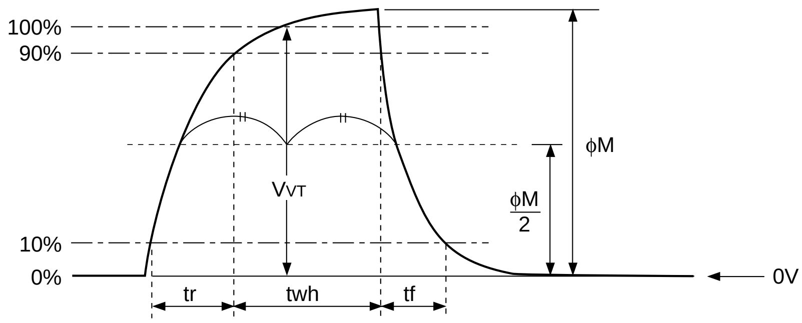
Vertical transfer clock equivalent circuit



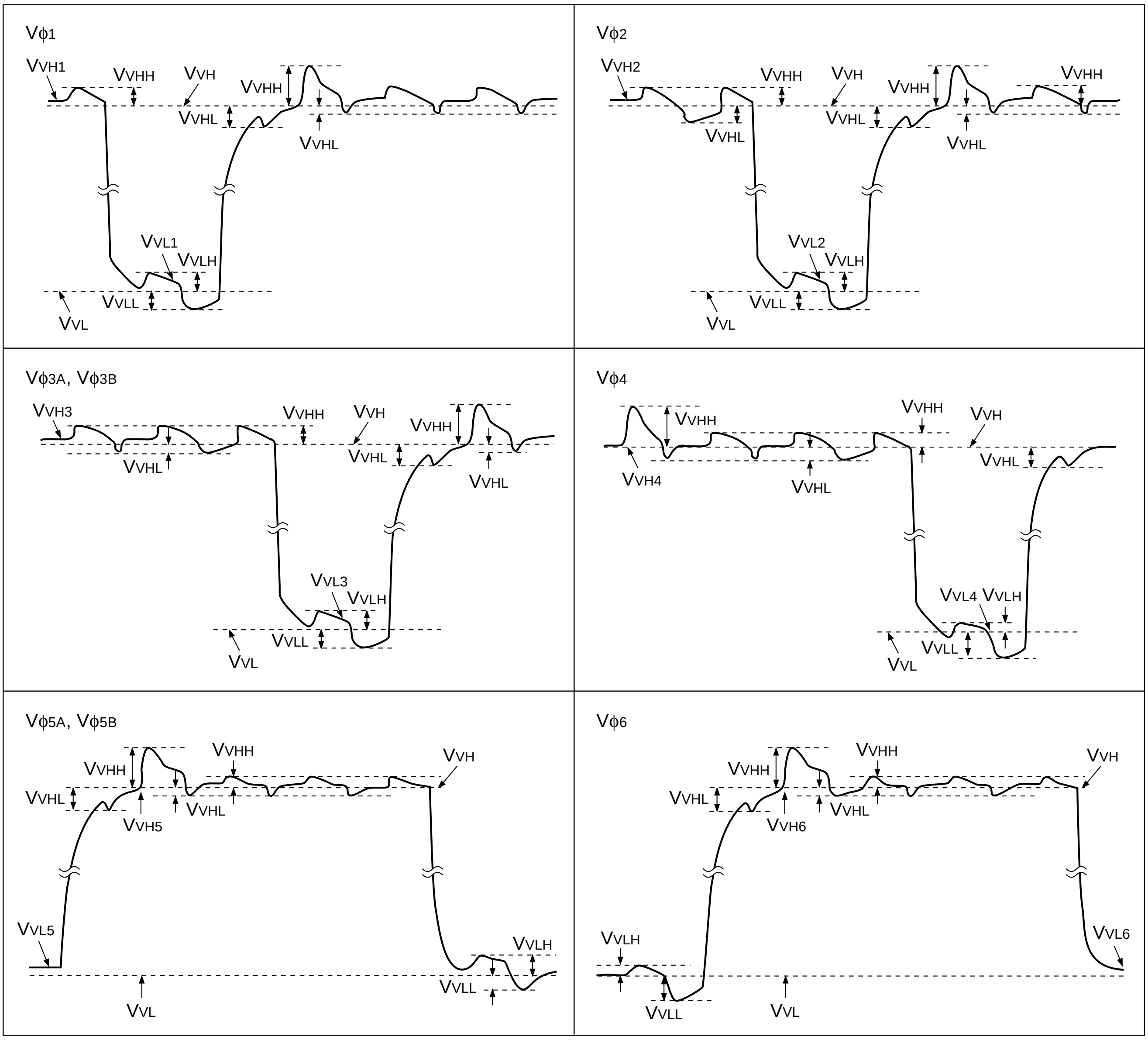
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

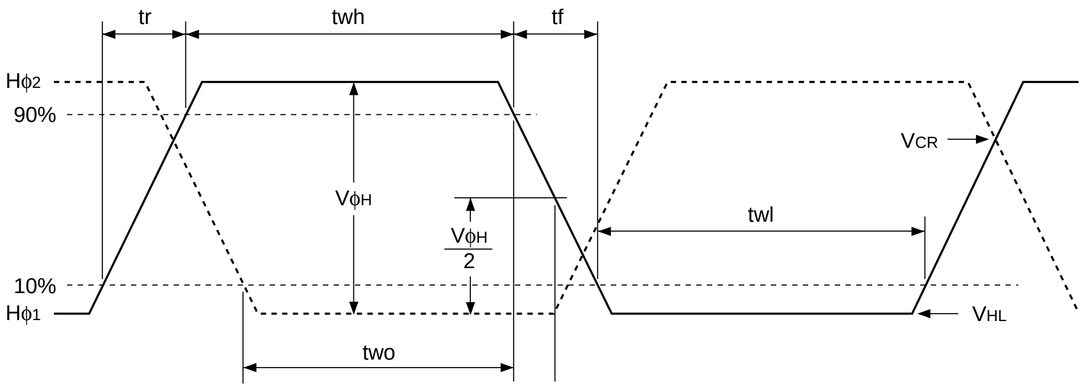


$V_{VH} = (V_{VH1} + V_{VH2} + V_{VH3} + V_{VH4})/4$

$V_{VL} = (V_{VL5} + V_{VL6})/2$

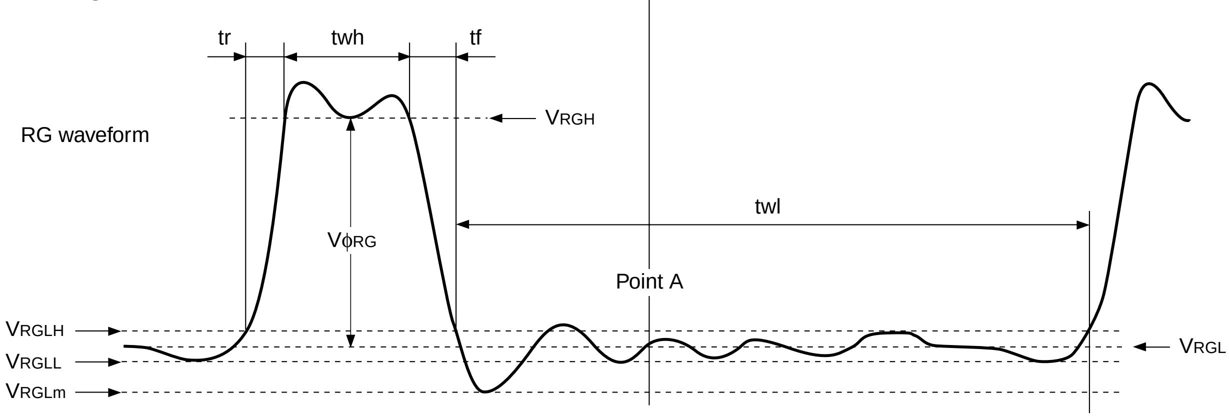
$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 6)

(3) Horizontal transfer clock waveform



Cross-point voltage for the $H\phi_1$ rising side of the horizontal transfer clocks $H\phi_1$ and $H\phi_2$ waveforms is V_{CR}.
The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

(4) Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

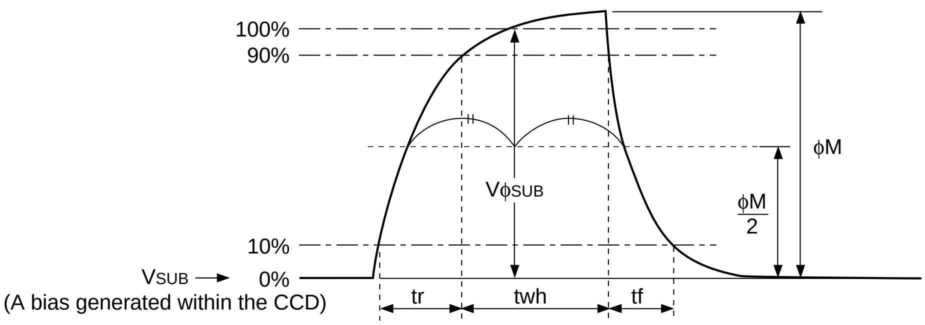
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval with twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is V_{RGLm}.

(5) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 24.3MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.63	2.83						0.5			0.5		µs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_4$, $V\phi_{5A}$, $V\phi_{5B}$, $V\phi_6$										15		350	ns	When using CXD3400N
Horizontal transfer clock	$H\phi_1$	11	15		11	15			6.0	9.5		6.0	9.5	ns	tf ≥ tr – 2ns
	$H\phi_2$	11	15		11	15			6.0	9.5		6.0	9.5		
Reset gate clock	ϕRG	6	8			28			3			3		ns	
Substrate clock	ϕSUB	2.5	3.02							0.5			0.5	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	10	15		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

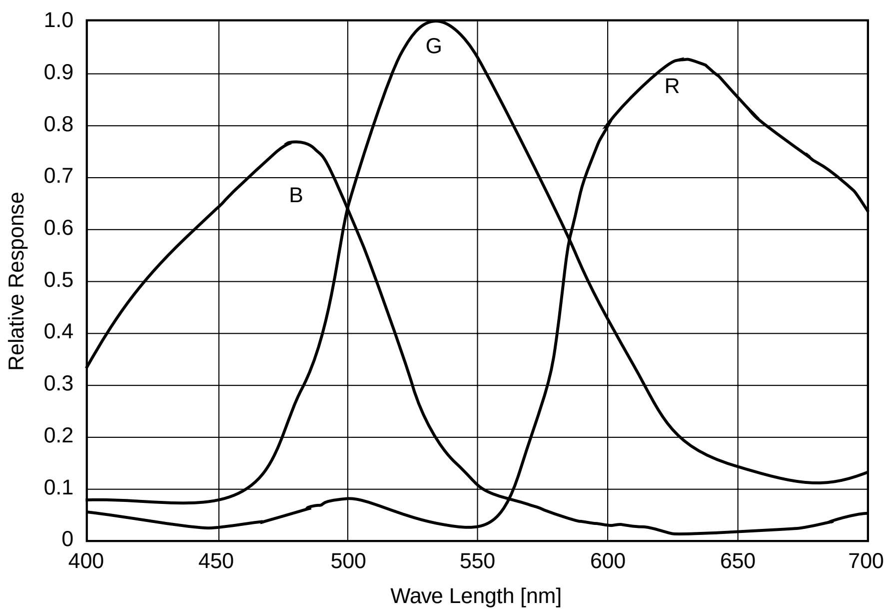


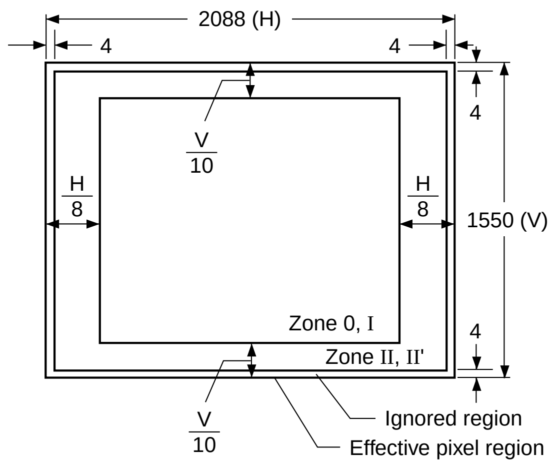
Image Sensor Characteristics (horizontal drive frequency: 24.3MHz) (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G Sensitivity	Sg	165	220	275	mV	1	1/30s accumulation
Sensitivity comparison	Rr	0.46		0.72		1	
	Rb	0.33		0.59		1	
Saturation signal	Vsat	420			mV	2	Ta = 60°C
Smear	Sm		–87.5	–80	dB	3	Frame readout mode*1
			–78	–70.5			High frame rate readout mode
Video signal shading	SHg			20	%	4	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			10	mV	5	Ta = 60°C, 5.0 frame/s
Dark signal shading	ΔVdt			8	mV	6	Ta = 60°C, 5.0 frame/s, *2
Line crawl G	Lcg			3.8	%	7	
Line crawl R	Lcr			3.8	%	7	
Line crawl B	Lcb			3.8	%	7	
Lag	Lag			0.5	%	8	

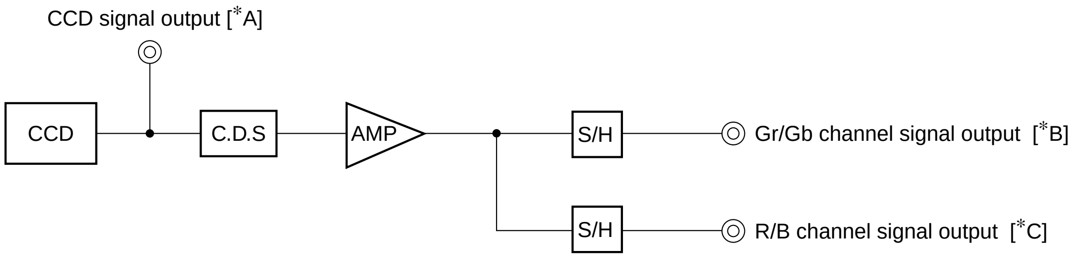
*1 After closing the mechanical shutter, the smear can be reduced to below the detection limit by performing vertical register sweep operation.

*2 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

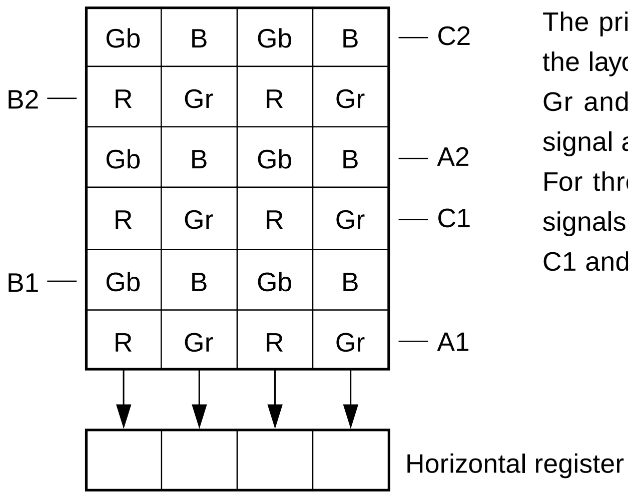
Image Sensor Characteristics Measurement Method

◎ Measurement conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the frame readout mode is used. In addition, V_{SUB} Cont. is turned off.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

◎ Color coding of this image sensor & Readout



Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.
For three frames readout, the A1 and A2 lines are output as signals in the A field, the B1 and B2 lines in the B field, and the C1 and C2 lines in the C field.

◎ Readout modes

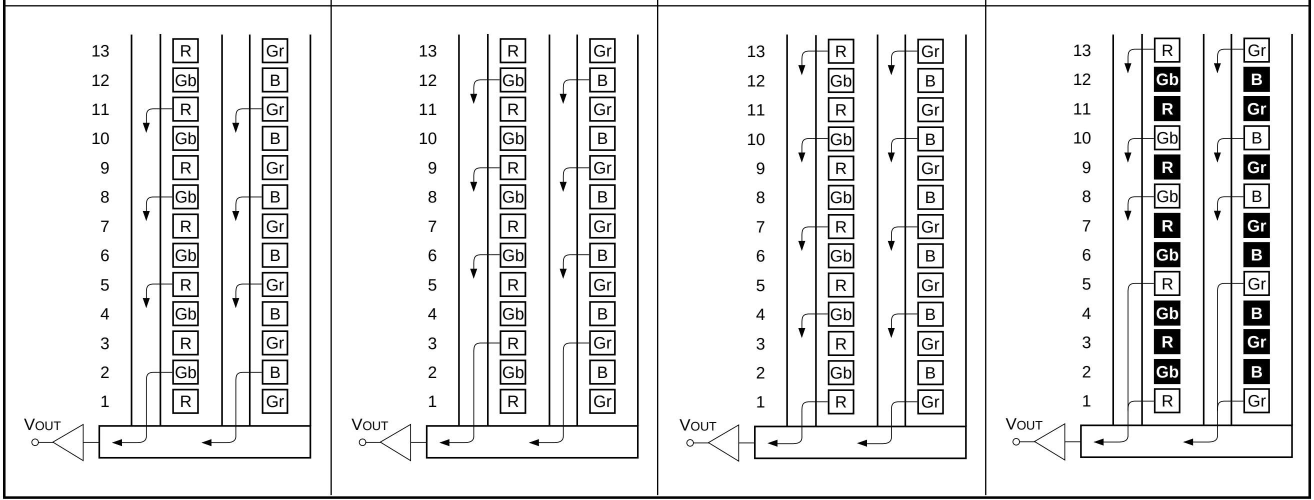
1. Readout modes list

The following readout modes are possible by driving the image sensor at the timing specifications noted in this Data Sheet.

Mode name		Frame rate	Number of effective output lines
Frame readout mode	NTSC mode	5.0 frame/s	1550 (1st 517, 2nd 516, 3nd 517)
	PAL mode	5.0 frame/s	1550 (1st 517, 2nd 516, 3nd 517)
High frame rate readout mode	NTSC mode	30 frame/s	258
	PAL mode	25 frame/s	258
AF mode	NTSC mode	60 frame/s	96
	PAL mode	50 frame/s	123

2. Frame readout mode, high frame rate readout mode

Frame readout mode			High frame rate readout mode
1st field	2nd field	3rd field	



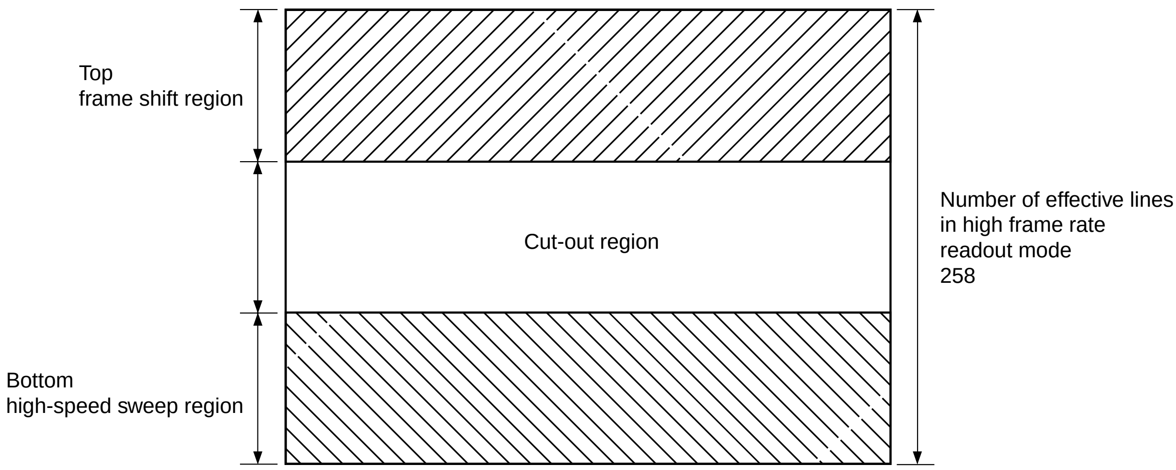
Note) Blacked out portions in the diagram indicate pixels which are not read out.

1. Frame readout mode
   In this mode, all pixel signals are divided into three fields and output.
   All pixel signals are read out independently, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   Output is performed at 30 frames per second by reading out 4 pixels for every 12 vertical pixels and adding 2 pixels in the horizontal CCD.
   The number of output lines is 258 lines.
   This readout mode emphasizes processing speed over vertical resolution.

3. AF

The AF mode increases the frame rate by cutting out a portion of the picture through high-speed elimination of the top and bottom of the picture in high frame rate readout mode. This mode allows 1/60s and 1/50s output, so it is effective for raising the auto focus (AF) speed.
In addition, the output line position and number of output lines are fixed. See the timing specifications for the cut-out region.



◎ Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

(3) Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens (exit pupil distance –33mm) with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G Sensitivity, sensitivity comparison
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{GR}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$$V_G = (V_{Gr} + V_{Gb})/2$$
$$Sg = V_G \times \frac{100}{30} \text{ [mV]}$$
$$Rr = V_R/V_G$$
$$Rb = V_B/V_G$$

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV.
After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = 20 \times \log\left(Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10}\right) \text{[dB] (1/10V method conversion value)}$$

4. Video signal shading

Set to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Grmax [mV]) and minimum value (Grmin [mV]) of the Gr signal output and substitute the values into the following formula.

$$SHg = (Grmax - Grmin)/150 \times 100\ [\%]$$

5. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta Vdt = Vdmax - Vdmin\ [mV]$$

7. Line crawl

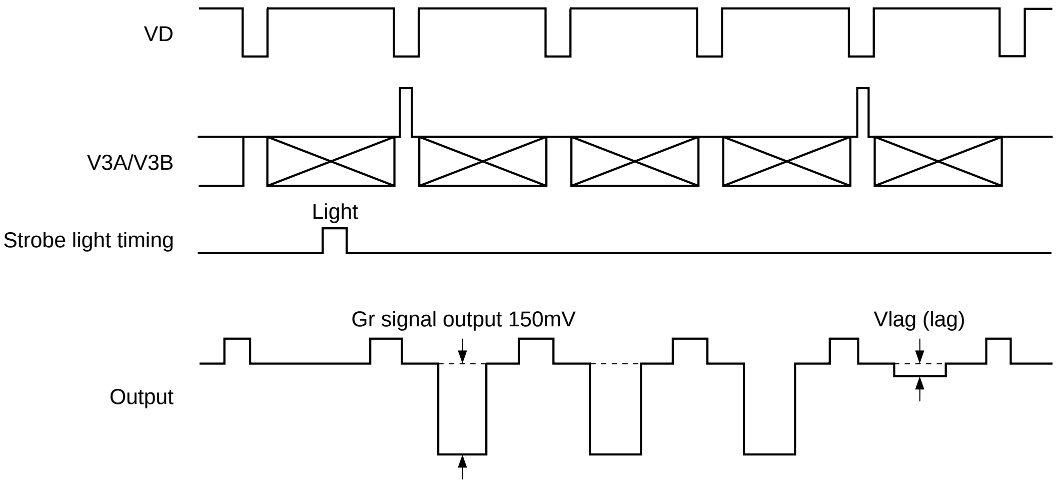
Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

$$Lci = \frac{\Delta Gli}{Gai} \times 100\ [\%]\ (i = r, g, b)$$

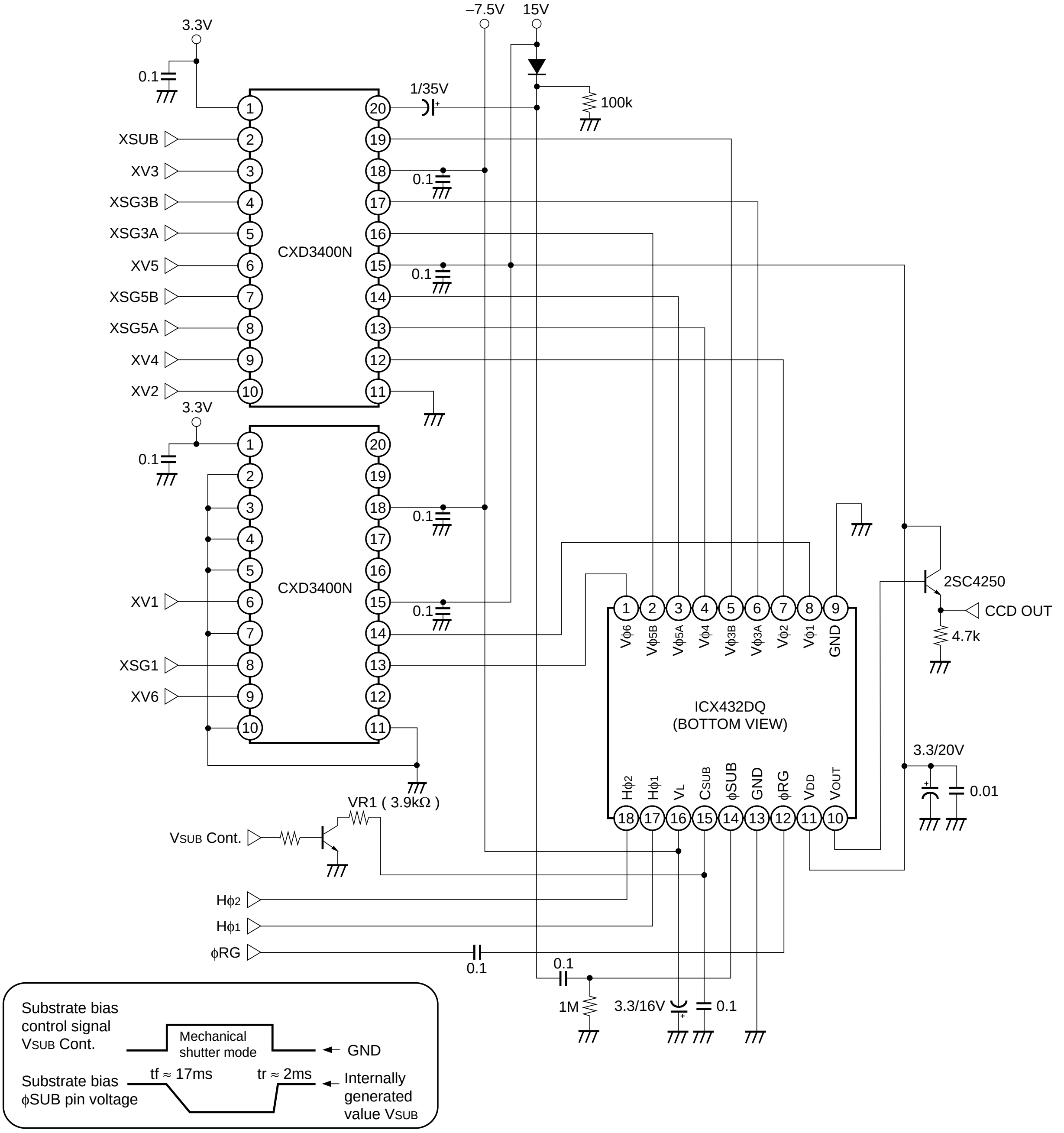
8. Lag

Adjust the Gr signal output value generated by the strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

$$Lag = (Vlag/150) \times 100\ [\%]$$



Drive Circuit



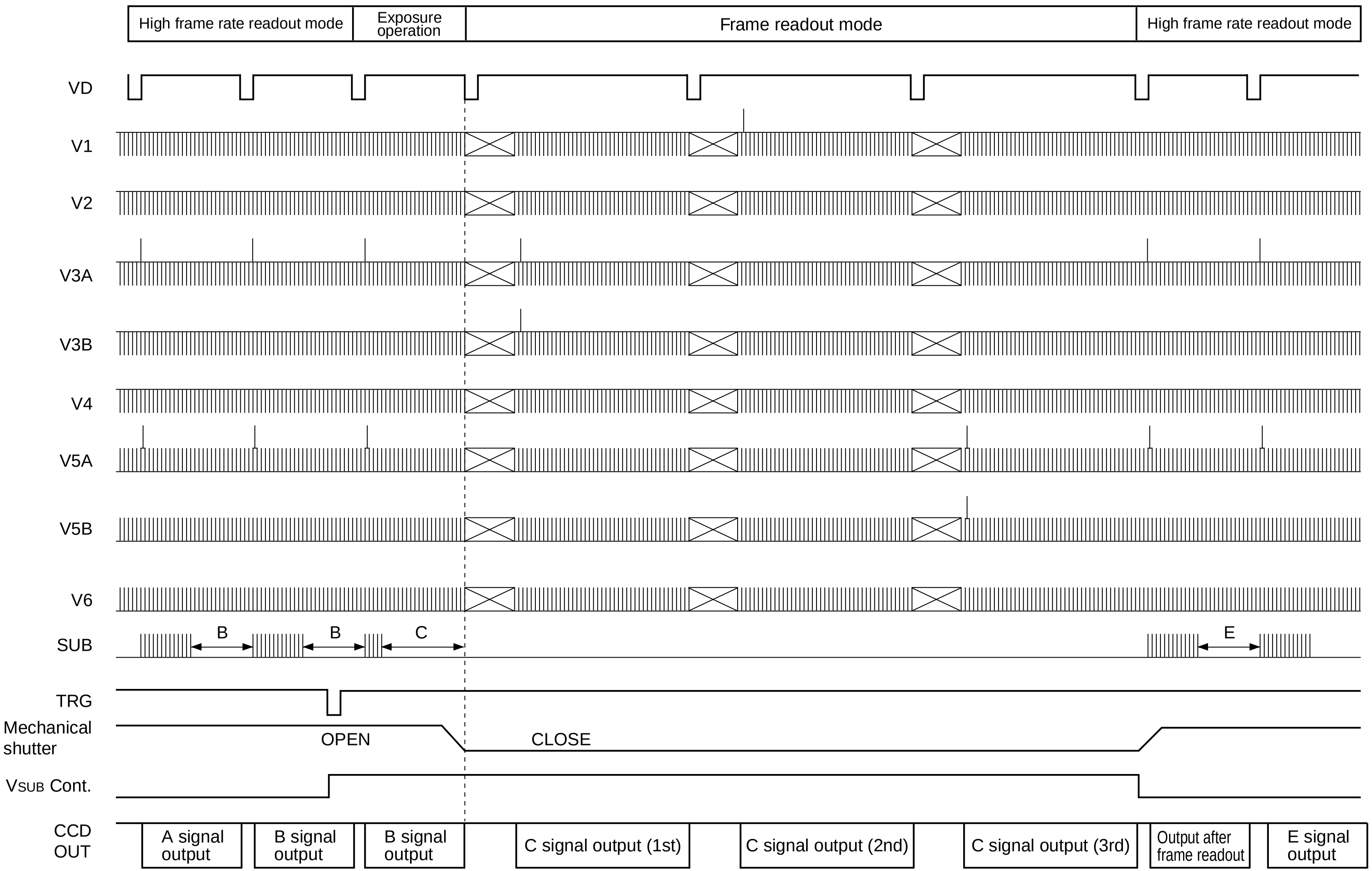
Notes) Substrate bias control

1. The saturation signal level decreases when exposure is performed using the mechanical shutter, so control the substrate bias.
2. A saturation signal level equivalent to that for continuous exposure can be assured by connecting a VR1 grounding registor to the CCD C_{SUB} pin.

Drive timing precautions

1. Blooming occurs in modes (high frame rate readout, etc.) that do not use the mechanical shutter, so do not ground the connected VR1 resistor.
2. tf is slow, so the internally generated voltage V_{SUB} may not drop to a sufficiently low level if the substrate bias control signal is not set to high level 30ms before entering the exposure period and the VR1 resistor connected to the C_{SUB} pin is not grounded.
3. The blooming signal generated during exposure in mechanical shutter mode is swept by providing two fields or more of idle transfer through vertical register high-speed sweep transfer from the time the mechanical shutter closes until sensor readout is performed. However, note that the V_L potential and the ϕSUB pin DC voltage sag at this time.

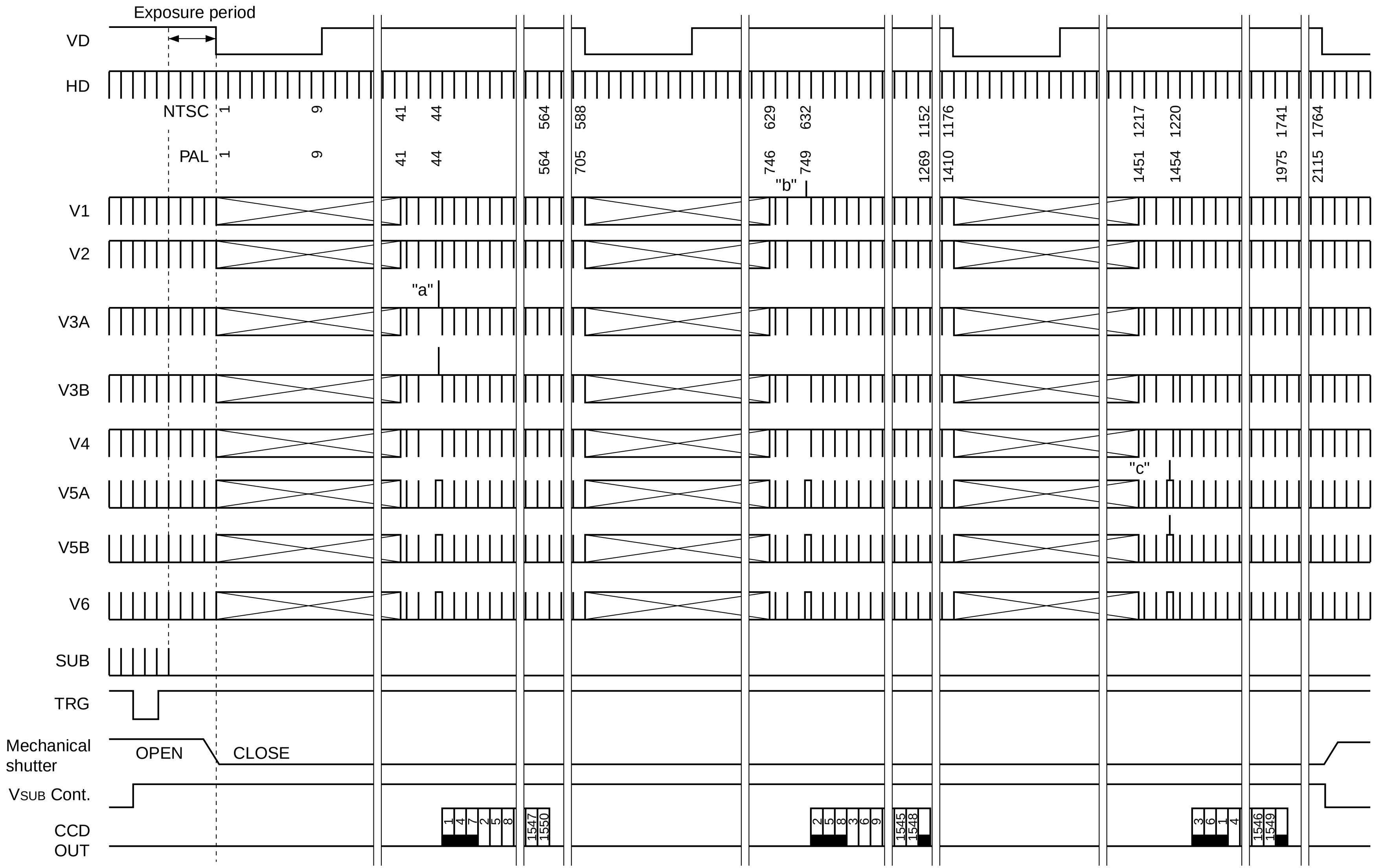
Drive Timing Chart (Vertical Sequence) High Frame Rate Readout Mode → Frame Readout Mode/Electronic Shutter Normal Operation



Note) High frame rate readout mode out signals of V_{SUB} Cont. high period contain a blooming component and should therefore not be used.
Apply 20 or more electronic shutter pulses at the start of exposure for the recording image.
If less than 20 pulses are applied, the electronic shutter may occur a discharge error.

Drive Timing Chart (Vertical Sync)

NTSC/PAL Frame Readout Mode
NTSC: 5.0 frame/s, PAL: 5.0 frame/s

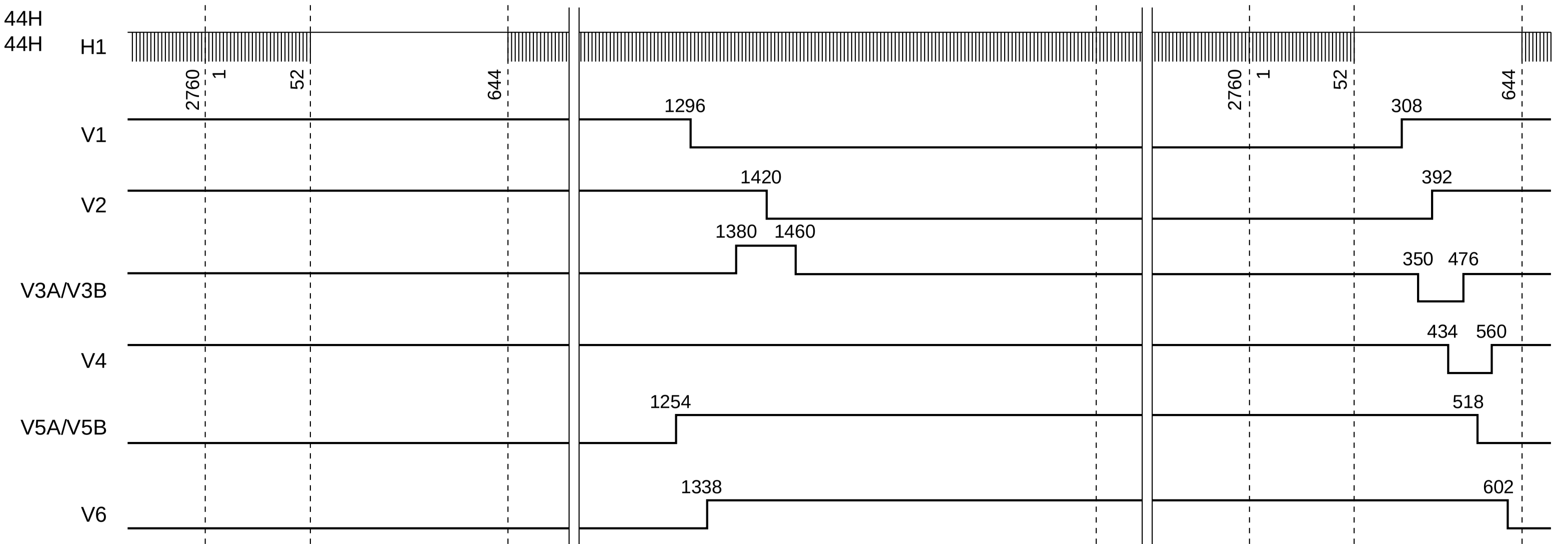


Note) 2760fH, however, 588H, 1176H and 1764H in NTSC mode are 1500clk, 705H, 1410H and 2115H in PAL mode are 960clk.

Drive Timing Chart (Readout) NTSC/PAL Frame Readout Mode

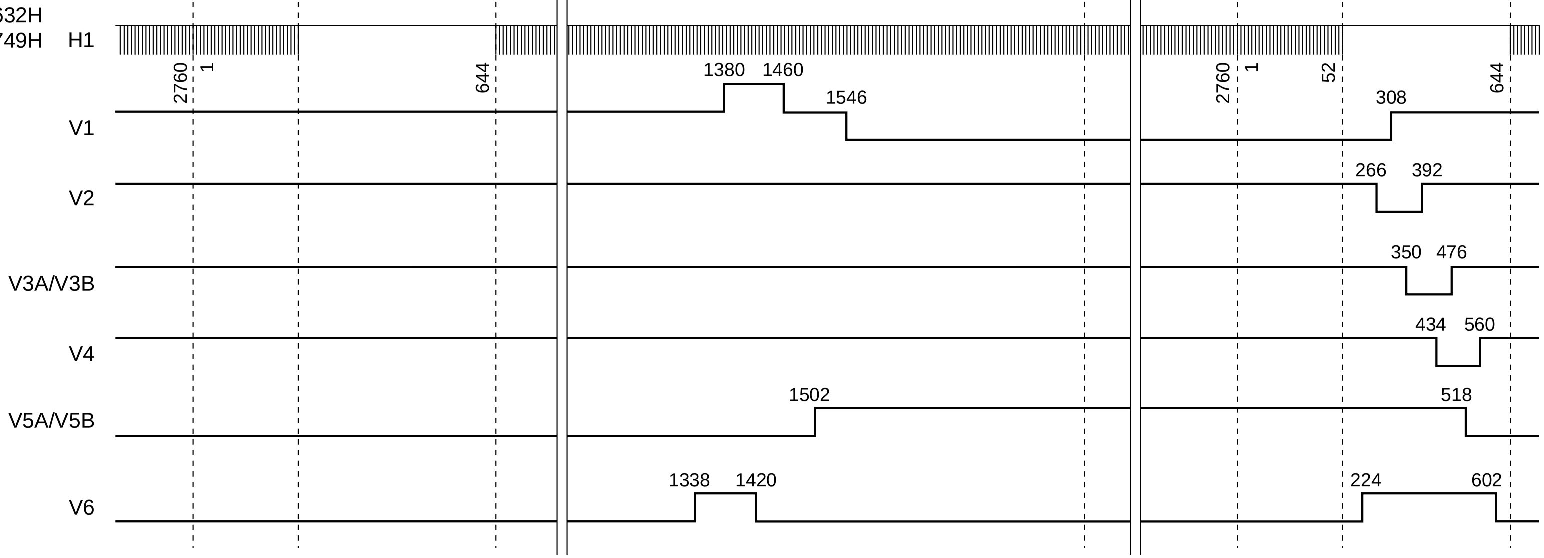
"a" Enlarged

NTSC 44H
PAL 44H



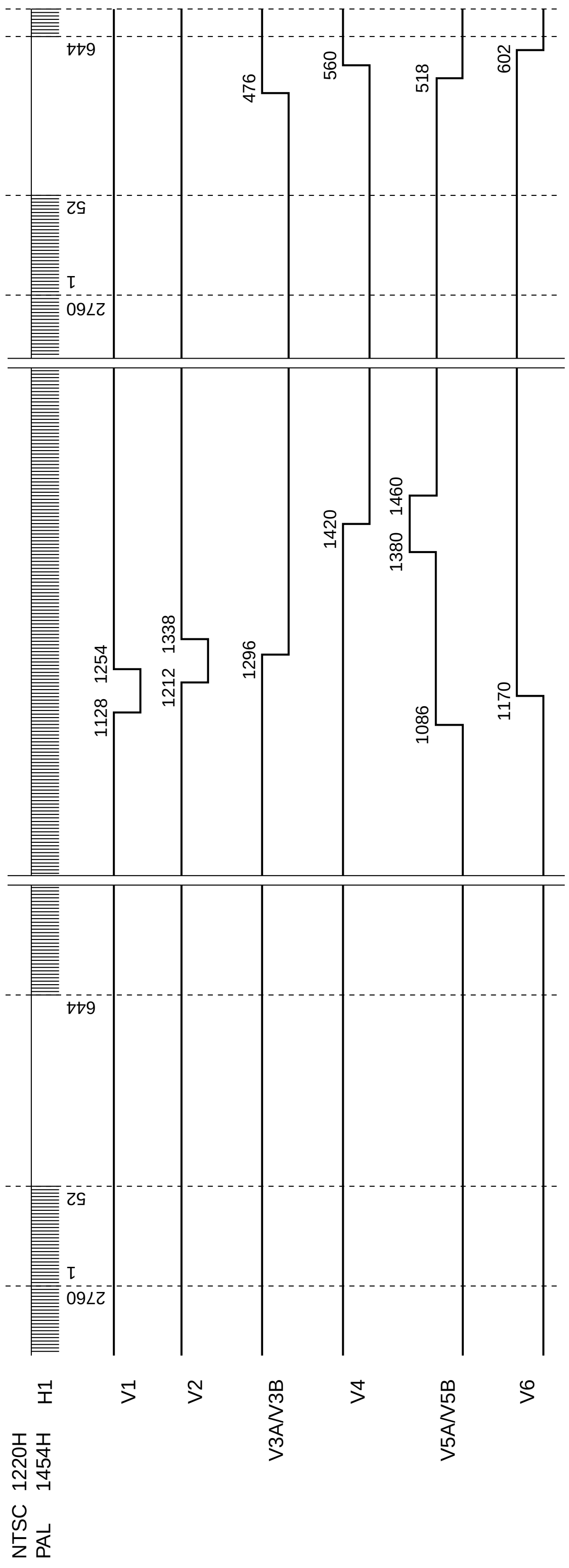
"b" Enlarged

NTSC 632H
PAL 749H

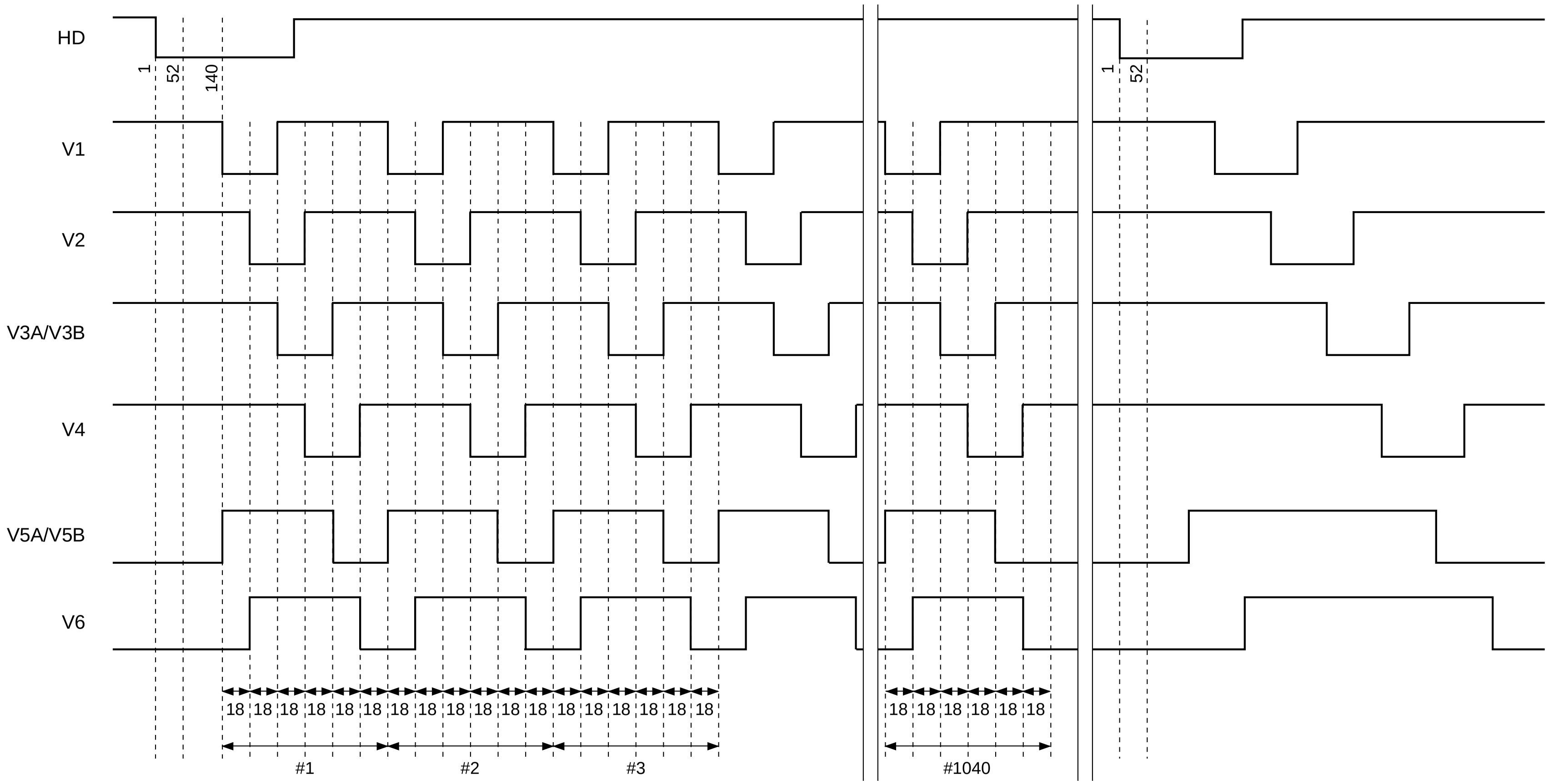


Drive Timing Chart (Readout) NTSC/PAL Frame Readout Mode

"c" Enlarged

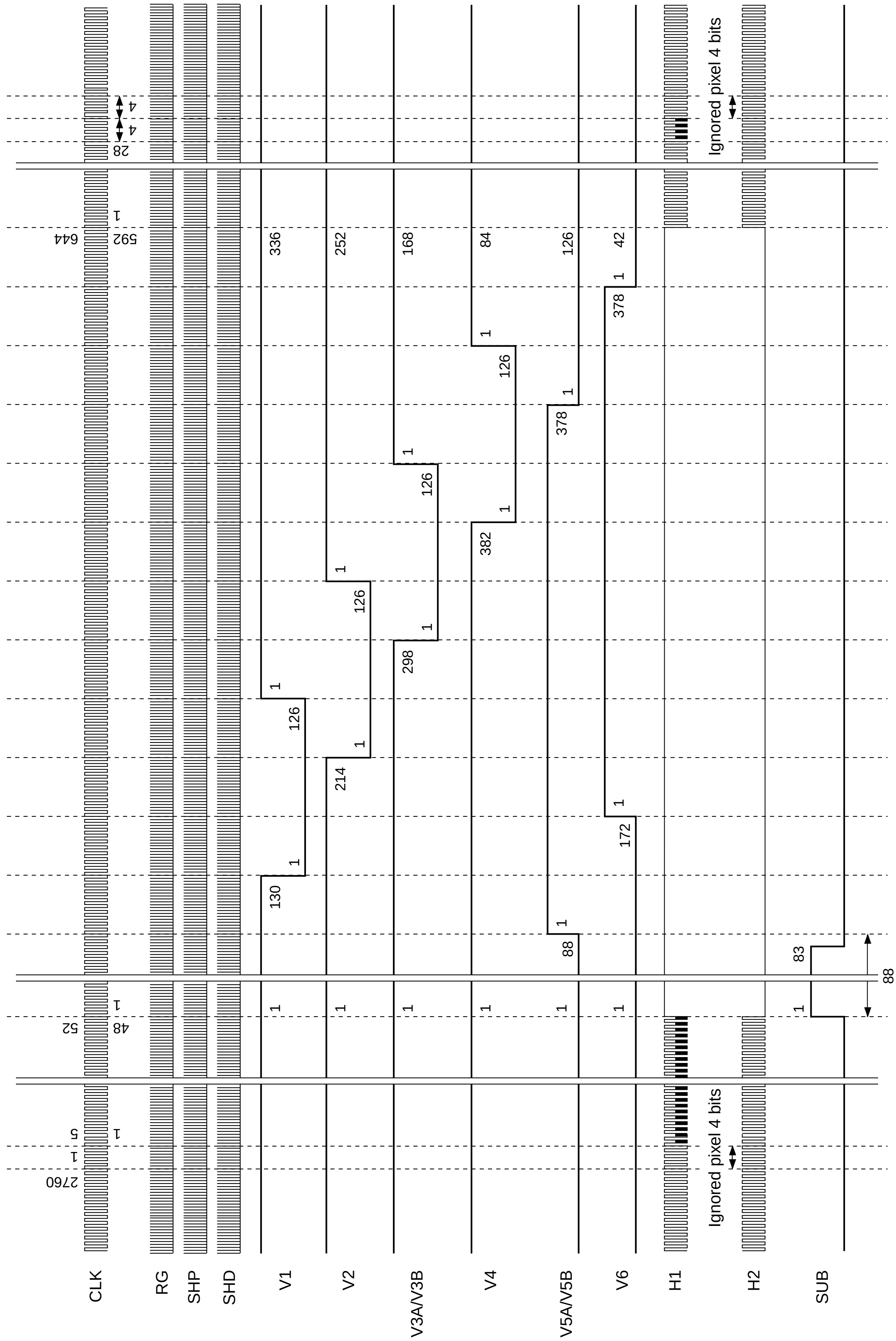


Drive Timing Chart (High-speed Sweep Operation) NTSC/PAL Frame Readout Mode



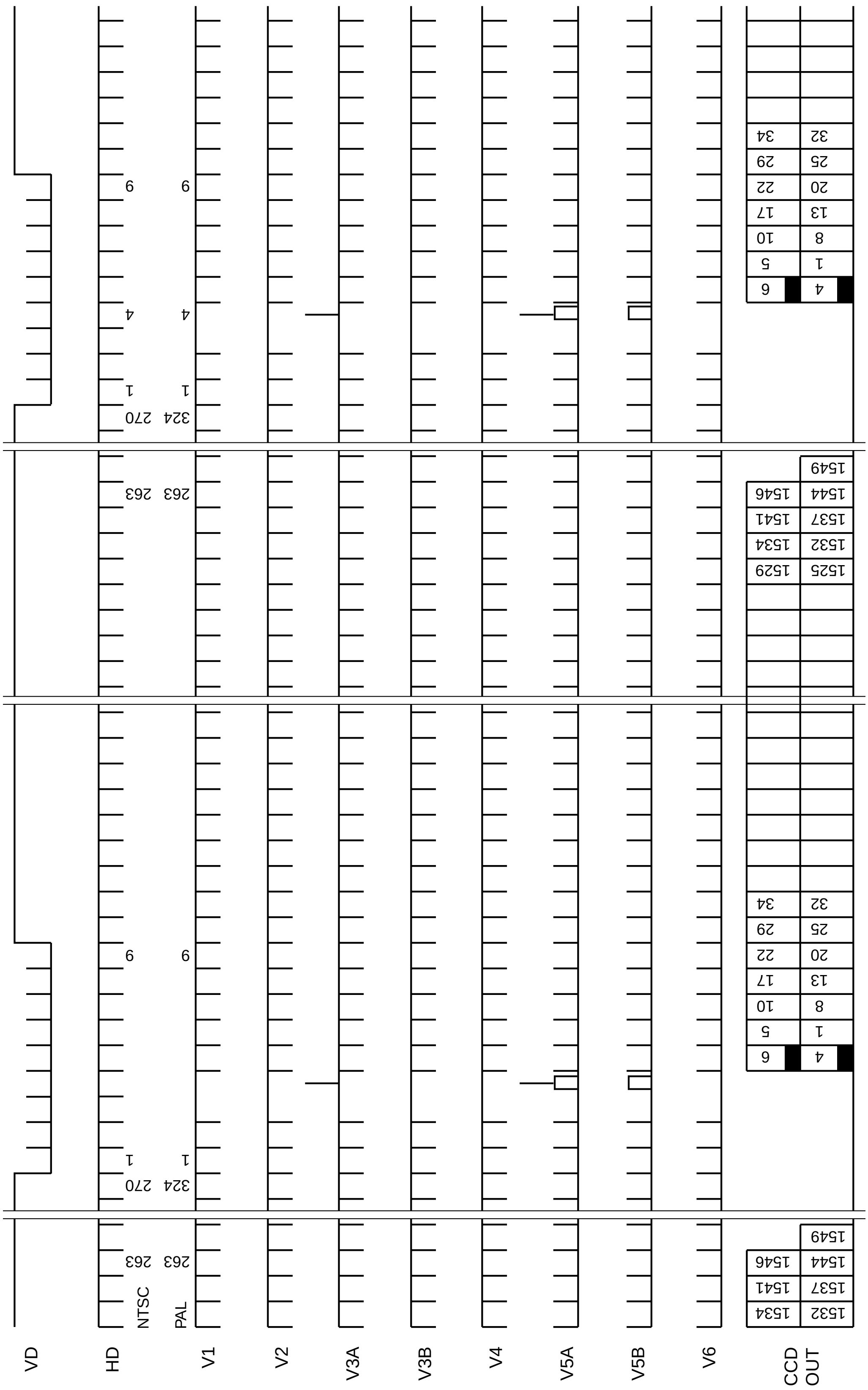
Note) In the period of high-speed sweep operation, the rising of input clocks XV1, XV2, XV3, XV4, XV5 and XV6 to vertical transfer clock driver CD3400N should be delayed by 1 clock against the above timing chart.

Drive Timing Chart (Horizontal Sync) NTSC/PAL Frame Readout Mode



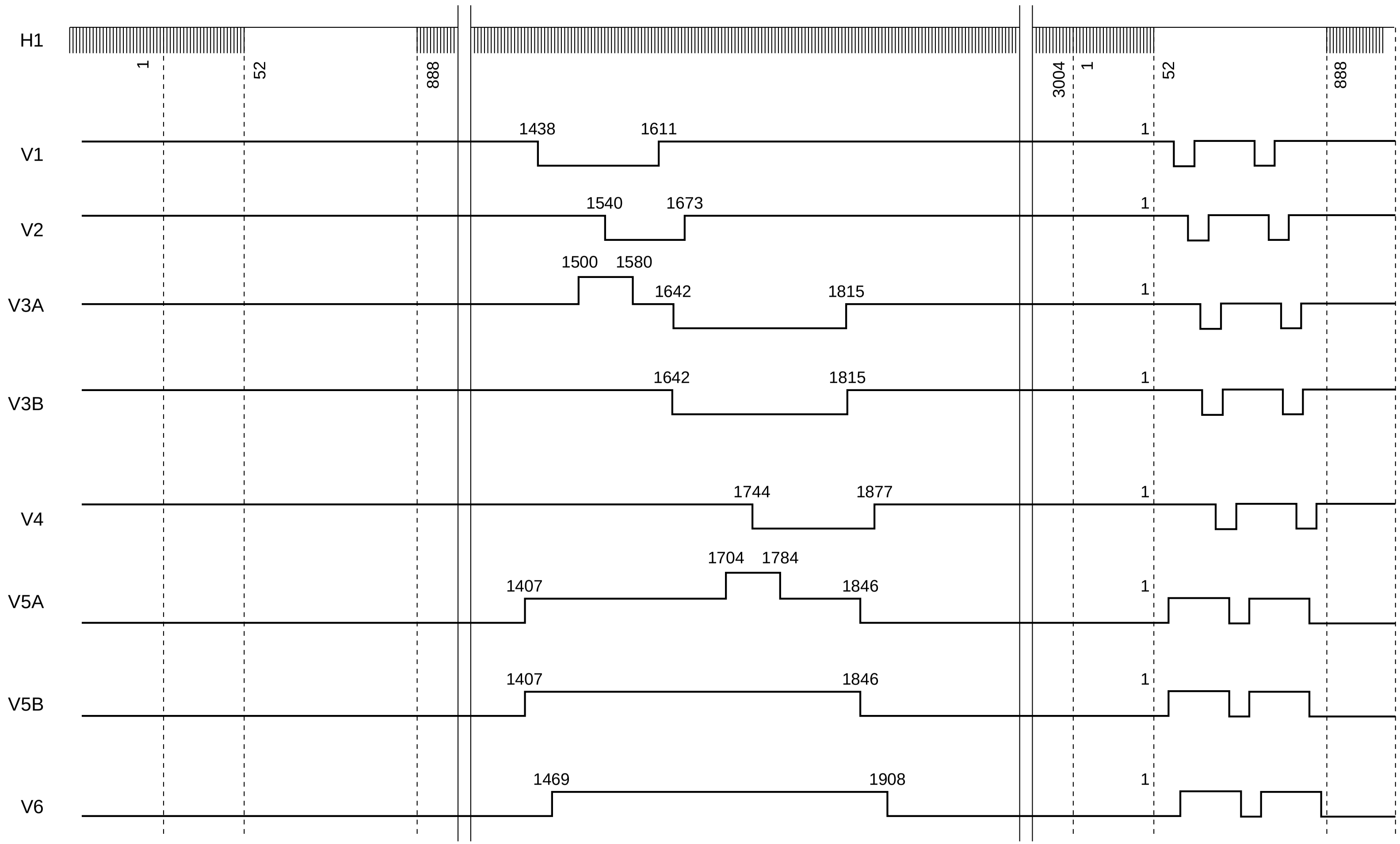
Drive Timing Chart (Vertical Sync)

NTSC/PAL High Frame Rate Readout Mode
NTSC: 30 frame/s, PAL: 25 frame/s

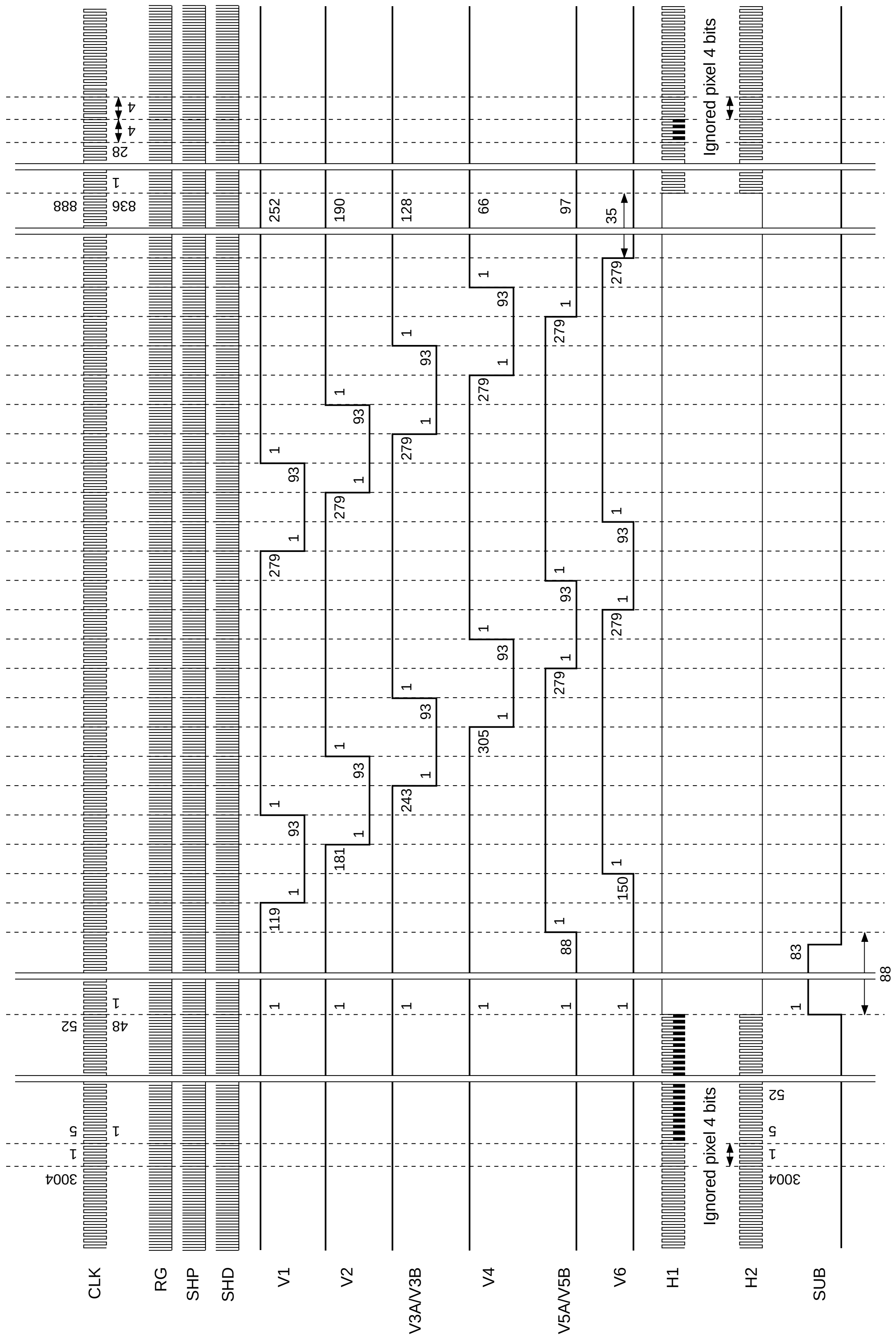


Note) 3004fH, however, 270H in NTSC mode is 2734fH, 324H in PAL mode is 1708fH.

Drive Timing Chart (Readout Portion) NTSC/PAL High Frame Rate Readout Mode/AF Mode

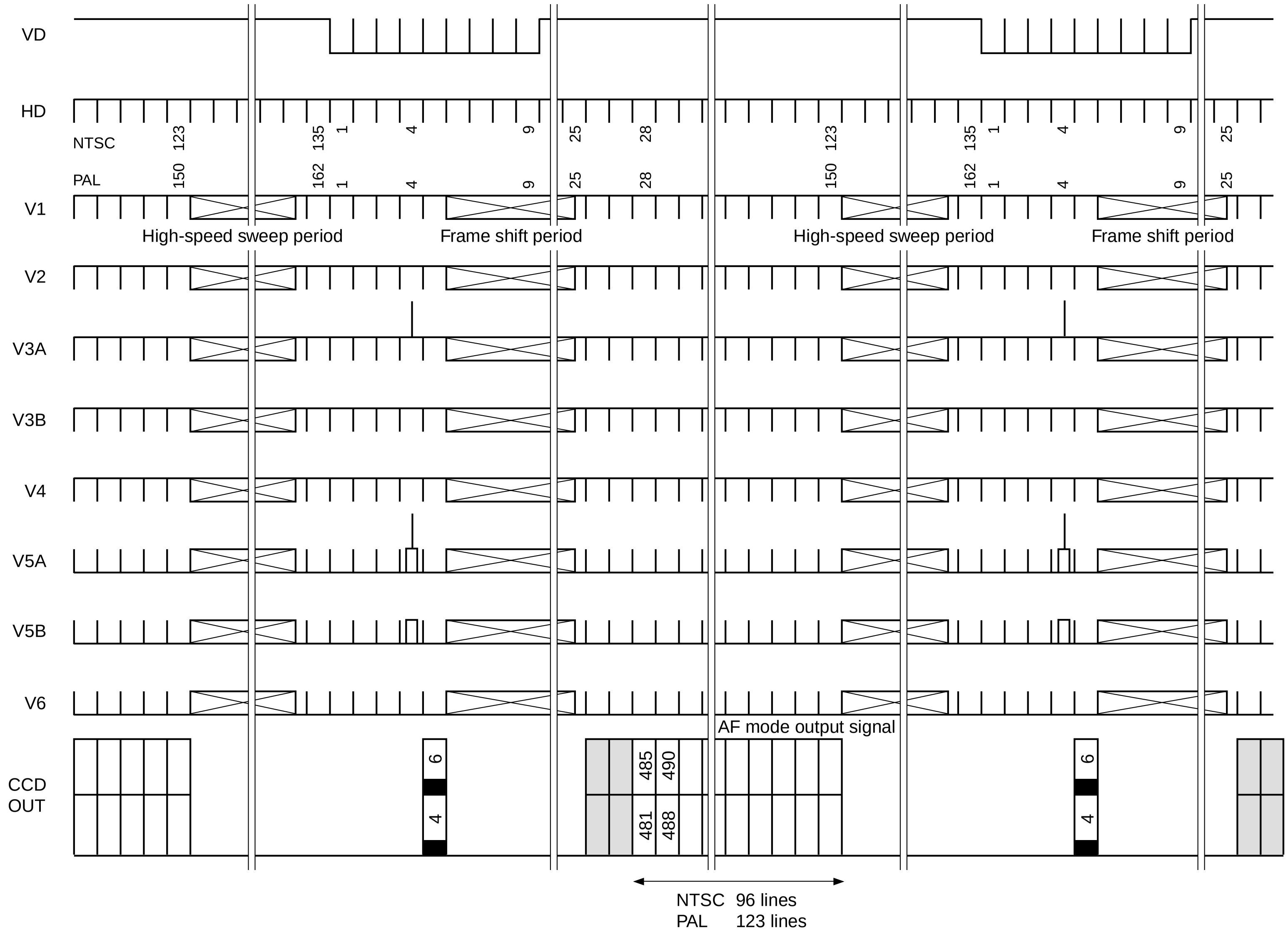


Drive Timing Chart (Horizontal Sync) NTSC/PAL High Frame Rate Readout Mode/AF Mode



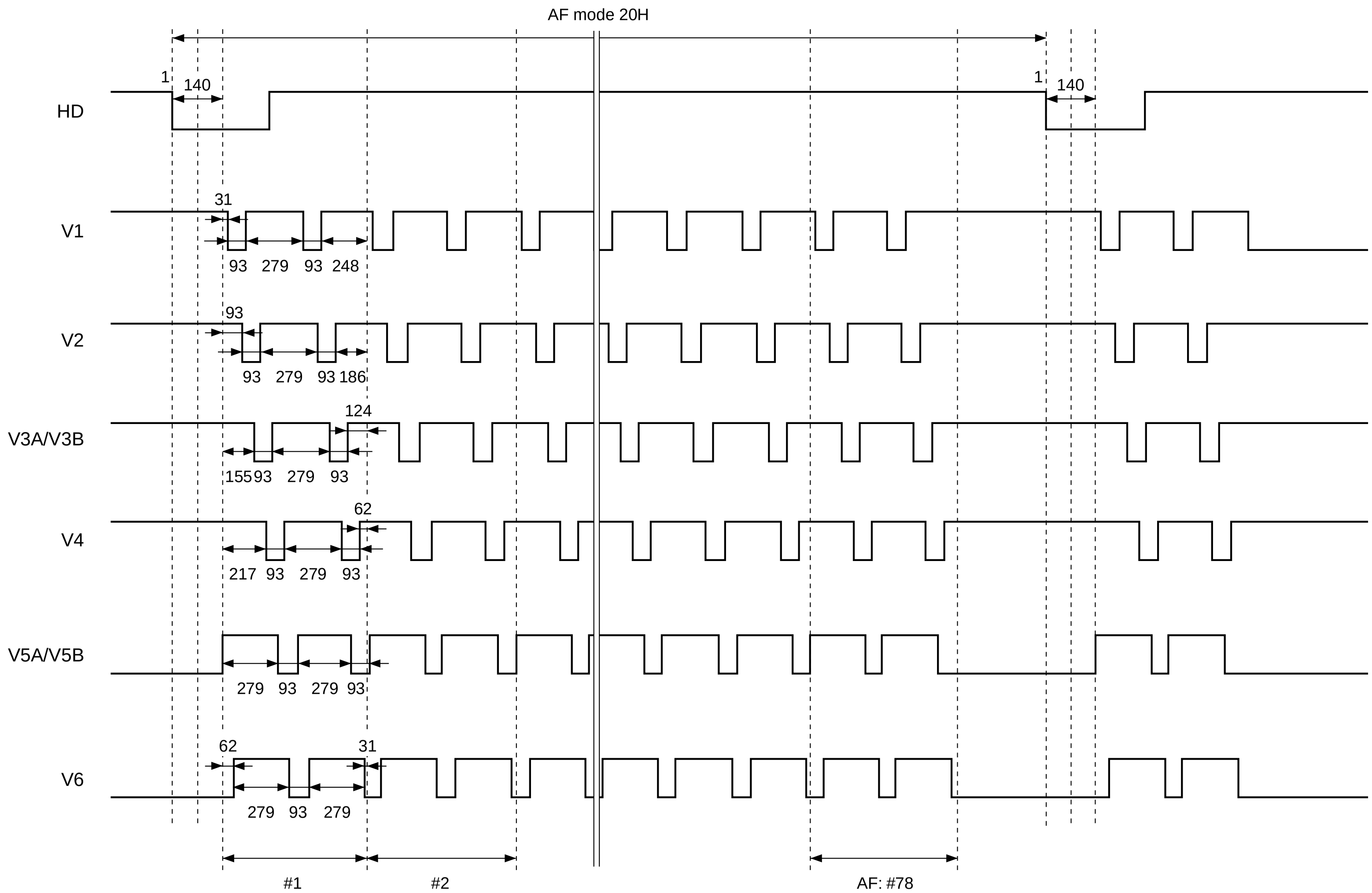
Drive Timing Chart (Vertical Sync) AF Mode

NTSC: 60 frame/s, PAL: 50 frame/s

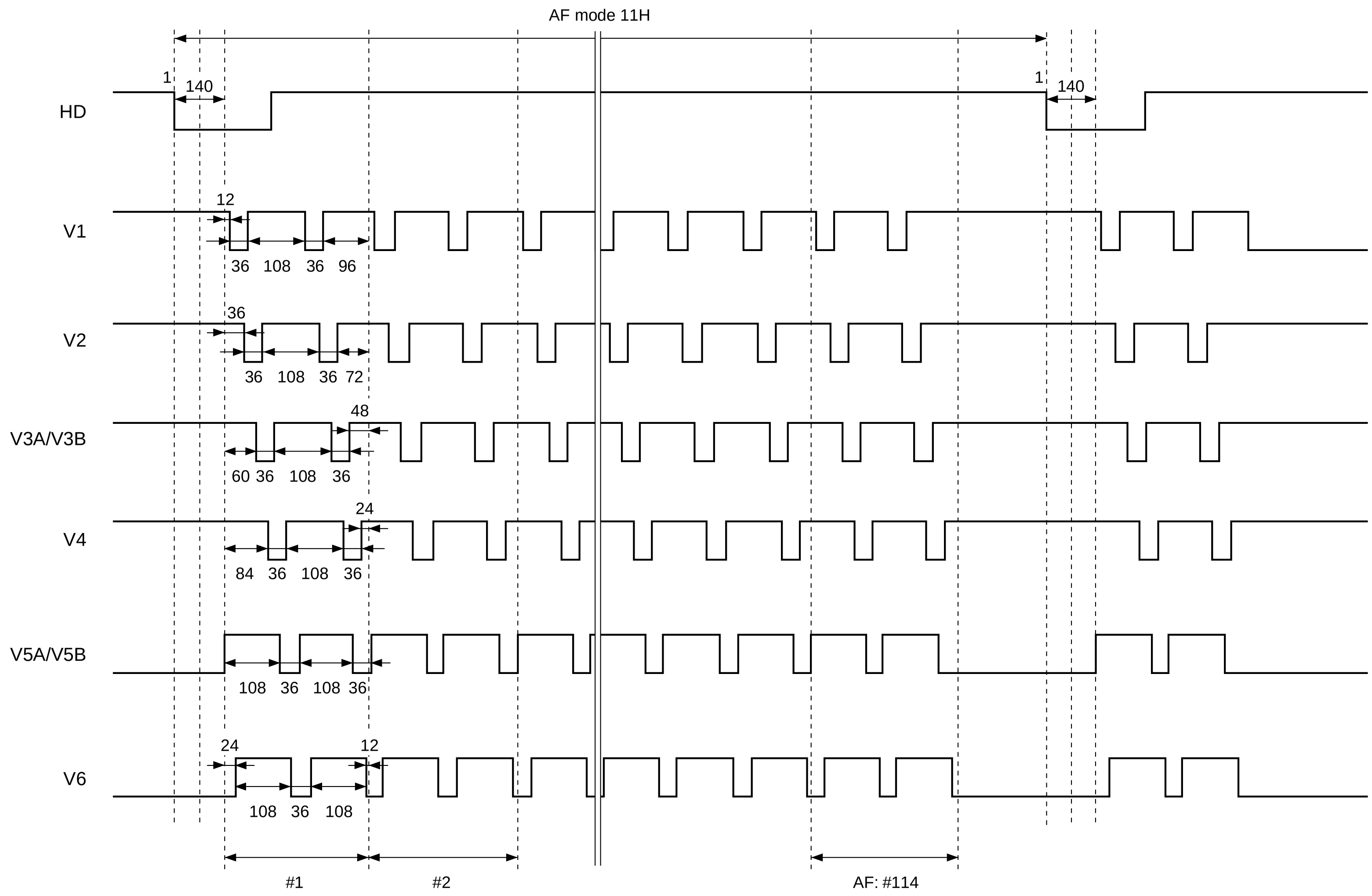


Note) 3004fH, however, 135H in NTSC mode is 2869clk, and 162H in PAL mode is 2356clk.

Drive Timing Chart (High-speed Frame Shift Operation) NTSC/PAL AF Mode



Drive Timing Chart (High-speed Frame Sweep Operation) NTSC/PAL AF Mode



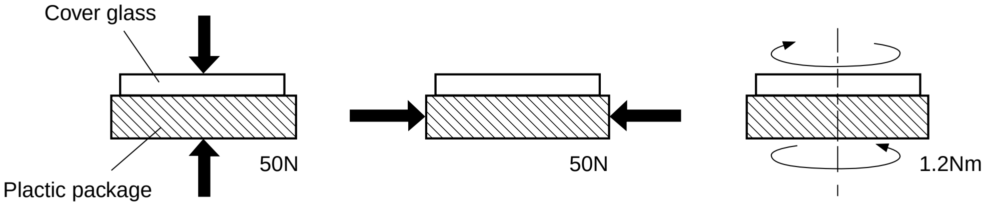
Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.

d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.

f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others

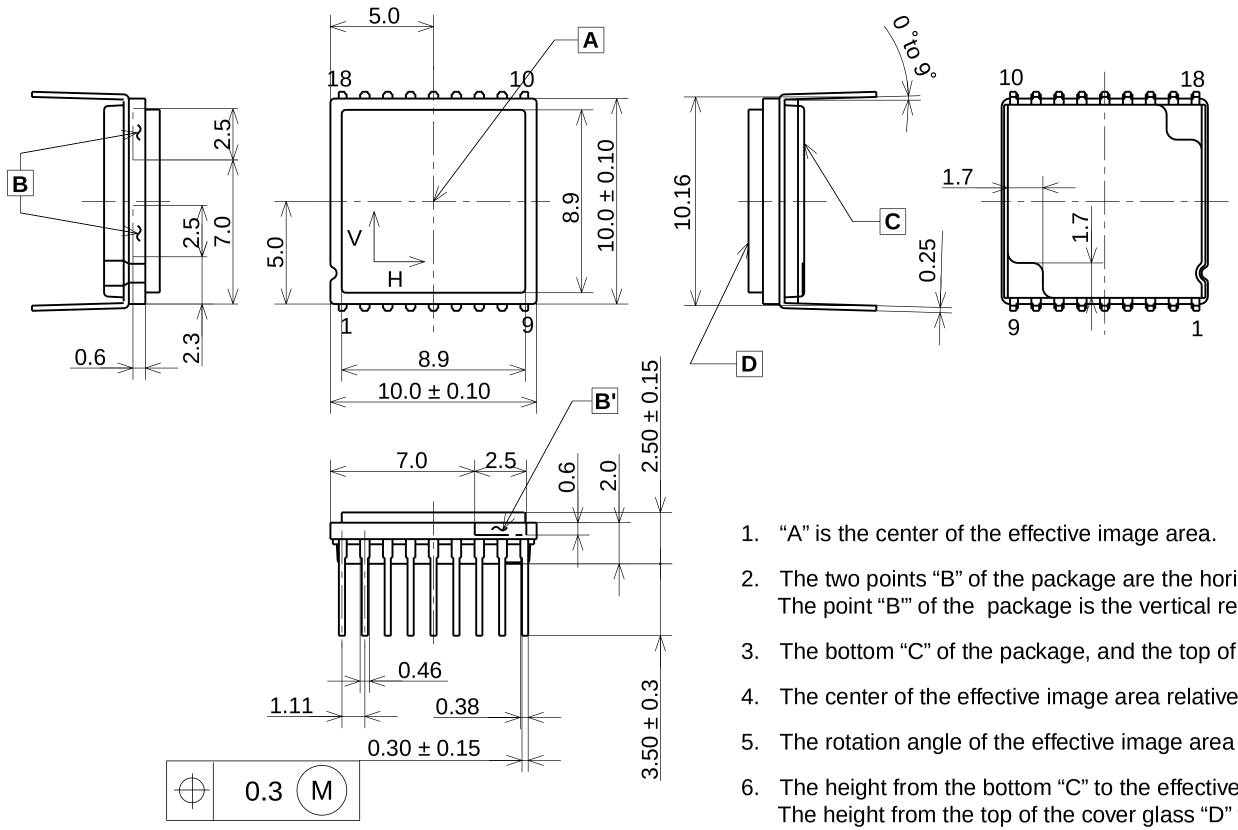
a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.

b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline Unit: mm

18 pin DIP (400mil)



PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.5g
DRAWING NUMBER	AS-C14-02(E)

1. “A” is the center of the effective image area.
2. The two points “B” of the package are the horizontal reference.
   The point “B'” of the package is the vertical reference.
3. The bottom “C” of the package, and the top of the cover glass “D” are the height reference.
4. The center of the effective image area relative to “B” and “B'” is (H, V) = (5.0, 5.0) ± 0.07mm.
5. The rotation angle of the effective image area relative to H and V is ± 0.8˚
6. The height from the bottom “C” to the effective image area is 1.20 ± 0.10mm.
   The height from the top of the cover glass “D” to the effective image area is 1.30 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom “C” is less than 25µm.
   The tilt of the effective image area relative to the top “D” of the cover glass is less than 25µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.