

4.6cm (1.8 Type) Black-and-White LCD Panel

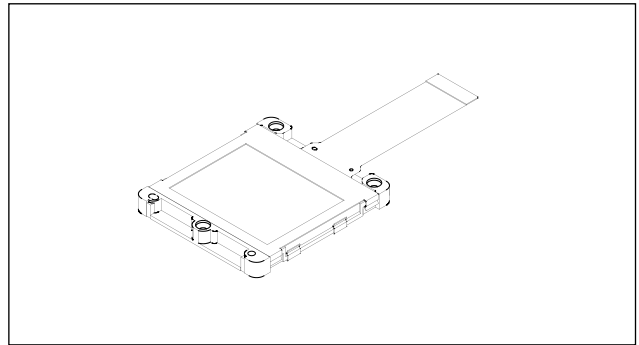
Description

The LCX017DLT is a 4.6cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX017DLT panels provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of DMS (Dual Metal Shield) structure realizes a high luminance screen. And new cross talk free and ghost free structures contribute to high picture quality.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains an active area variable circuit which supports S-XGA 5:4 and PC-98 8:5 data signals by changing the active area according to the type of input signal.



Features

- Number of active dots: 786,432 (1.8 Type, 4.6cm in diagonal)
- Accepts the computer requirements of XGA, SVGA, VGA, NTSC and PAL
- Supports SXGA with simple display
- High optical transmittance: 23% (typ.)
- New high light resistance DMS (Dual Metal Shield) structure adopted
- New cross talk free and ghost free structures
- High contrast ratio with normally white mode: 350 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function
- Antidust glass used

Element Structure

- Dots: 1024 (H) × 768 (V) = 786,432
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

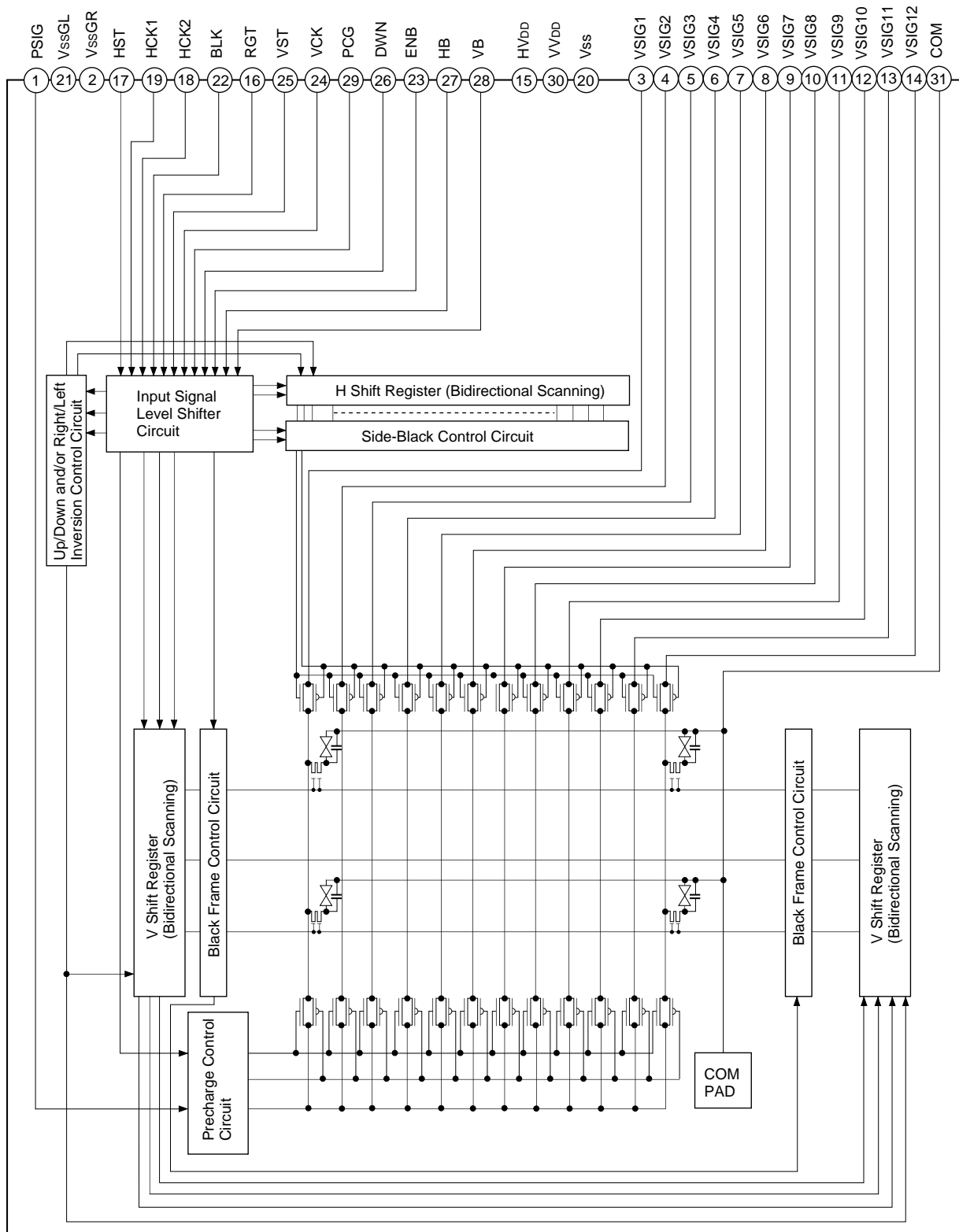
Applications

- Liquid crystal data projectors
- Liquid crystal rear-projector TVs, etc.

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Block Diagram



Absolute Maximum Ratings ($V_{SS} = 0V$)

| | | | |
|--------------------------------------|---|-------------|----|
| • H driver supply voltage | HV _{DD} | -1.0 to +20 | V |
| • V driver supply voltage | VV _{DD} | -1.0 to +20 | V |
| • Common pad voltage | COM | -1.0 to +17 | V |
| • H shift register input pin voltage | HST, HCK1, HCK2, RGT | -1.0 to +17 | V |
| • V shift register input pin voltage | VST, VCK, PCG, BLK, ENB, DWN HB, VB | -1.0 to +17 | V |
| • Video signal input pin voltage | SIG1 to 12, PSIG | -1.0 to +15 | V |
| • Operating temperature* | Topr | -10 to +70 | °C |
| • Storage temperature | Tstg | -30 to +85 | °C |

* Panel temperature inside the ant dust glass

Operating Conditions ($V_{SS} = 0V$)

| | | | |
|---|------------------|-------------|--|
| • Supply voltage | | | |
| | HV _{DD} | 13.5 ± 0.5V | |
| | VV _{DD} | 15.5 ± 0.5V | |
| • Input pulse voltage (V _{p-p} of all input pins except video signal and uniformity improvement signal input pins) | | | |
| | V _{in} | 5.0 ± 0.5V | |

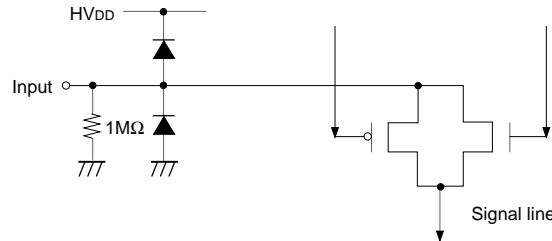
Pin Description

| Pin No. | Symbol | Description |
|---------|--------------------|--|
| 1 | PSIG | Uniformity improvement signal |
| 2 | V _{ss} GR | GND for right V gate |
| 3 | VSIG1 | Video signal 1 to panel |
| 4 | VSIG2 | Video signal 2 to panel |
| 5 | VSIG3 | Video signal 3 to panel |
| 6 | VSIG4 | Video signal 4 to panel |
| 7 | VSIG5 | Video signal 5 to panel |
| 8 | VSIG6 | Video signal 6 to panel |
| 9 | VSIG7 | Video signal 7 to panel |
| 10 | VSIG8 | Video signal 8 to panel |
| 11 | VSIG9 | Video signal 9 to panel |
| 12 | VSIG10 | Video signal 10 to panel |
| 13 | VSIG11 | Video signal 11 to panel |
| 14 | VSIG12 | Video signal 12 to panel |
| 15 | HV _{DD} | Power supply for H driver |
| 16 | RGT | Drive direction pulse for H shift register (H: normal, L: reverse) |
| 17 | HST | Start pulse for H shift register drive |
| 18 | HCK2 | Clock pulse for H shift register drive 2 |
| 19 | HCK1 | Clock pulse for H shift register drive 1 |
| 20 | V _{ss} | GND (H, V drivers) |
| 21 | V _{ss} GL | GND for left V gate |
| 22 | BLK | Input for PC98 mode |
| 23 | ENB | Enable pulse for gate selection |
| 24 | VCK | Clock pulse for V shift register drive |
| 25 | VST | Start pulse for V shift register drive |
| 26 | DWN | Drive direction pulse for V shift register (H: normal, L: reverse) |
| 27 | HB | Display switch for S-XGA |
| 28 | VB | Display switch for PC98 mode |
| 29 | PCG | Improvement pulse for uniformity |
| 30 | VV _{DD} | Power supply for V driver |
| 31 | COM | Common voltage of panel |
| 32 | TEST | Test pin, leave this pin open |

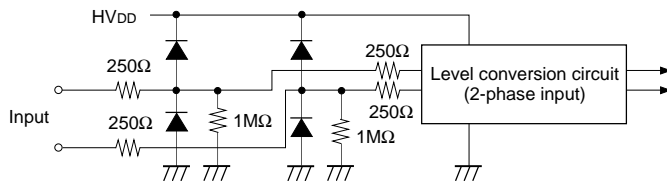
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

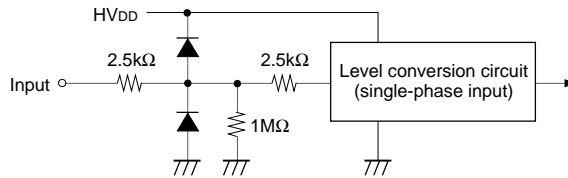
(1) VSIG1 to VSIG12, PSIG



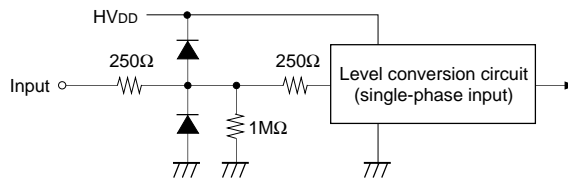
(2) HCK1, HCK2



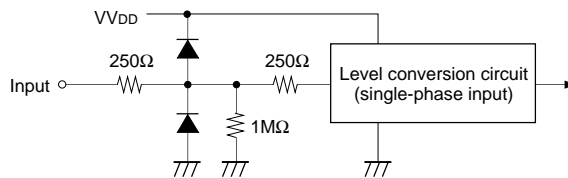
(3) RGT



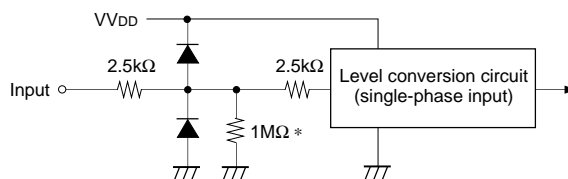
(4) HST



(5) PCG, VCK

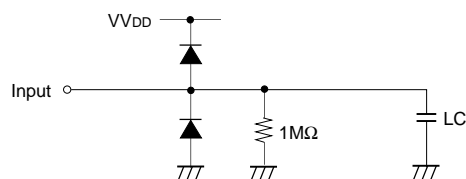


(6) VST, BLK, ENB, DWN, HB, VB

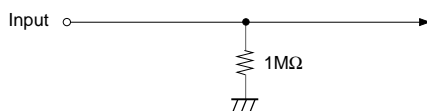


* DWN is 400kΩ.

(7) COM



(8) HVDD, VssGR, VssGL, VVDD



are all Vss.

Input Signals

1. Input signal voltage conditions ($V_{SS} = 0V$)

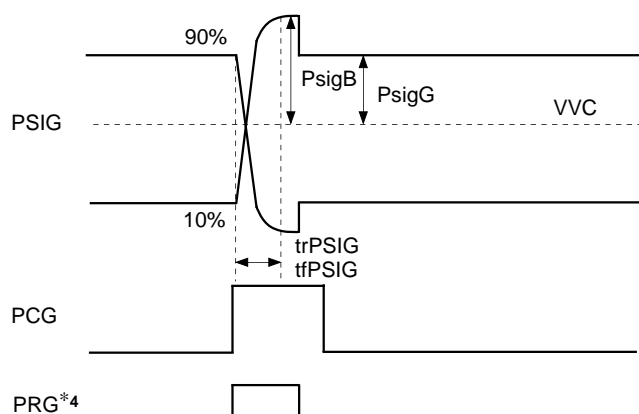
| Item | Symbol | Min. | Typ. | Max. | Unit | |
|---|--------|---------------|---------------|---------------|------|---|
| H shift register input voltage HST, HCK1, HCK2, RGT | (Low) | VHIL | -0.5 | 0.0 | 0.4 | V |
| | (High) | VHIH | 4.5 | 5.0 | 5.5 | V |
| V shift register input voltage HB, VB, BLK, VST, VCK, PCG, ENB, DWN | (Low) | VVIL | -0.5 | 0.0 | 0.4 | V |
| | (High) | VVIH | 4.5 | 5.0 | 5.5 | V |
| Video signal center voltage | VVC | 6.9 | 7.0 | 7.1 | V | |
| Video signal input range*1 | Vsig | $VVC - 4.5$ | 7.0 | $VVC + 4.5$ | V | |
| Common voltage of panel*2 | Vcom | $VVC - 0.5$ | $VVC - 0.4$ | $VVC - 0.3$ | V | |
| Uniformity improvement signal input voltage (PSIG)*3 | VpsigB | $VVC \pm 4.4$ | $VVC \pm 4.5$ | $VVC \pm 4.6$ | V | |
| | VpsigG | $VVC \pm 1.8$ | $VVC \pm 1.9$ | $VVC \pm 2.0$ | | |

*1 Input video signal shall be symmetrical to VVC.

*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value. When the typical value is lowered, the maximum and minimum values may lower.

*3 Input a uniformity improvement signal PSIG in the same polarity with video signals VSIG1 to VSIG12 and which is symmetrical to VVC. PSIG wave form is 2 steps like below, in the upper chart, upper shows signal level of the 1st step, lower shows signal level of the 2nd step. Also, the rising and falling of PSIG are synchronized with the rising of PCG pulse, and the rise time tr_{PSIG} and fall time tf_{PSIG} are suppressed within 450ns (as shown in a diagram below).

Input waveform of uniformity improvement signal PSIG



*4 PRG shows the time of the 1st step of PSIG signal, and it is not input to the panel.

Level Conversion Circuit

The LCX017DLT has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD} . The V_{CC} of external ICs are applicable to $5 \pm 0.5V$.

2. Clock timing conditions (Ta = 25°C)

(XGA mode: fHckn = 3.9MHz, fVck = 34.3kHz)

| | Item | Symbol | Min. | Typ. | Max. | Unit |
|-------------------|--|---------------------|------|------|------|------|
| HST | Hst rise time | trHst | — | — | 30 | ns |
| | Hst fall time | tfHst | — | — | 30 | |
| | Hst data set-up time | tdHst | 55 | 65 | 75 | |
| | Hst data hold time | thHst | 55 | 65 | 75 | |
| HCK | Hckn rise time* ⁵ | trHckn | — | — | 30 | ns |
| | Hckn fall time* ⁵ | tfHckn | — | — | 30 | |
| | Hck1 fall to Hck2 rise time | to1Hck | -15 | 0 | 15 | |
| | Hck1 rise to Hck2 fall time | to2Hck | -15 | 0 | 15 | |
| VST | Vst rise time | trVst | — | — | 100 | μs |
| | Vst fall time | tfVst | — | — | 100 | |
| | Vst data set-up time | tdVst | 2 | 7 | 12 | |
| | Vst data hold time | thVst | 2 | 7 | 12 | |
| VCK | Vck rise time | trVck | — | — | 100 | μs |
| | Vck fall time | tfVck | — | — | 100 | |
| ENB | Enb rise time | trEnb | — | — | 100 | ns |
| | Enb fall time | tfEnb | — | — | 100 | |
| | Horizontal video period completed to Enb fall time | tdEnb | 760 | 800 | — | |
| | Enb rise to PRG* ⁴ fall time | toPRG* ⁴ | 110 | 120 | 130 | |
| | Enb fall to Pcg rise time | toPcg | 830 | 1000 | — | |
| | Enb pulse width | twEnb | 1650 | — | — | |
| PCG | Pcg rise time | trPcg | — | — | 30 | ns |
| | Pcg fall time | tfPcg | — | — | 30 | |
| | Pcg rise to Vck rise/fall time | toVck | -100 | 0 | 100 | |
| | Pcg fall to horizontal video period start time | toVideo | 170 | 200 | — | |
| | Pcg pulse width | twPcg | 1400 | 1700 | — | |
| PRG* ⁴ | PRG* ⁴ rise to Pcg rise time | toPcgr | -10 | 0 | 10 | ns |
| | PRG* ⁴ fall to Pcg fall time | toPcgf | 570 | 700 | — | |
| | PRG* ⁴ pulse width | twPRG* ⁴ | 830 | 1000 | — | |
| BLK* ⁵ | Blk rise time | trBlk | — | — | 100 | μs |
| | Blk fall time | tfBlk | — | — | 100 | |
| | Blk rise to Enb fall time | toEnb | 2 | 1 | 0 | |
| | Blk fall to Pcg rise time | toPcg | -1 | 0 | 1 | |

*⁵ Hckn means Hck1 and Hck2.*⁶ Blk is the timing during PC98 mode, which keeps "H" level in other modes.

<Horizontal Shift Register Driving Waveform>

| Item | | Symbol | Waveform | Conditions |
|------|------------------------------|--------|----------|--|
| HST | Hst rise time | trHst | | <ul style="list-style-type: none"> • Hckn^{*5} duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Hst fall time | tfHst | | |
| | Hst data set-up time | tdHst | | |
| | Hst data hold time | thHst | | |
| HCK | Hckn rise time ^{*5} | trHckn | | <ul style="list-style-type: none"> • Hckn^{*5} duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Hckn fall time ^{*5} | tfHckn | | |
| | Hck1 fall to Hck2 rise time | to1Hck | | |
| | Hck1 rise to Hck2 fall time | to2Hck | | |

^{*7} Definitions: The right-pointing arrow ($\bullet \rightarrow$) means +.

The left-pointing arrow ($\leftarrow \bullet$) means -.

The black dot at an arrow (\bullet) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

| Item | | Symbol | Waveform | Conditions |
|-----------------|--|---------|----------|------------|
| VST | Vst rise time | trVst | | |
| | Vst fall time | tfVst | | |
| | Vst data set-up time | tdVst | | |
| | Vst data hold time | thVst | | |
| VCK | Vck rise time | trVck | | |
| | Vck fall time | tfVck | | |
| ENB | Enb rise time | trEnb | | |
| | Enb fall time | tfEnb | | |
| | Horizontal video period completed to Enb fall time | tdEnb | | |
| | Enb rise to PRG*4 fall time | toPRG*4 | | |
| | Enb fall to Pcg rise time | toPcg | | |
| Enb pulse width | twEnb | | | |

| Item | | Symbol | Waveform | Conditions |
|----------|--|---------|----------|------------|
| PCG*8 | Pcg rise time | trPcg | | |
| | Pcg fall time | tfPcg | | |
| | Pcg rise to Vck rise/fall time | toVck | | |
| | Pcg fall to horizontal video period start time | toVideo | | |
| | Pcg pulse width | twPcg | | |
| *8 PRG*4 | PRG*4 rise to Pcg rise time | toPcgr | | |
| | PRG*4 fall to Pcg fall time | toPcgf | | |
| | PRG*4 pulse width | twPRG*4 | | |
| BLK | Blk rise time | trBlk | | |
| | Blk fall time | tfBlk | | |
| | Blk rise to Enb fall time | toEnb | | |
| | Blk fall to Pcg rise time | toPcg | | |

*8 PCG input pin and PRG*4 should be "H" level during the horizontal 1H period, where the above BLK is low more than 10ns.

Electrical Characteristics ($T_a = 25^\circ\text{C}$, $HV_{DD} = 13.5\text{V}$, $VV_{DD} = 15.5\text{V}$)**1. Horizontal drivers**

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition | |
|------------------------------------|--------|-------|-------|------|------|---------------------------|------------|
| Input pin capacitance | HCKn | CHckn | — | 30 | 35 | pF | |
| | HST | CHst | — | 35 | 40 | pF | |
| Input pin current | HCK1 | | -500 | -220 | — | μA | HCK1 = GND |
| | HCK2 | | -1000 | -390 | — | μA | HCK2 = GND |
| | HST | | -500 | -120 | — | μA | HST = GND |
| | RGT | | -150 | -30 | — | μA | RGT = GND |
| Video signal input pin capacitance | Csig | — | 200 | 250 | pF | | |
| Current consumption | IH | — | 14.0 | 20.0 | mA | HCKn: HCK1, HCK2 (3.9MHz) | |

2. Vertical drivers

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition | |
|----------------------------|---------|------|-------|------|------|----------------|------------------------------------|
| Input pin capacitance | VCK | CVck | — | 15 | 20 | pF | |
| | VST | CVst | — | 15 | 20 | pF | |
| Input pin current | VCK,PCG | | -1000 | -180 | — | μA | VCK = GND, PCG = GND |
| VST, ENB, DWN, BLK, HB, VB | | | -150 | -40 | — | μA | VST, ENB, DWN, BLK, HB VB = GND |
| Current consumption | IV | — | 4.0 | 6.0 | mA | VCK: (34.3kHz) | |

3. Total power consumption of the panel

| Item | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|--------|------|------|------|------|
| Total power consumption of the panel | PWR | — | 250 | 400 | mW |

4. Pin input resistance

| Item | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------|--------|------|------|------|------------------|
| Pin – Vss input resistance | Rpin | 0.4 | 1 | — | $\text{M}\Omega$ |

5. Uniformity improvement signal

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|------|------|------|------|
| Input pin capacitance for uniformity improvement signal | CPSIGo | — | 13 | 16 | nF |

6. COM pin capacitance

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---------------------|--------|------|------|------|------|
| COM pin capacitance | COM | — | 20 | 25 | nF |

Electro-optical Characteristics

(XGA mode)

| Item | | Symbol | Measurement method | Min. | Typ. | Max. | Unit | |
|-----------------------|-----------------|--------|---------------------|------|------|------|------|----|
| Contrast ratio | | 25°C | CR | 1 | 200 | 350 | — | |
| Optical transmittance | | 25°C | T | 2 | 20 | 23 | — | |
| V-T characteristics | V ₉₀ | 25°C | RV ₉₀₋₂₅ | 3 | 0.7 | 1.1 | 1.5 | V |
| | | | GV ₉₀₋₂₅ | | 0.9 | 1.3 | 1.6 | |
| | | | BV ₉₀₋₂₅ | | 1.0 | 1.4 | 1.7 | |
| | | 60°C | RV ₉₀₋₆₀ | | 0.7 | 1.1 | 1.4 | |
| | | | GV ₉₀₋₆₀ | | 0.8 | 1.2 | 1.5 | |
| | | | BV ₉₀₋₆₀ | | 1.0 | 1.4 | 1.7 | |
| | V ₅₀ | 25°C | RV ₅₀₋₂₅ | | 1.1 | 1.5 | 1.8 | |
| | | | GV ₅₀₋₂₅ | | 1.2 | 1.6 | 1.9 | |
| | | | BV ₅₀₋₂₅ | | 1.3 | 1.7 | 2.0 | |
| | | 60°C | RV ₅₀₋₆₀ | | 1.1 | 1.5 | 1.8 | |
| | | | GV ₅₀₋₆₀ | | 1.2 | 1.6 | 1.9 | |
| | | | BV ₅₀₋₆₀ | | 1.3 | 1.7 | 2.0 | |
| | V ₁₀ | 25°C | RV ₁₀₋₂₅ | | 1.6 | 2.0 | 2.3 | |
| | | | GV ₁₀₋₂₅ | | 1.7 | 2.1 | 2.4 | |
| | | | BV ₁₀₋₂₅ | | 1.8 | 2.2 | 2.5 | |
| | | 60°C | RV ₁₀₋₆₀ | | 1.6 | 2.0 | 2.3 | |
| | | | GV ₁₀₋₆₀ | | 1.7 | 2.1 | 2.4 | |
| | | | BV ₁₀₋₆₀ | | 1.8 | 2.2 | 2.5 | |
| Response time | ON time | 0°C | ton0 | 4 | — | 37 | 80 | ms |
| | | 25°C | ton25 | | — | 17 | 40 | |
| | OFF time | 0°C | toff0 | | — | 100 | 200 | |
| | | 25°C | toff25 | | — | 30 | 70 | |
| Flicker | | 60°C | F | 5 | — | -65 | -40 | dB |
| Image retention time | | 25°C | YT60 | 6 | — | 0 | — | s |
| Cross talk | | 25°C | CTK | 7 | — | — | 5 | % |

Reflection Preventive Processing

When a phase substrate which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a phase substrate with reflection preventive processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

HV_{DD} = 13.5V, VV_{DD} = 15.5V

VV_C = 7.0V, V_{com} = 6.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

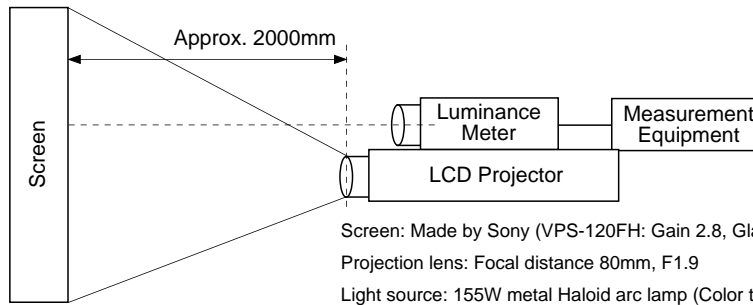
(4) Measurement systems

Two types of measurement systems are used as shown below.

(5) Video input signal voltage (V_{sig})

V_{sig} = 7.0 ± V_{AC} [V] (V_{AC} = signal amplitude)

• Measurement system I



Screen: Made by Sony (VPS-120FH: Gain 2.8, Glass Beaded Type) or equivalent

Projection lens: Focal distance 80mm, F1.9

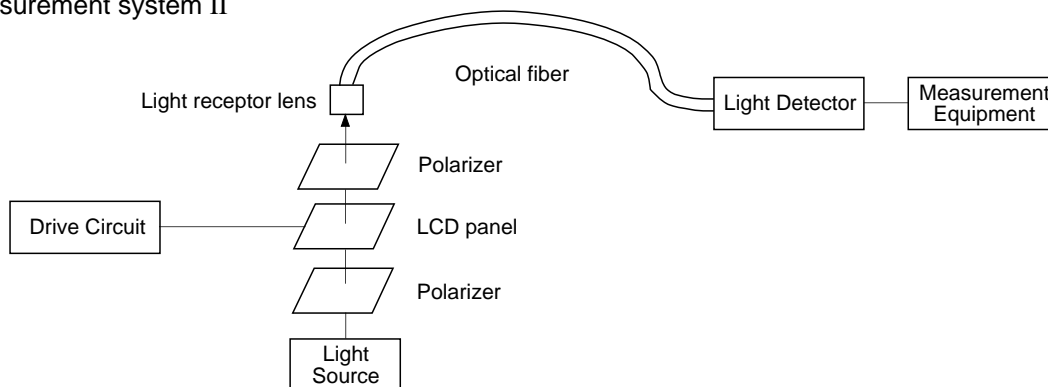
Light source: 155W metal Haloid arc lamp (Color temperature 7500K ± 500)

(× 24, Sensor area: 7mmφ)

Polarizer: Side of incidence - Nitto Denko's EG-1224DU or Polatechno's SKN-18242T or equivalent

Side of output light - Polatechno's SHC-128 or equivalent

• Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L(\text{White})}{L(\text{Black})} \dots (1)$$

L (White): Surface luminance of the center of the screen at the input signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the center of the screen at V_{AC} = 4.5V.

Both luminosities are measured by System I.

2. Optical Transmittance

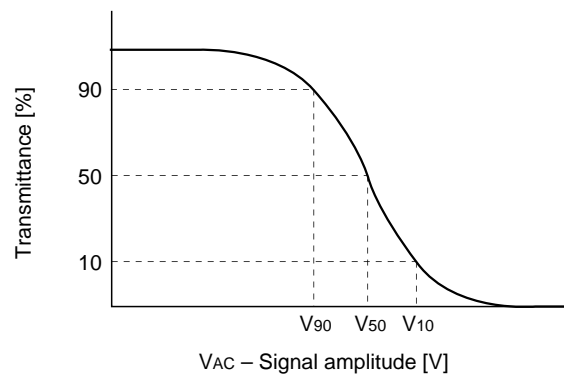
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100 [\%] \dots (2)$$

"White luminance" means the maximum luminance on the screen at the input signal amplitude $V_{AC} = 0.5V$ on Measurement System I.

3. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panels, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90} , V_{50} , and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



4. Response Time

Response time t_{on} and t_{off} are defined by formulas (5) and (6) respectively.

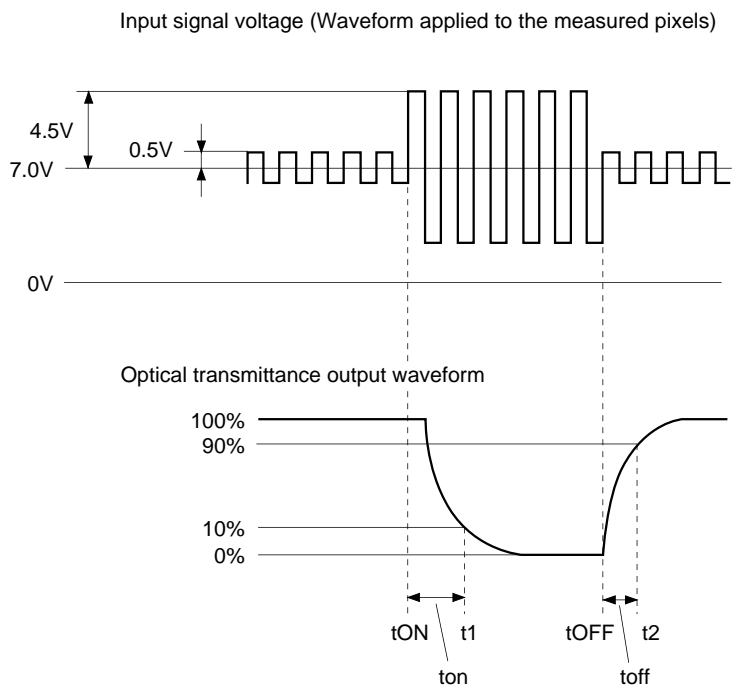
$$t_{on} = t_1 - t_{ON} \dots (5)$$

$$t_{off} = t_2 - t_{OFF} \dots (6)$$

t_1 : time which gives 10% transmittance of the panel.

t_2 : time which gives 90% transmittance of the panel.

The relationships between t_1 , t_2 , t_{ON} and t_{OFF} are shown in the right figure.



5. Flicker

Flicker (F) is given by formula (7). DC and AC (XGA/NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

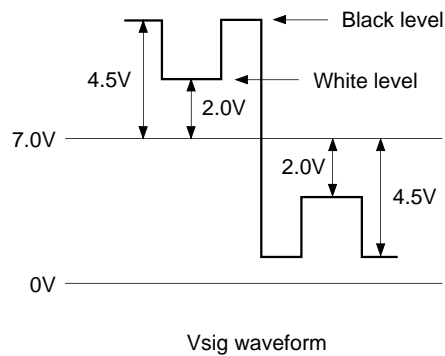
$$F [dB] = 20 \log \left\{ \frac{\text{AC component}}{\text{DC component}} \right\} \dots(7)$$

* Each input signal voltage for gray raster mode is given by $V_{sig} = 7.0 \pm V_{50}$ [V] where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6. Image Retention Time

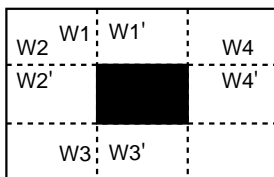
Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of $V_{sig} = 7.0 \pm V_{AC}$ (V_{AC} : 3 to 4V). Judging by sight at the V_{AC} that holds the maximum image retention, measure the time till the residual image becomes indistinct.

* Monoscope signal conditions:
 $V_{sig} = 7.0 \pm 4.5$ or ± 2.0 [V]
 (shown in the right figure)
 $V_{com} = 6.6V$



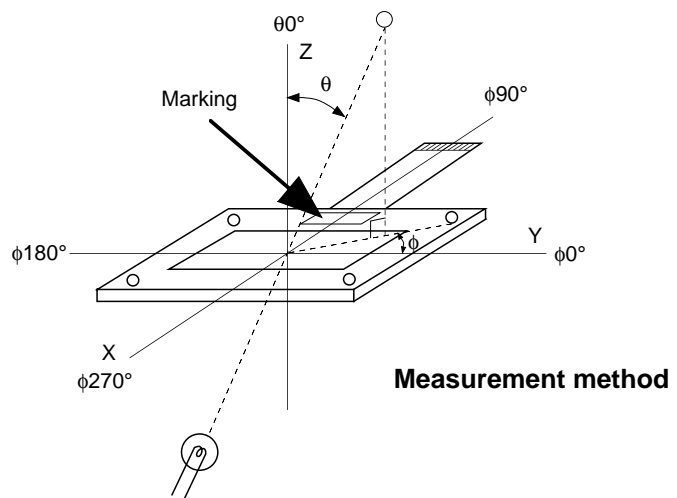
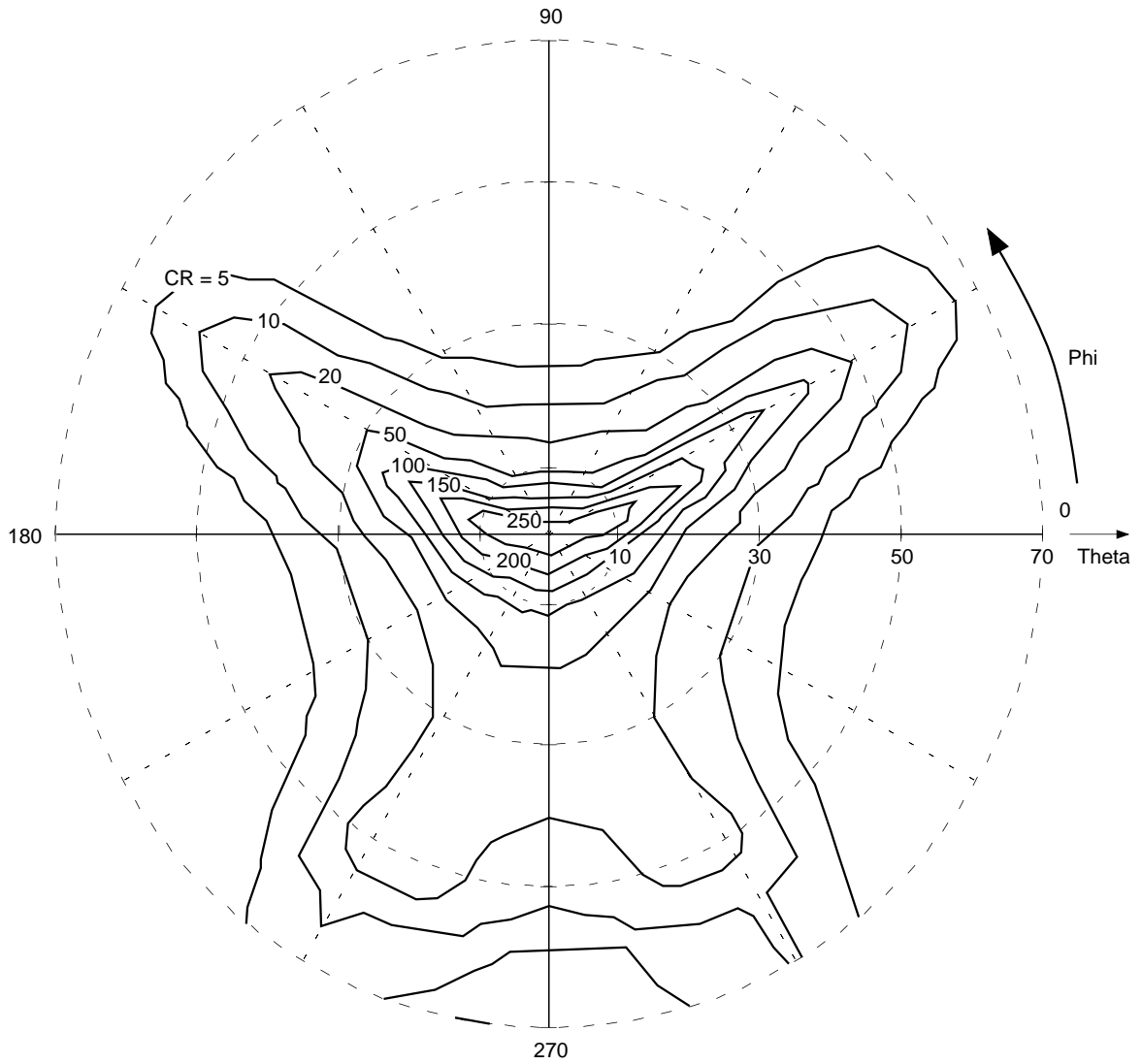
7. Cross Talk

Cross talk is determined by the luminance differences between adjacent areas represented by W_i' and W_i ($i = 1$ to 4) around a black window ($V_{sig} = 4.5 V/1V$).



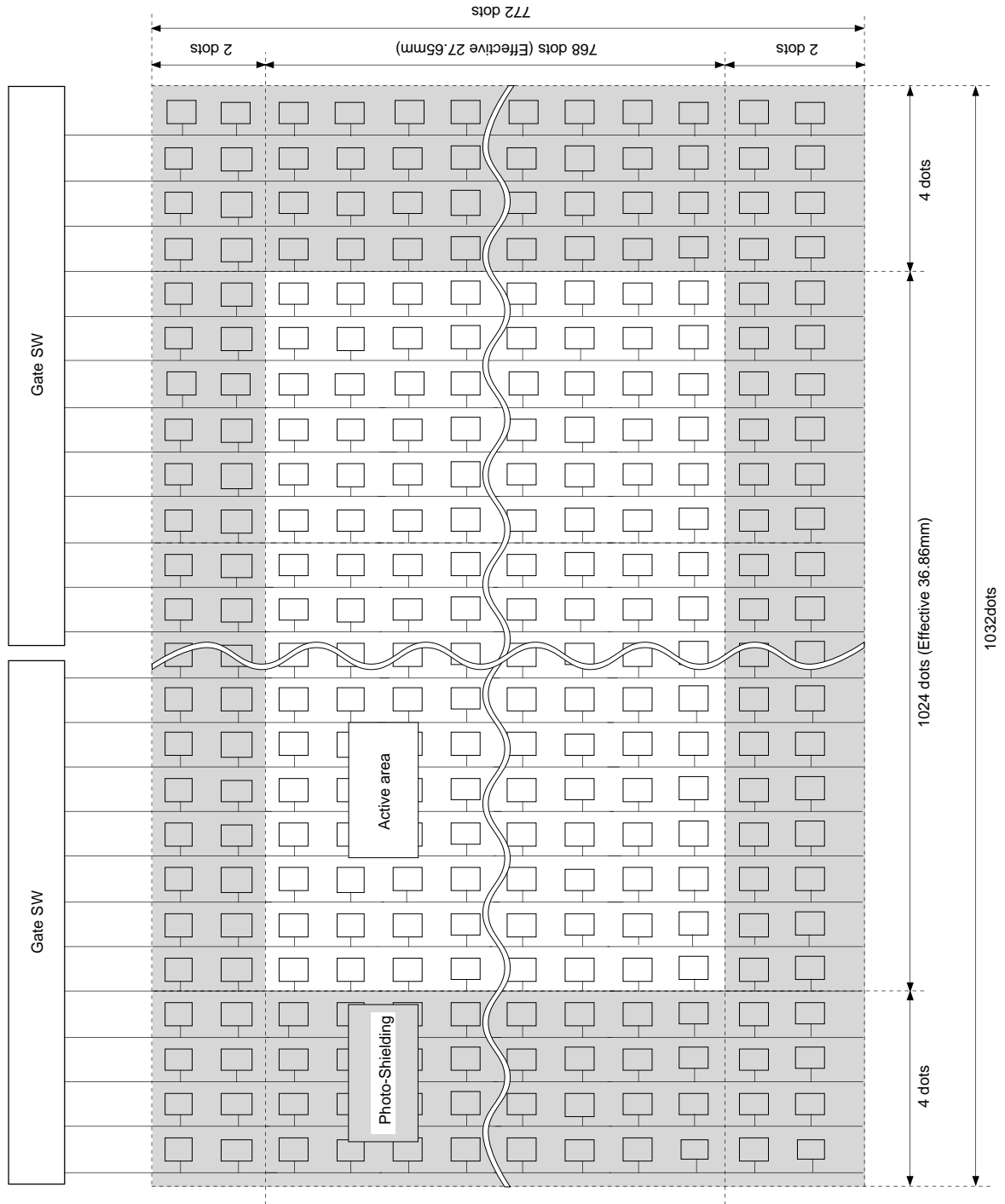
$$\text{Cross talk value CTK} = \left| \frac{W_i' - W_i}{W_i} \right| \times 100 [\%]$$

Viewing angle characteristics (Typical Value)



1. Dot Arrangement

The dots are arranged in a stripe. The shaded area is used for the dark border around the display.



2. LCD Panel Operations

[Description of basic operations]

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 768 gate lines sequentially in a single horizontal scanning period. (XGA mode)
- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 1024 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.
- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs) turn on to apply a video signal to the dot. The same procedures lead to the entire 768 × 1024 dots to display a picture in a single vertical scanning period.
- The data and video signals shall be input with the 1H-inverted system.

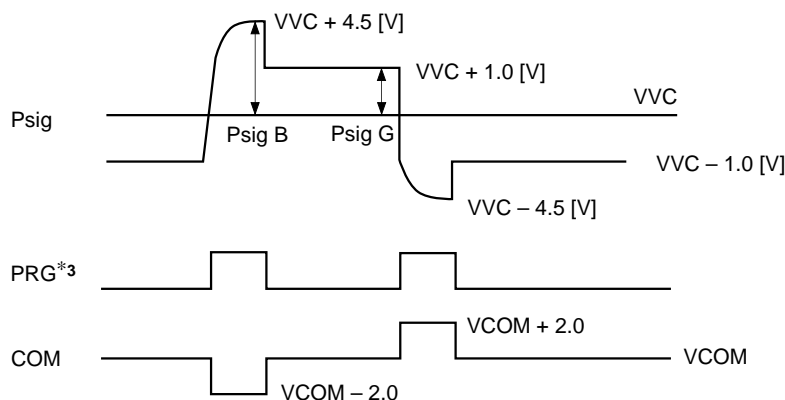
[Description of operating mode]

This LCD panel can change the active area by displaying a black frame to support various computer or video signals. The active area is switched by HB, VB and BLK. However, the center of the screen is not changed. The active area setting modes are shown below.

| HB | VB | BLK | Screen aspect ratio |
|----|----|-----|---------------------|
| H | H | H | 4:3 1024 × 768 |
| L | H | H | 5:4*2 960 × 768 |
| H | L | *1 | 8:5 1024 × 640 |

*1 Input BLK pulse (refer to drive waveform and vertical blanking period of PC98 made).

*2 For only aspect ratio 5:4 mode, set P_{sig} and COM voltage as shown below. The value of P_{sig}G and COM voltage is typical value. It is necessary to optimize the voltage for each set construction.



*3 PRG shows the time of the 1st step of P_{sig} signal, and it is not input to the panel.

This LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and/or up/down setting modes are shown below.

| RGT | Mode |
|-----|------------|
| H | Right scan |
| L | Left scan |

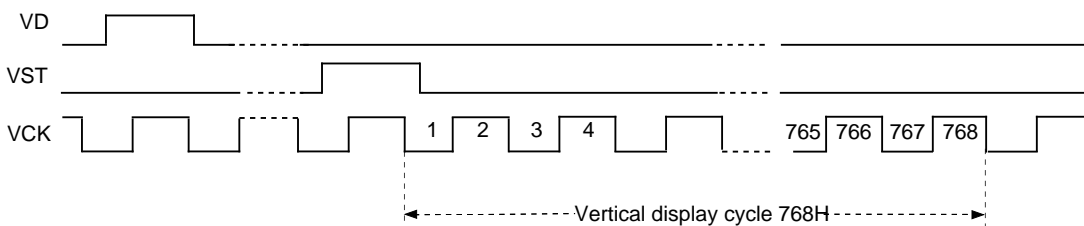
| DWN | Mode |
|-----|-----------|
| H | Down scan |
| L | Up scan |

Right/left and/or up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

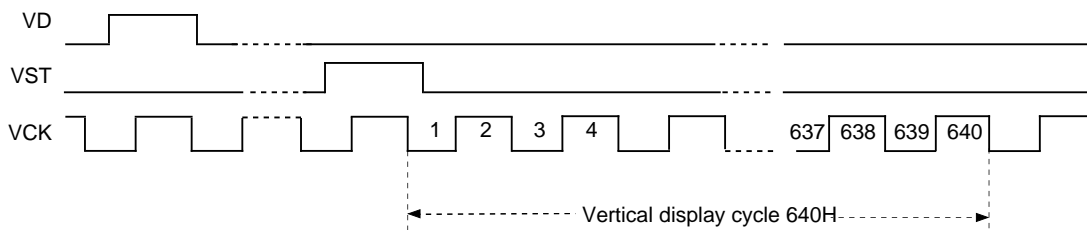
To locate the active area in the center of the panel in each mode, polarity of the start pulse and clock phase for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown below.

(1) Vertical direction display cycle (DWN = H, L)

(1.1) XGA, SXGA

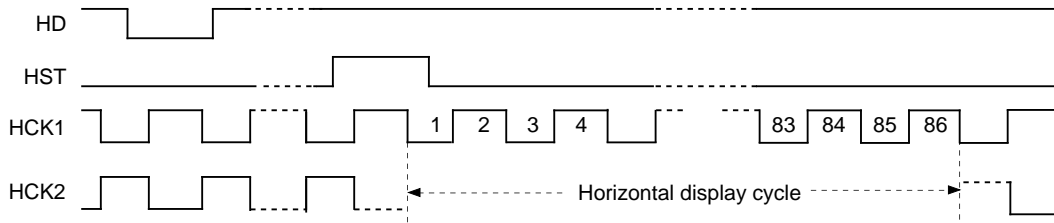


(1.2) PC98

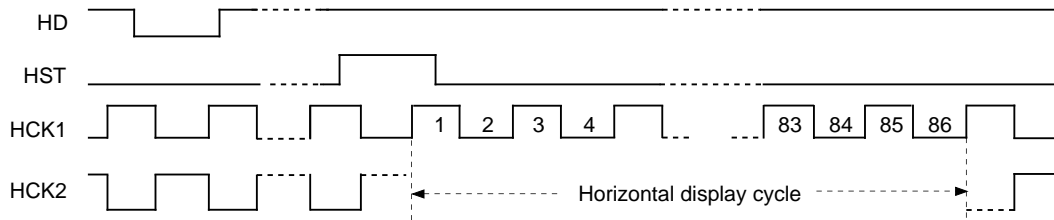


(2) Horizontal direction display cycle

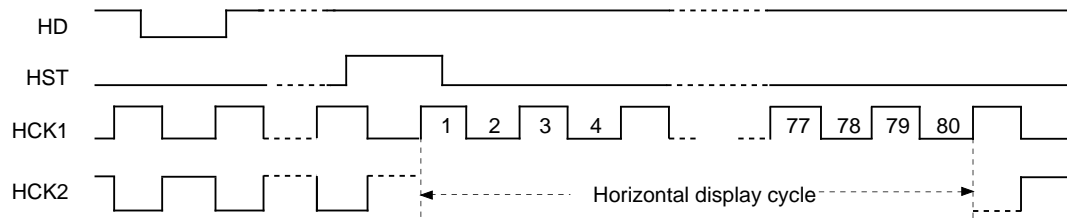
(2.1.1) XGA, PC98 (RGT = H)



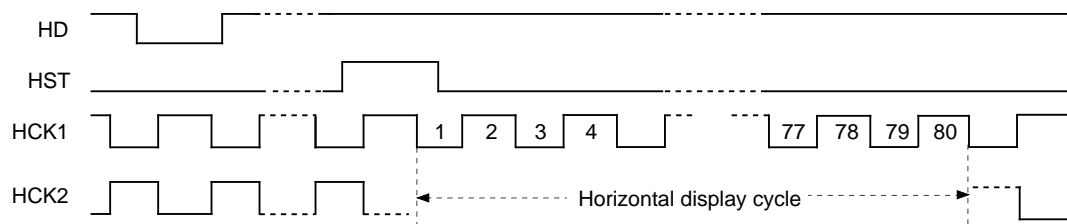
(2.1.2) XGA, PC98 (RGT = L)



(2.2.1) SXGA (RGT = H)

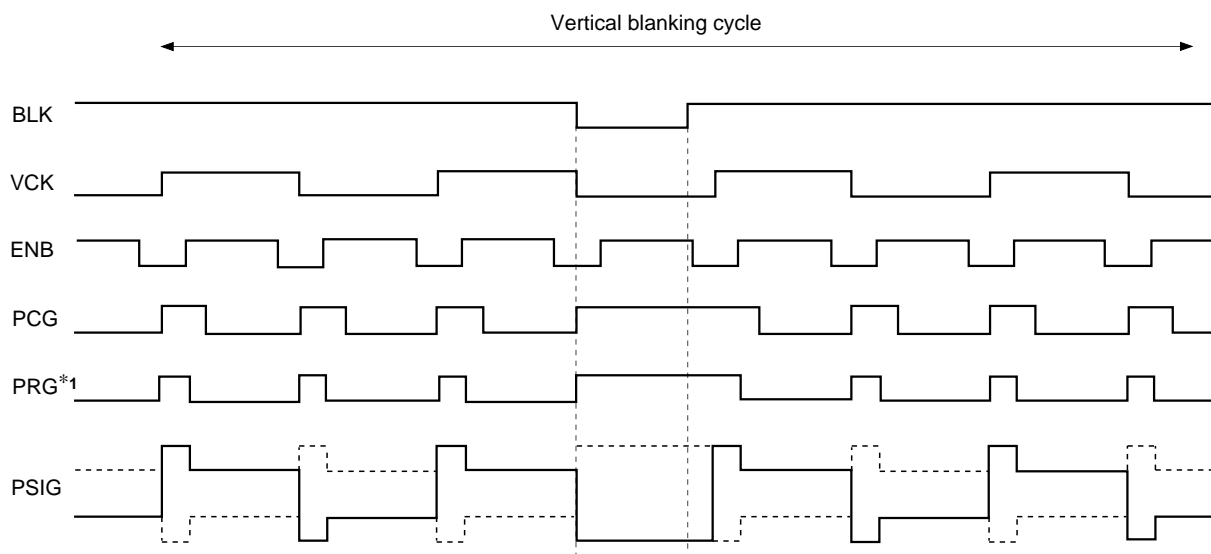


(2.2.2) SXGA (RGT = L)



(3) Vertical blanking cycle of PC98 mode

The input waveforms of PCG, PRG*1 and PSIG should be changed as shown below when BLK pulse is input.

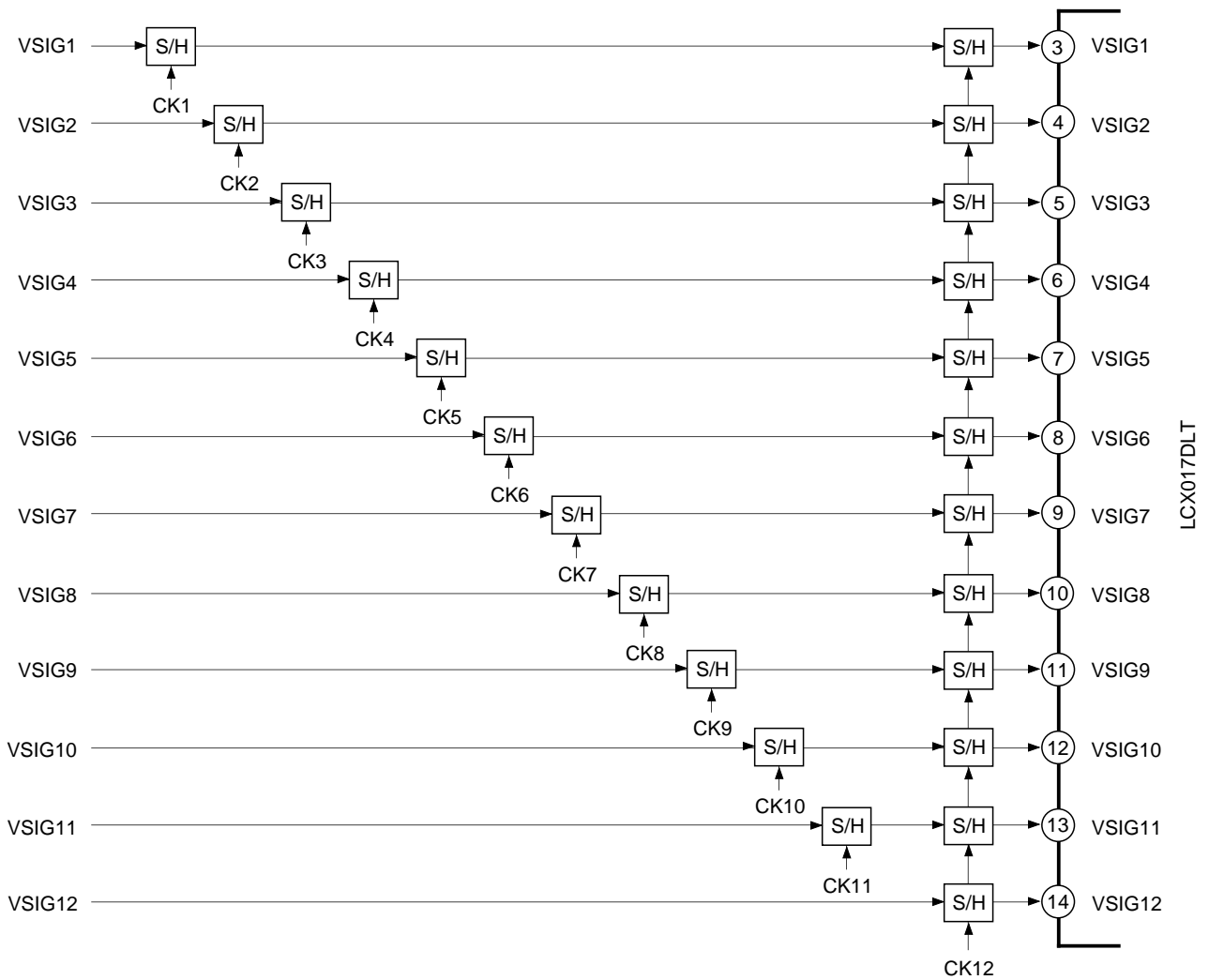


*1 PRG shows the period of PSIG black level, it is not input to the panel.

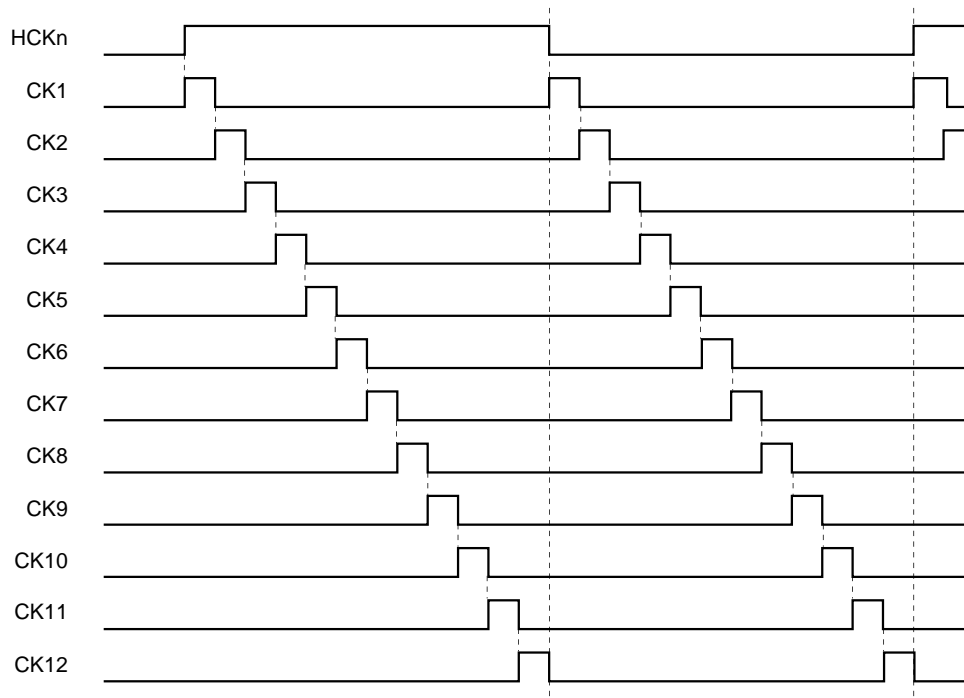
3. 12-dot Simultaneous Sampling

The horizontal shift register samples signals VSIG1 to VSIG12 simultaneously. This requires phase matching between signals VSIG1 to VSIG12 to prevent the horizontal resolution from deteriorating. Thus, phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High level). For left scan (RGT = Low level), the phase settings for signals VSIG1 to VSIG12 are exactly reversed.

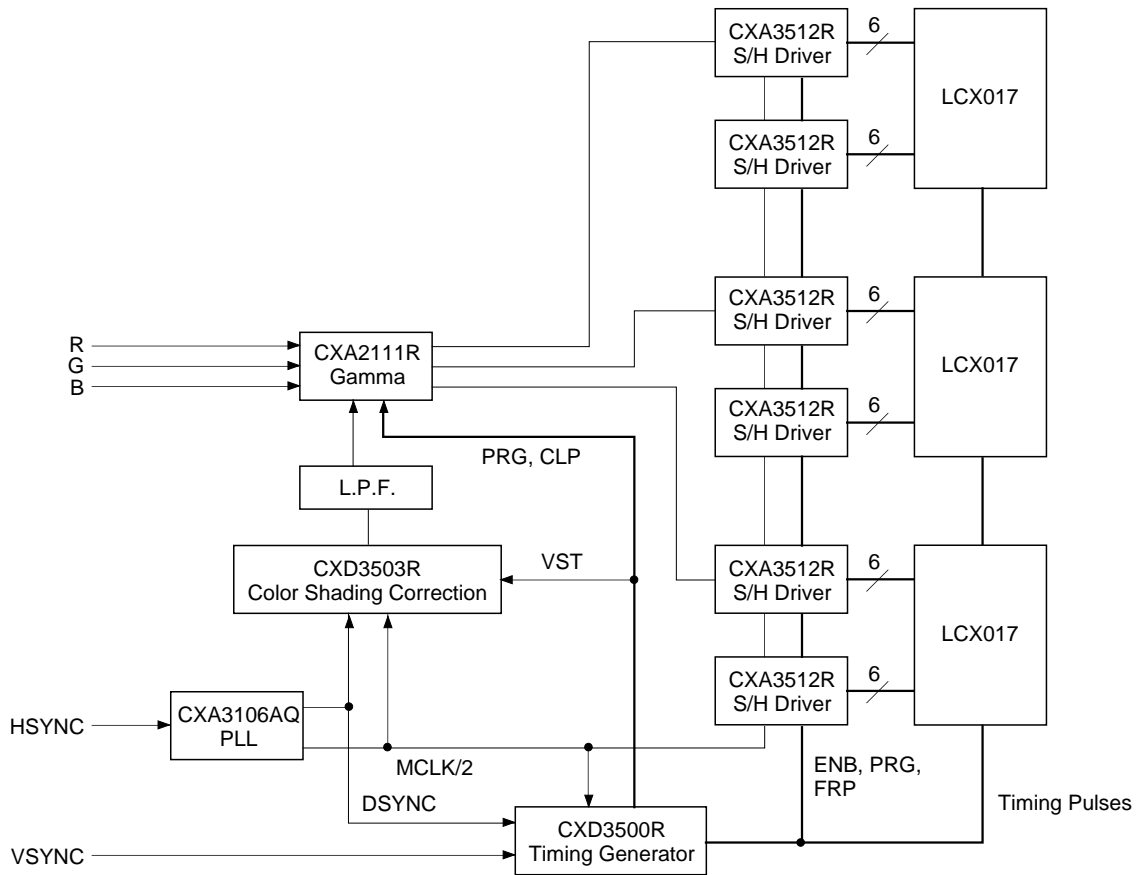


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

- a) Use non-chargeable gloves, or simply use bare hands.
- b) Use an earth-band when handling.
- c) Do not touch any electrodes of a panel.
- d) Wear non-chargeable clothes and conductive shoes.
- e) Install conductive mats on the working floor and working table.
- f) Keep panels away from any charged materials.
- g) Use ionized air to discharge the panels.

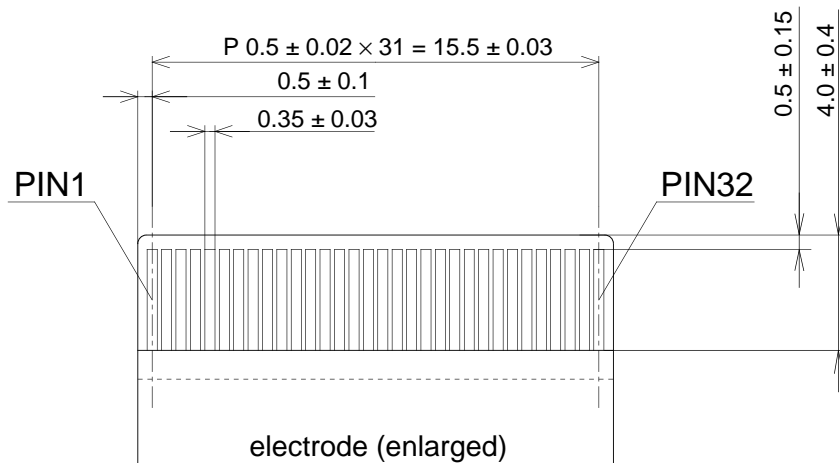
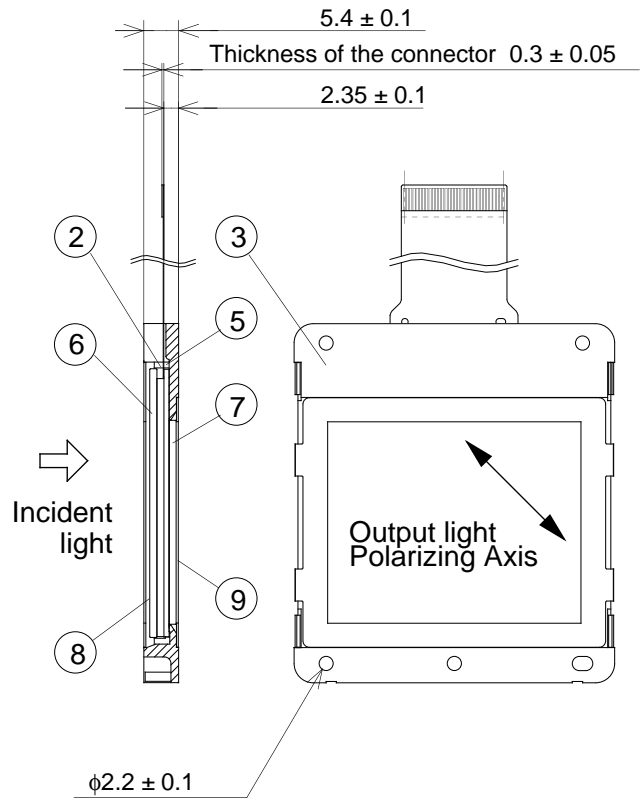
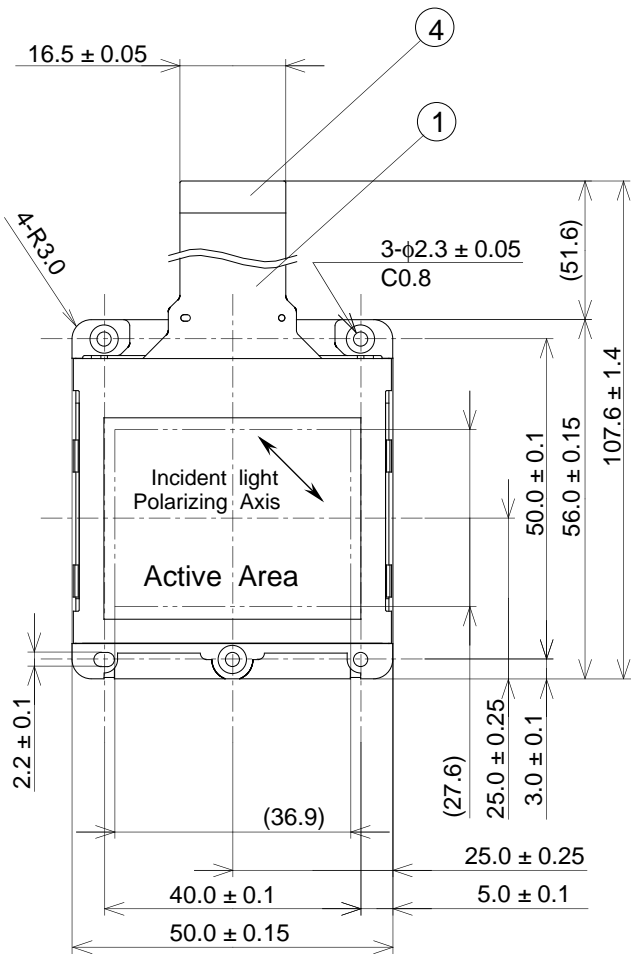
(2) Protection from dust and dirt

- a) Operate in a clean environment.
- b) When delivered, the panel surface (glass panel) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the glass panel.
- c) Do not touch the glass panel surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
- d) Use ionized air to blow dust off the glass panel.

(3) Other handling precautions

- a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
- b) Do not drop the panel.
- c) Do not twist or bend the panel or panel frame.
- d) Keep the panel away from heat sources.
- e) Do not dampen the panel with water or other solvents.
- f) Avoid storing or using the panel at a high temperature or high humidity, which may result in panel damages.
- g) Minimum radius of bending curvature for a flexible substrate must be 1mm.
- h) Torque required to tighten screws on a panel must be 0.294N · m or less.
- i) Use appropriate filter to protect a panel.
- j) Do not pressure the portion other than mounting hole (cover).

Package Outline Unit: mm



The rotation angle of the active area relative to H and V is $\pm 1^\circ$.

| No | Description |
|----|----------------------|
| 1 | F P C |
| 2 | Molding material |
| 3 | Outside frame |
| 4 | Reinforcing board |
| 5 | Reinforcing material |
| 6 | Glass 1 |
| 7 | Glass 2 |
| 8 | Cover 1 |
| 9 | Cover 2 |

Mass 25g