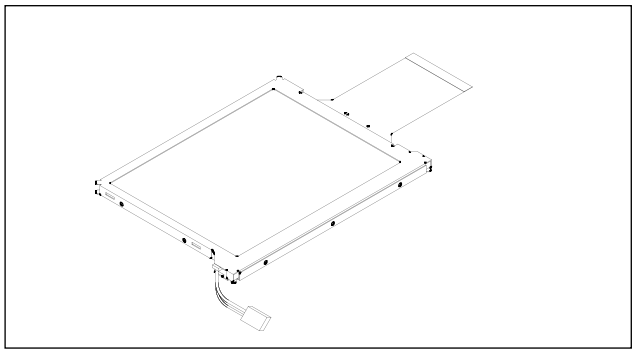
SONY

ACX704AKM

9.60cm (3.78 Type) QVGA Reflective Color LCD Module



Description

The ACX704AKM is a 9.60cm diagonal, QVGA formatted active matrix reflective color TFT-LCD with a high performance front light unit. This panel provides ultra-high reflectivity (30% typ.) with high contrast ratio (25:1 typ.). These characteristics are realized by a newly developed reflective electrode structure. In addition, this panel provides low power consumption (20mW typ.) which is realized by built-in 4-bit digital interface circuitry addressed by low temperature polycrystalline silicon transistors.

Features

- Number of dots: 320 × RGB × 240
- Dot size: 80µm × 240µm
- High reflectivity: 30% (typ.)
- High contrast ratio: 25:1 (typ.)
- Number of colors: 4096
- Low power consumption: 20mW (typ.)
- Built-in 4-bit digital interface circuitry
- Compact size
- Thin and bright front light unit

Element Structure

- Active matrix TFT-LCD panel with built-in peripheral driving circuitry using low temperature polycrystalline silicon transistors
- Number of dots
  - Total number of dots: 322 × 3 (H) × 242 (V) = 233,772
  - Number of active dots: 320 × 3 (H) × 240 (V) = 230,400
- Dimensions
  - Module dimensions: 96.8 (W) × 73.0 (D) × 3.96 (H) (mm)
  - Effective display dimensions: 76.800 (H) × 57.600 (V) (mm)

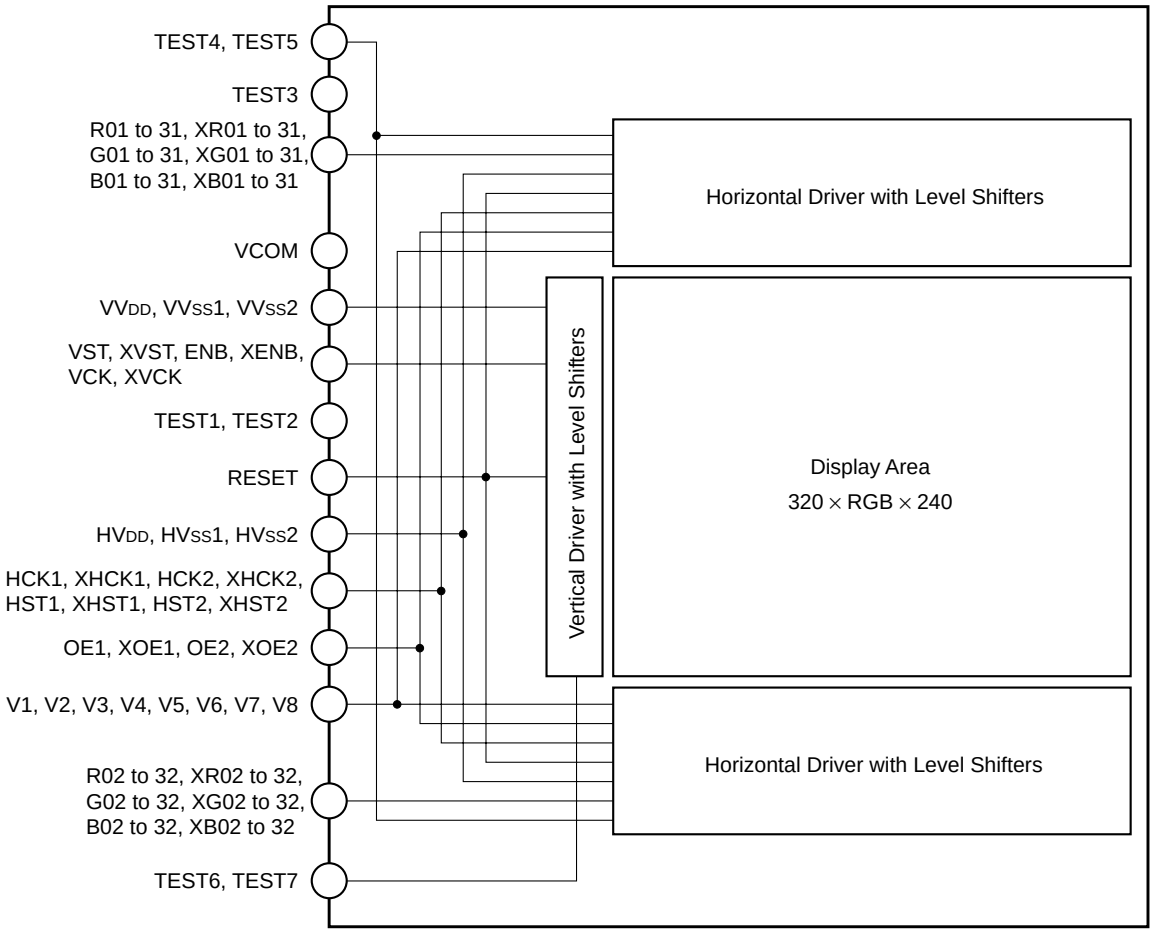
Applications

PDA, etc.

E00813

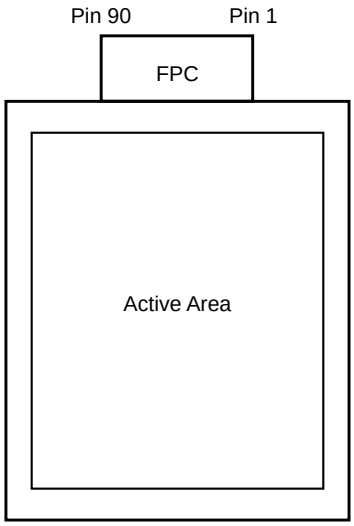
Block Diagram

The panel block diagram is shown below.



Pin Location of Panel Block

The FPC pin assignment is described in the page 4. The location of Pin 1 is shown below.



Front View

Absolute Maximum Ratings ($HV_{SS}1$, $VV_{SS}1$ = 0V)

• H driver supply voltage 1	HV_{DD}	–1.0 to +10.5	V
• V driver supply voltage 1	VV_{DD}	–1.0 to +10.5	V
• H driver supply voltage 2	$HV_{SS}2$	–7.5 to +1.0	V
• V driver supply voltage 2	$VV_{SS}2$	–7.5 to +1.0	V
• Power-on reset input pin voltage	RESET	–1.0 to +10.5	V
• Vcom input pin voltage	VCOM	–1.0 to +10.5	V
• Reference voltage input pin voltage	V0, V1, V2, V3, V4, V5, V6, V7, V8	–1.0 to +10.5	V
• H driver pulse input pin voltage	HST1, XHST1, HST2, XHST2, HCK1, XHCK1, HCK2, XHCK2, OE1, XOE1, OE2, XOE2, TEST4, TEST5	–1.0 to +10.5	V
• V driver pulse input pin voltage	VST, XVST, VCK, XVCK, ENB, XENB, TEST6, TEST7	–1.0 to +10.5	V
• Data signal input pin voltage	Rnm, XRnm, Gnm, XGnm, Bnm, XBnm (n = 0, 1, 2, 3, m = 1, 2)	–1.0 to +10.5	V
• Operating temperature	Topr	–10 to +40	°C
• Storage temperature	Tstg	–30 to +60	°C

Power Consumption

Less than 35mW (typ. 20mW) excluding the front light and supporting circuitry on the typical operating condition.

Pin Description of Panel Block

Pin No.	Symbol	Description	Comment	Pin No.	Symbol	Description	Comment
1	TEST4	Test input	Connected to 0V	36	VCK	Pulse input	
2	TEST5	Test input	Connected to 3.3V	37	XVCK	Pulse input	
3	TEST3	Test output	No connection	38	TEST1	Test output	No connection
4	R31	Data input		39	TEST2	Test output	No connection
5	R21	Data input		40	RESET	Power-on reset	Connected to R/C
6	R11	Data input		41	HV_{DD}	Power supply	
7	R01	Data input		42	$HV_{SS}1$	GND	
8	G31	Data input		43	$HV_{SS}2$	Power supply	
9	G21	Data input		44	HCK1	Pulse input	
10	G11	Data input		45	XHCK1	Pulse input	
11	G01	Data input		46	HCK2	Pulse input	
12	B31	Data input		47	XHCK2	Pulse input	
13	B21	Data input		48	HST1	Pulse input	
14	B11	Data input		49	XHST1	Pulse input	
15	B01	Data input		50	HST2	Pulse input	
16	XR31	Data input		51	XHST2	Pulse input	
17	XR21	Data input		52	OE1	Pulse input	
18	XR11	Data input		53	XOE1	Pulse input	
19	XR01	Data input		54	OE2	Pulse input	
20	XG31	Data input		55	XOE2	Pulse input	
21	XG21	Data input		56	V0	Reference voltage	
22	XG11	Data input		57	V1	Reference voltage	
23	XG01	Data input		58	V2	Reference voltage	
24	XB31	Data input		59	V3	Reference Voltage	
25	XB21	Data input		60	V4	Reference voltage	
26	XB11	Data input		61	V5	Reference voltage	
27	XB01	Data input		62	V6	Reference voltage	
28	VCOM	Common voltage		63	V7	Reference voltage	
29	VV_{DD}	Power supply		64	V8	Reference voltage	
30	$VV_{SS}1$	GND		65	XB02	Data input	
31	$VV_{SS}2$	Power supply		66	XB12	Data input	
32	VST	Pulse input		67	XB22	Data input	
33	XVST	Pulse input		68	XB32	Data input	
34	ENB	Pulse input		69	XG02	Data input	
35	XENB	Pulse input		70	XG12	Data input	

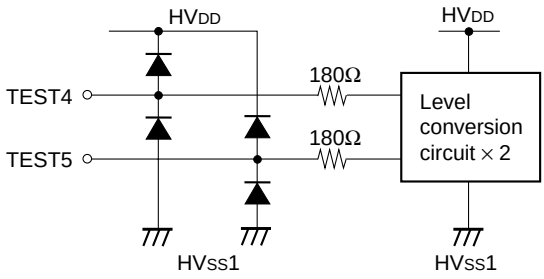
Pin No.	Symbol	Description	Comment
71	XG22	Data input	
72	XG32	Data input	
73	XR02	Data input	
74	XR12	Data input	
75	XR22	Data input	
76	XR32	Data input	
77	B02	Data input	
78	B12	Data input	
79	B22	Data input	
80	B32	Data input	
81	G02	Data input	
82	G12	Data input	
83	G22	Data input	
84	G32	Data input	
85	R02	Data input	
86	R12	Data input	
87	R22	Data input	
88	R32	Data input	
89	TEST6	Test input	Connected to 0V
90	TEST7	Test input	Connected to 3.3V

Input Equivalent Circuits of Panel Block

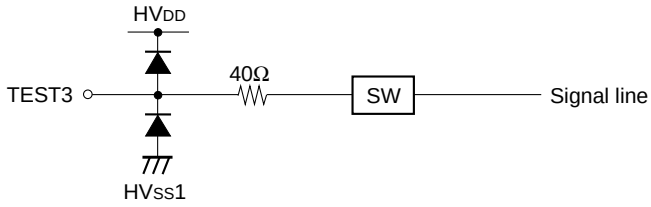
To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the reference input pins, data input pins, HCK1, XHCK1, HCK2 and XHCK2. Reference input pins and VCOM are connected to $HV_{SS}1$ with a high resistance of 2MΩ (typ.). The equivalent circuit of each pin is shown below.

(Resistor value: typ.)

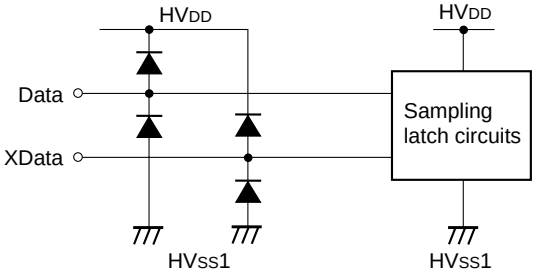
(1) TEST4, TEST5



(2) TEST3

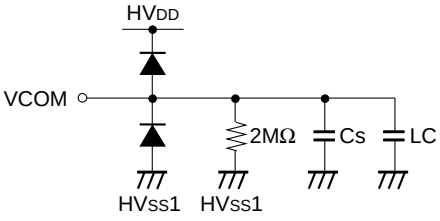


(3) Data, XData

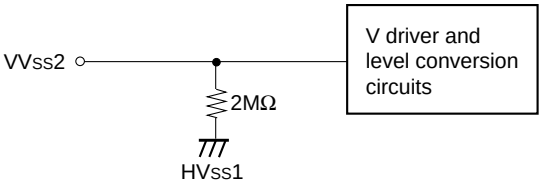


* Data means Rmn, Gmn, Bmn. (n = 0, 1, 2, 3, m = 1, 2)
XData means XRmn, XGmn, XBmn. (n = 0, 1, 2, 3, m = 1, 2)

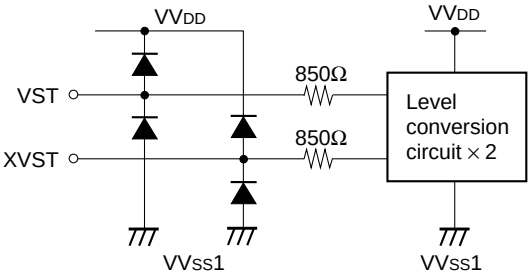
(4) VCOM



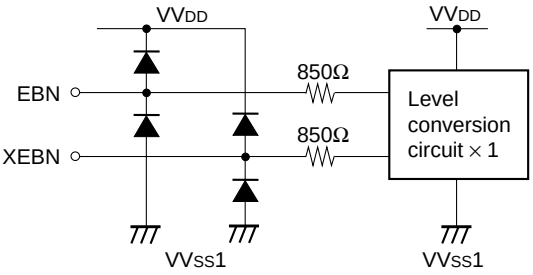
(5) $V_{VSS}2$



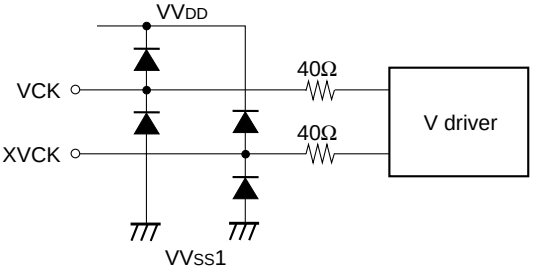
(6) VST, XVST



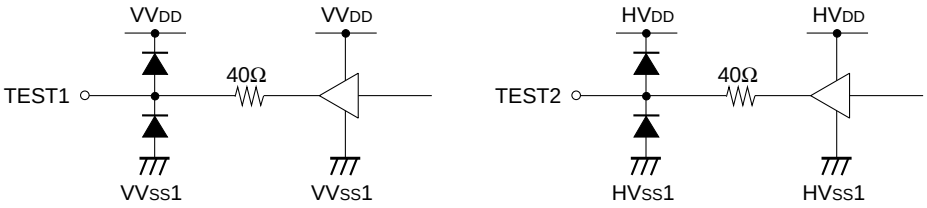
(7) ENB, XENB



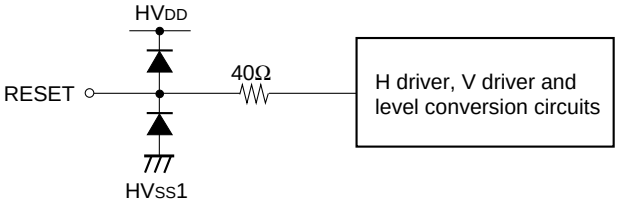
(8) VCK, XVCK



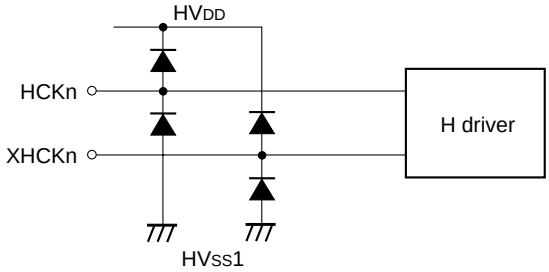
(9) TEST1, TEST2



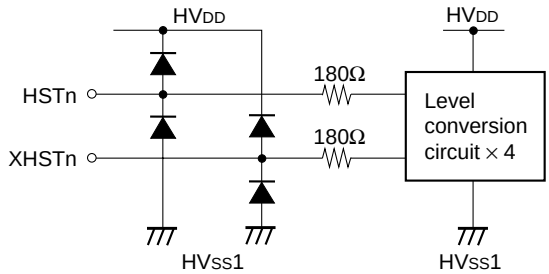
(10) RESET



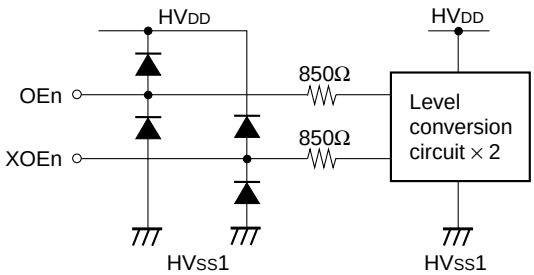
(11) HCKn, XHCKn (n = 1, 2)



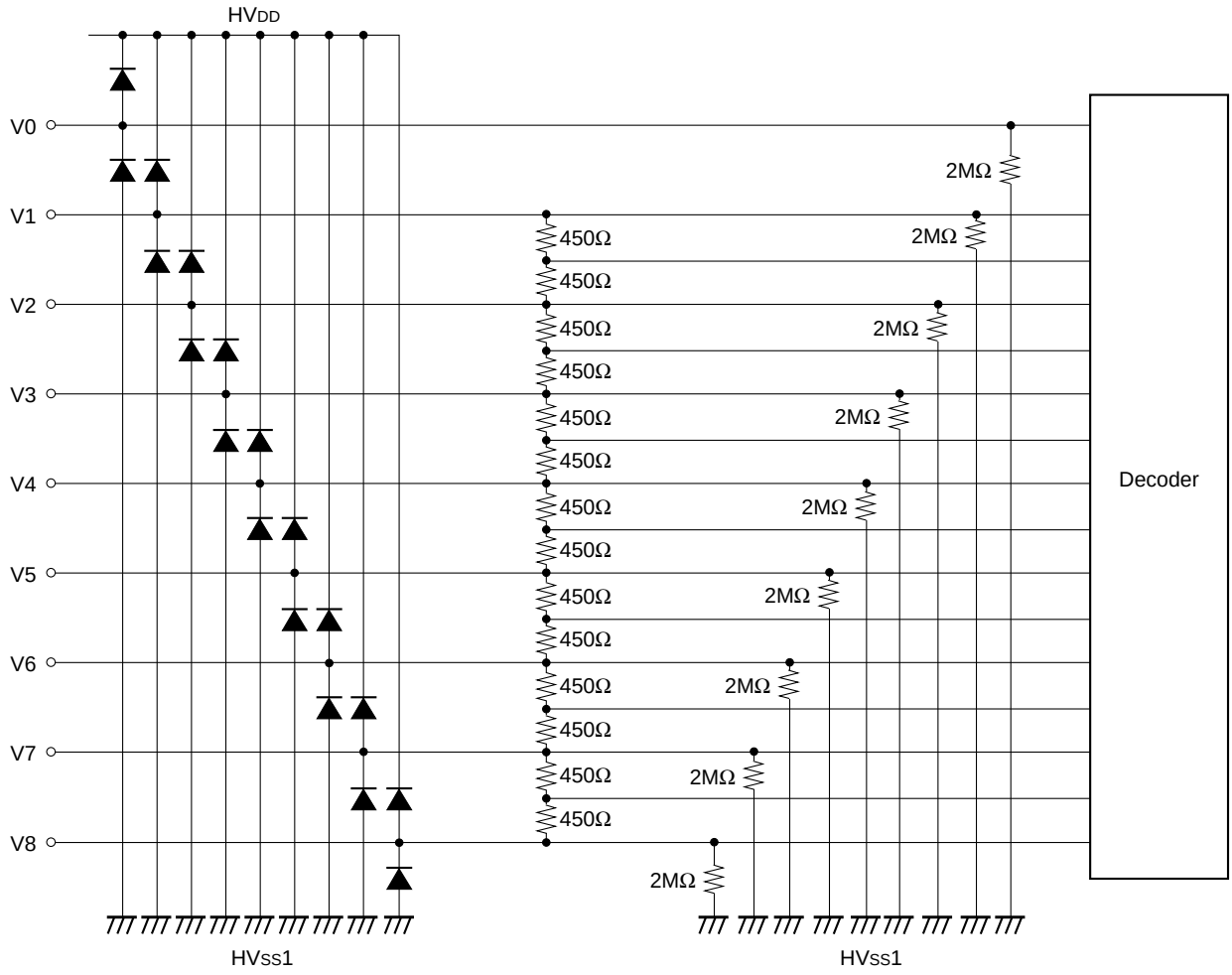
(12) HSTn, XHSTn (n = 1, 2)



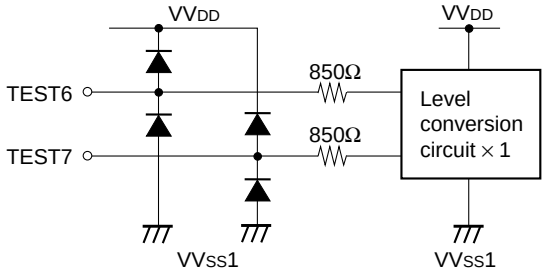
(13) OEn, XOEn (n = 1, 2)



(14) Reference voltage input V0-V8



(15) TEST6, TEST7

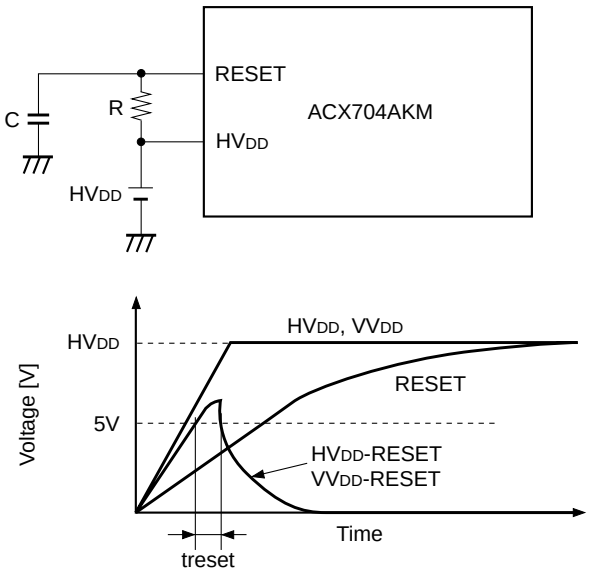


Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit	Pin/Remark
Supply voltage 1	HV_{DD}	8.5	9.0	9.5	V	HV_{DD}
Supply voltage 2	VV_{DD}	8.5	9.0	9.5	V	VV_{DD}
Supply voltage 3	$HV_{SS}2$	–7.0	–6.5	–6.0	V	$HV_{SS}2$
Supply voltage 4	$VV_{SS}2$	–7.0	–6.5	–6.0	V	$VV_{SS}2$
Reset voltage	Vreset	HV_{DD} – 0.1	HV_{DD}	HV_{DD} + 0.1	V	RESET, *1
Data/pulse input (Low)	V_{IL}	–0.3	0.0	0.3	V	*2
Data/pulse input (High)	V_{IH}	3.0	3.3	3.6	V	*2
Common voltage center	VcomC				V	VCOM, *3
Common voltage swing	VcomA		5.0		V	VCOM
Reference voltage 1	Vref1	0.0		5.0	V	V0, V1, V8
Reference voltage 2	Vref2	0.5		4.5	V	V2, V3, V4, V5, V6, V7
Vertical frequency	fv		60	65	Hz	
Horizontal frequency	fh		15.84	17.16	kHz	
Data frequency	fdot		2.79	3.02	MHz	
VCOM rise time	trvcom			12.5	µs	VCOM
VCOM fall time	tfvcom			12.5	µs	VCOM
V0-V8 rise time	trvn			12.5	µs	*4
V0-V8 fall time	tfvn			12.5	µs	*4
Data rise time	trdata			40	ns	*5
Data fall time	tfdata			40	ns	*5
HST rise time	trhst			30	ns	HST1, XHST1, HST2, XHST2
HST fall time	tfhst			30	ns	HST1, XHST1, HST2, XHST2
HCK rise time	trhck			30	ns	HCK1, XHCK1, HCK2, XHCK2
HCK fall time	tfhck			30	ns	HCK1, XHCK1, HCK2, XHCK2
OE1 pulse rise time	troe1			60	ns	OE1, XOE1
OE1 pulse fall time	tfoe1			60	ns	OE1, XOE1
OE2 pulse rise time	troe2			60	ns	OE2, XOE2
OE2 pulse fall time	tfoe2			60	ns	OE2, XOE2
VST pulse rise time	trvst			60	ns	VST, XVST
VST pulse fall time	tfvst			60	ns	VST, XVST
VCK pulse rise time	trvck			60	ns	VCK, XVCK
VCK pulse fall time	tfvck			60	ns	VCK, XVCK
ENB pulse rise time	trenb			80	ns	ENB, XENB
ENB pulse fall time	tfenb			80	ns	ENB, XENB
HCK duty	Dhck	48	50	52	%	*6
Cross point time lag	tdcross	–15	0	15	ns	*7
Data setup time 1	tstp1	35	50	120	ns	*8
Data setup time 2	tstp2	35	50	120	ns	*8

*1 Connect the resistor and capacitor to the RESET pin as shown in the figure below.

The external C and R value differs according to the rising time of the panel supply voltage.



Set a C value that satisfies treset > 1ms.

*2 This is applied to the following pins.
R31, R21, R11, R01, G31, G21, G11, G01, B31, B21, B11, B01, XR31, XR21, XR11, XR01, XG31, XG21, XG11, XG01, XB31, XB21, XB11, XB01,
R32, R22, R12, R02, G32, G22, G12, G02, B32, B22, B12, B02, XR32, XR22, XR12, XR02, XG32, XG22, XG12, XG02, XB32, XB22, XB12, XB02,
HST1, XHST1, HST2, XHST2, HCK1, XHCK1, HCK2, XHCK2, OE1, XOE1, OE2, XOE2,
VST, XVST, VCK, XVCK, ENB, XENB, TEST4, TEST5, TEST6, TEST7

*3 Common voltage center VcomC should be adjusted so as to minimize flicker or maximum contrast every each module.

*4 This is applied to the following pins.
V0, V1, V2, V3, V4, V5, V6, V7, V8

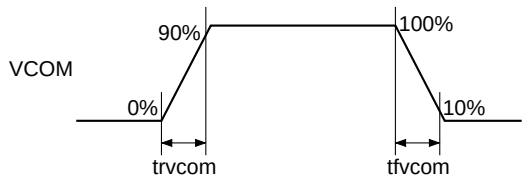
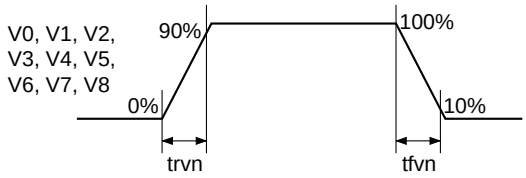
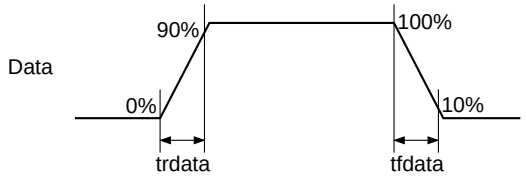
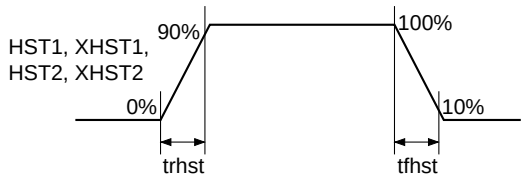
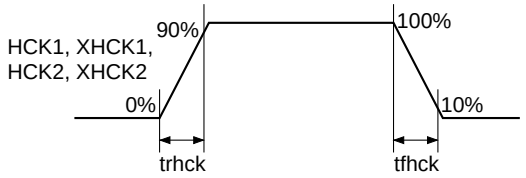
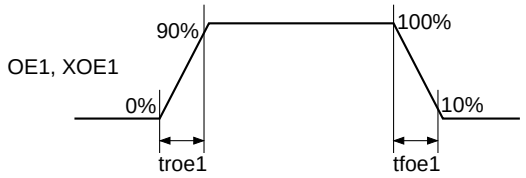
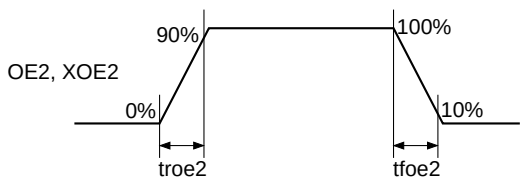
*5 This is applied to the following pins.
R31, R21, R11, R01, G31, G21, G11, G01, B31, B21, B11, B01, XR31, XR21, XR11, XR01, XG31, XG21, XG11, XG01, XB31, XB21, XB11, XB01,
R32, R22, R12, R02, G32, G22, G12, G02, B32, B22, B12, B02, XR32, XR22, XR12, XR02, XG32, XG22, XG12, XG02, XB32, XB22, XB12, XB02

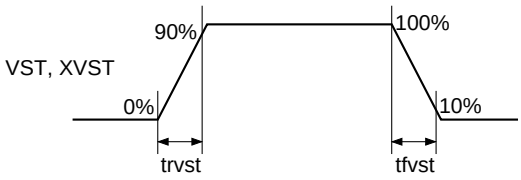
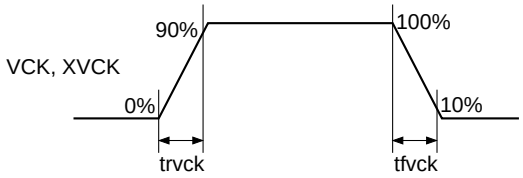
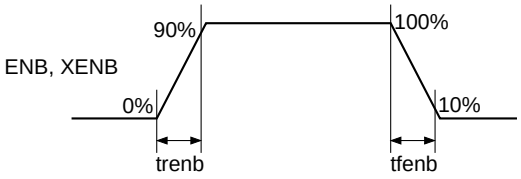
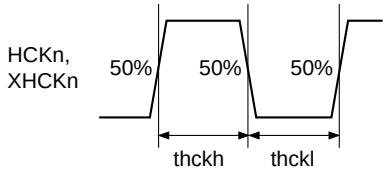
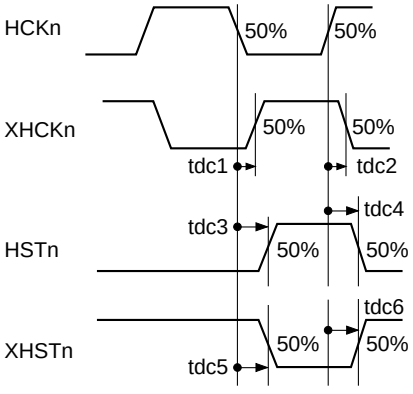
*6 This is applied to the following pins.
HCK1, XHCK1, HCK2, XHCK2

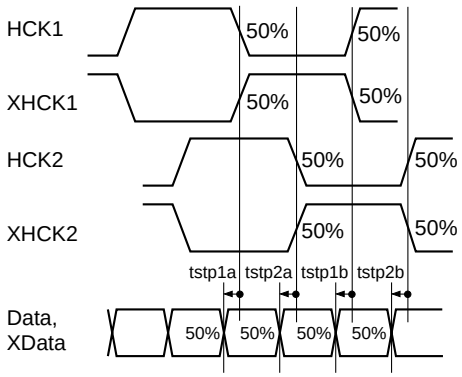
*7 This is applied to the following pins.
HST1, XHST1, HST2, XHST2, HCK1, XHCK1, HCK2, XHCK2

*8 This is applied to the following pins.
R31, R21, R11, R01, G31, G21, G11, G01, B31, B21, B11, B01, XR31, XR21, XR11, XR01, XG31, XG21, XG11, XG01, XB31, XB21, XB11, XB01,
R32, R22, R12, R02, G32, G22, G12, G02, B32, B22, B12, B02, XR32, XR22, XR12, XR02, XG32, XG22, XG12, XG02, XB32, XB22, XB12, XB02,
HCK1, XHCK1, HCK2, XHCK2

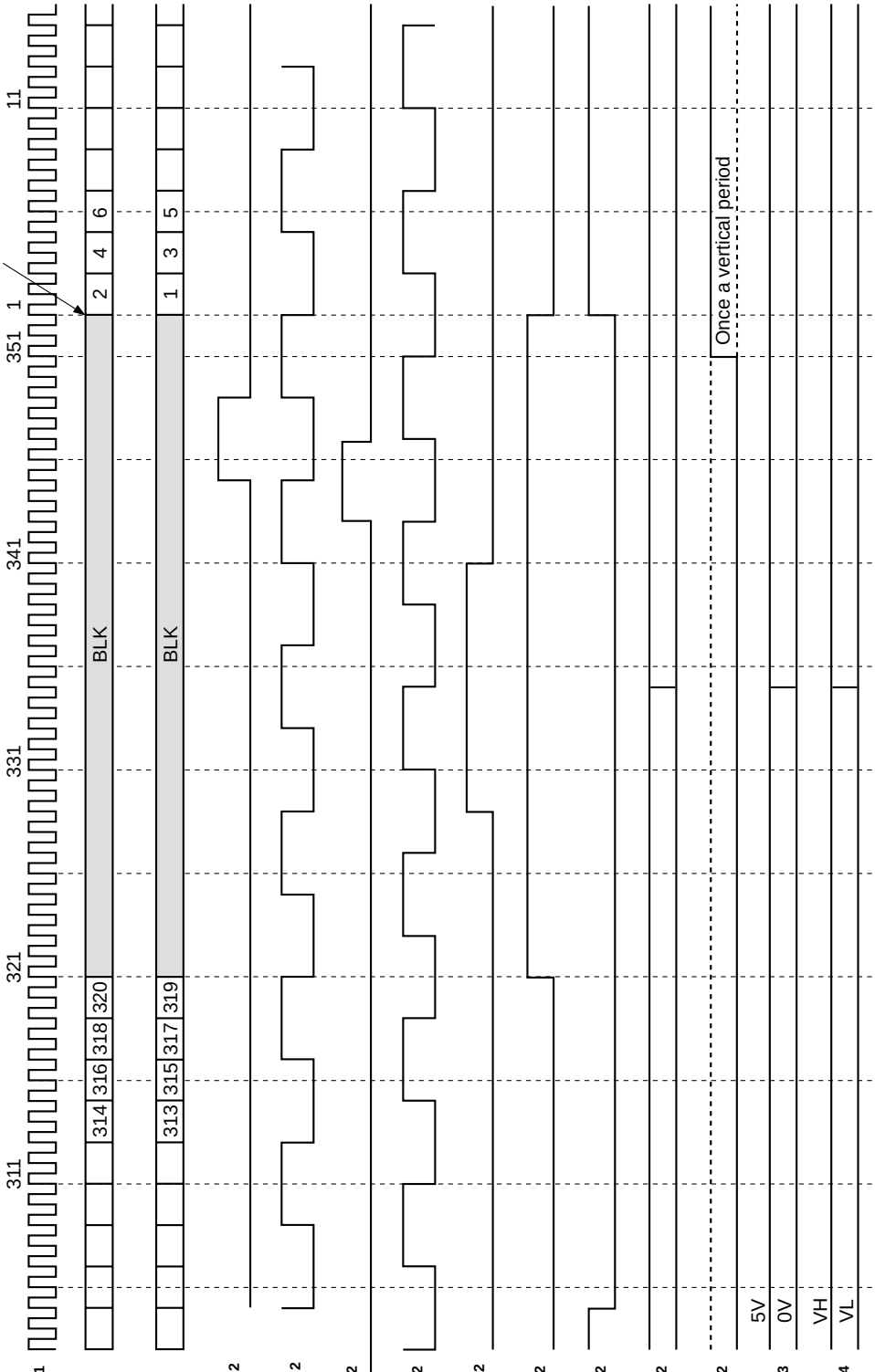
Input Waveforms

Item	Symbol	Waveform	Conditions
VCOM rise time	trvcom		
VCOM fall time	tfvcom		
V0-V8 rise time	trvn		
V0-V8 fall time	tfvn		
Data rise time	trdata		
Data fall time	tfdata		
HST rise time	trhst		
HST fall time	tfhst		
HCK rise time	trhck		
HCK fall time	tfhck		
OE1 pulse rise time	troe1		
OE1 pulse fall time	tfoe1		
OE2 pulse rise time	troe2		
OE2 pulse fall time	tfoe2		

Item	Symbol	Waveform	Conditions
VST pulse rise time	trvst		
VST pulse fall time	tfvst		
VCK pulse rise time	trvck		
VCK pulse fall time	tfvck		
ENB pulse rise time	trenb		
ENB pulse fall time	tfenb		
HCK duty	Dhck	 Dhck = thck/(thckh + thckl) × 100%	
Cross-point time lag	tdcross	 tdcross = Maximum (tdc1, tdc2, tdc3, tdc4, tdc5, tdc6)	

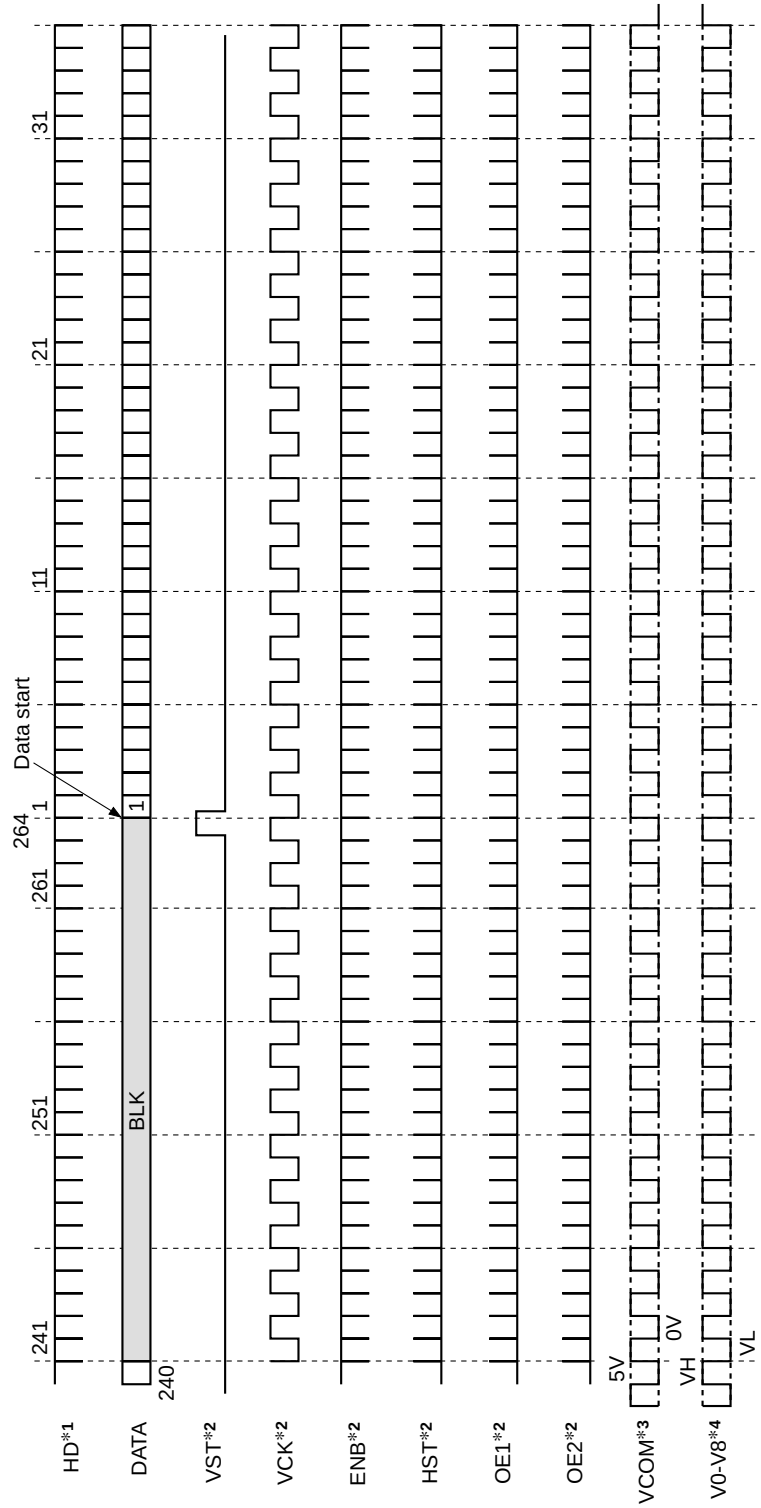
Item	Symbol	Waveform	Conditions
Data setup time 1	tstp1	 tstp1 = Maximum (tstp1a, tstp1b) tstp2 = Maximum (tstp2a, tstp2b)	
Data setup time 2	tstp2		

Horizontal Timing Chart



*1 This clock is not a signal for LCD panel.
*2 Inverted pulse is required for every data/pulse input except for VCOM, V0, V1, V2, V3, V4, V5, V6, V7 and V8.
*3 VCOM should be inverted every horizontal and every vertical cycle.
*4 V0-V8 should be inverted every horizontal and every vertical cycle.

Vertical Timing Chart



*1 This clock is not a signal for LCD panel.
*2 Inverted pulse is required for every data/pulse input except for VCOM, V0, V1, V2, V3, V4, V5, V6, V7 and V8.
*3 VCOM should be inverted every horizontal and every vertical cycle.
*4 V0-V8 should be inverted every horizontal and every vertical cycle.

Operating Condition of Front Light (Ta = 25°C)

Item	Symbol	Typ.	Unit	Conditions
Voltage	VL	335 ± 35	Vrms	25°C
Current	IL	1.4	mArms	25°C
Vstart	VS	520	Vrms	25°C
		780	Vrms	0°C
Frequency	F	60	kHz	25°C
Power Consumption	P	0.5	W	25°C

* These items shall depend on the used inverter.

Lamp Life

The lamp life shall be grater than 10,000 hours. The operating lamp life is defined as having ended when the illumination of light has reached 50% of the initial value.

Electrical Characteristics

HV_{DD} = VV_{DD} = 9V, $HV_{SS}1$ = $VV_{SS}1$ = 0V, $HV_{SS}2$ = $VV_{SS}2$ = –6.5V, V_{IH} = 3.3V, V_{IL} = 0V, Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Pin
HV_{DD} current consumption	I (HV_{DD})	—	1.6	2.6	mA	HV_{DD}
VV_{DD} current consumption	I (VV_{DD})	—	0.05	0.2	mA	VV_{DD}
$HV_{SS}2$ current consumption	I ($HV_{SS}2$)	—	0.7	1.4	mA	$HV_{SS}2$
$VV_{SS}2$ current consumption	I ($VV_{SS}2$)	—	0.01	0.1	mA	$VV_{SS}2$
HST input pin capacitance	Chst	—	70	100	pF	HST1, XHST1, HST2, XHST2
HCK input pin capacitance	Chck	—	120	150	pF	HCK1, XHCK1, HCK2, XHCK2
OE input pin capacitance	Coe	—	40	60	pF	OE1, XOE1, OE2, XOE2
Data input pin capacitance	Cdata	—	45	70	pF	*1
VCK input pin capacitance	Cvck	—	70	100	pF	VCK, XVCK
VST input pin capacitance	Cvst	—	55	85	pF	VST, XVST
EBN input pin capacitance	Cenb	—	45	70	pF	ENB, XENB
VCOM input pin capacitance	Cvcom	—	33	40	nF	VCOM
V0-V8 input pin capacitance	Cvn	—	25	40	nF	V0, V1, V2, V3, V4, V5, V6, V7, V8
HST input pin current	Ihst	–50	–10	—	µA	HST1, XHST1, HST2, XHST2
HCK input pin current	Ihck	–1000	–200	—	µA	HCK1, XHCK1, HCK2, XHCK2
OE input pin current	Ioe	–100	–20	—	µA	OE1, XOE1, OE2, XOE2
Data input pin current	Idata	–10	–2	—	µA	*1
VST input pin current	Ivst	–10	–2	—	µA	VCK, XVCK
VCK input pin current	Ivck	–25	–5	—	µA	VST, XVST
EBN input pin current	Ienb	–25	–5	—	µA	ENB, XENB

*1 This is applied to the following pins.
R31, R21, R11, R01, G31, G21, G11, G01, B31, B21, B11, B01, XR31, XR21, XR11, XR01, XG31, XG21, XG11, XG01, XB31, XB21, XB11, XB01,
R32, R22, R12, R02, G32, G22, G12, G02, B32, B22, B12, B02, XR32, XR22, XR12, XR02, XG32, XG22, XG12, XG02, XB32, XB22, XB12, XB02

Gray Scale Table

Color	Data input											
	R31	R21	R11	R01	G31	G21	G11	G01	B31	B21	B11	B01
	R32	R22	R12	R02	G32	G22	G12	G02	B32	B22	B12	B02
0 (Black)	L	L	L	L	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L	L	H	L	L
5	L	H	L	H	L	H	L	H	L	H	L	H
6	L	H	H	L	L	H	H	L	L	H	H	L
7	L	H	H	H	L	H	H	H	L	H	H	H
8	H	L	L	L	H	L	L	L	H	L	L	L
9	H	L	L	H	H	L	L	H	H	L	L	H
10	H	L	H	L	H	L	H	L	H	L	H	L
11	H	L	H	H	H	L	H	H	H	L	H	H
12	H	H	L	L	H	H	L	L	H	H	L	L
13	H	H	L	H	H	H	L	H	H	H	L	H
14	H	H	H	L	H	H	H	L	H	H	H	L
15 (White)	H	H	H	H	H	H	H	H	H	H	H	H

Color	Xdata input											
	XR31	XR21	XR11	XR01	XG31	XG21	XG11	XG01	XB31	XB21	XB11	XB01
	XR32	XR22	XR12	XR02	XG32	XG22	XG12	XG02	XB32	XB22	XB12	XB02
0 (Black)	H	H	H	H	H	H	H	H	H	H	H	H
1	H	H	H	L	H	H	H	L	H	H	H	L
2	H	H	L	H	H	H	L	H	H	H	L	H
3	H	H	L	L	H	H	L	L	H	H	L	L
4	H	L	H	H	H	L	H	H	H	L	H	H
5	H	L	H	L	H	L	H	L	H	L	H	L
6	H	L	L	H	H	L	L	H	H	L	L	H
7	H	L	L	L	H	L	L	L	H	L	L	L
8	L	H	H	H	L	H	H	H	L	H	H	H
9	L	H	H	L	L	H	H	L	L	H	H	L
10	L	H	L	H	L	H	L	H	L	H	L	H
11	L	H	L	L	L	H	L	L	L	H	L	L
12	L	L	H	H	L	L	H	H	L	L	H	H
13	L	L	H	L	L	L	H	L	L	L	H	L
14	L	L	L	H	L	L	L	H	L	L	L	H
15 (White)	L	L	L	L	L	L	L	L	L	L	L	L

Selected Reference Voltage Levels

A voltage level is selected by the combination of the data input. This relations are shown below.

Data input*1				Selected voltage level*2, *3
D3	D2	D1	D0	
L	L	L	L	V0
L	L	L	H	V1
L	L	H	L	(V1 + V2)/2
L	L	H	H	V2
L	H	L	L	(V2 + V3)/2
L	H	L	H	V3
L	H	H	L	(V3 + V4)/2
L	H	H	H	V4
H	L	L	L	(V4 + V5)/2
H	L	L	H	V5
H	L	H	L	(V5 + V6)/2
H	L	H	H	V6
H	H	L	L	(V6 + V7)/2
H	H	L	H	V7
H	H	H	L	(V7 + V8)/2
H	H	H	H	V8

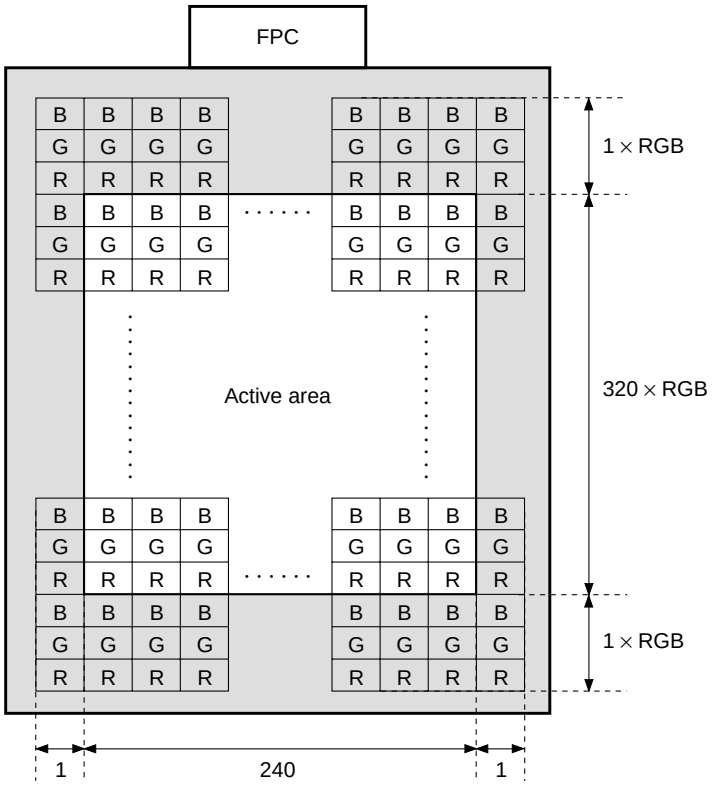
*1 Data input: D3 means R3m, G3m, B3m (m = 1, 2).
D2 means R2m, G2m, B2m (m = 1, 2).
D1 means R1m, G1m, B1m (m = 1, 2).
D0 means R0m, G0m, B0m (m = 1, 2).

*2 Selected voltage input: This voltage is applied to display area.
See the following page regarding VR characteristics.

*3 V0-V8: Reference voltage inputs

Color Coding

The color filters are coded in vertical stripe arrangement. The shaded area is used for the dark border around the display.

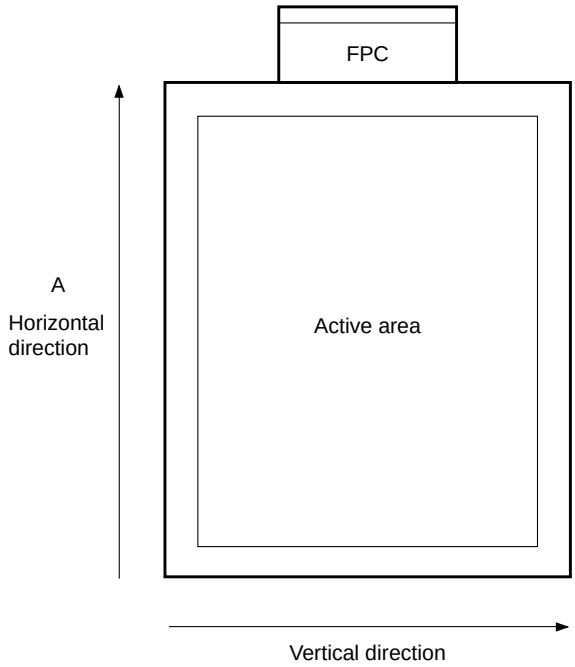


Front view

Scanning Direction

The scanning direction for the horizontal period and for the vertical period are A and B respectively as shown below.

These scanning directions are from a front view.



Front view

Color Combination Table

Color	Data input											
	R31	R21	R11	R01	G31	G21	G11	G01	B31	B21	B11	B01
	R32	R22	R12	R02	G32	G22	G12	G02	B32	B22	B12	B02
Black	L	L	L	L	L	L	L	L	L	L	L	L
Blue	L	L	L	L	L	L	L	L	H	H	H	H
Green	L	L	L	L	H	H	H	H	L	L	L	L
Cyan	L	L	L	L	H	H	H	H	H	H	H	H
Red	H	H	H	H	L	L	L	L	L	L	L	L
Magenta	H	H	H	H	L	L	L	L	H	H	H	H
Yellow	H	H	H	H	H	H	H	H	L	L	L	L
White	H	H	H	H	H	H	H	H	H	H	H	H

Color	Xdata input											
	XR31	XR21	XR11	XR01	XG31	XG21	XG11	XG01	XB31	XB21	XB11	XB01
	XR32	XR22	XR12	XR02	XG32	XG22	XG12	XG02	XB32	XB22	XB12	XB02
Black	H	H	H	H	H	H	H	H	H	H	H	H
Blue	H	H	H	H	H	H	H	H	L	L	L	L
Green	H	H	H	H	L	L	L	L	H	H	H	H
Cyan	H	H	H	H	L	L	L	L	L	L	L	L
Red	L	L	L	L	H	H	H	H	H	H	H	H
Magenta	L	L	L	L	H	H	H	H	L	L	L	L
Yellow	L	L	L	L	L	L	L	L	H	H	H	H
White	L	L	L	L	L	L	L	L	L	L	L	L

Electro-optical Characteristics

Ta = 25°C, with front light turning off

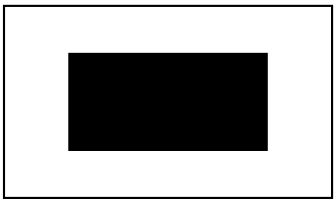
Item		Symbol	Min.	Typ.	Max.	Unit	Notes
Reflectivity		R	25	30	—	%	1
Contrast ratio		CR	19:1	25:1	—		2
White chromaticity	x	xfloff	0.29	0.32	0.34	CIE	3
	y	yfloff	0.32	0.34	0.36	CIE	
Response time	on	Ton	—	15	30	ms	4
	off	Toff	—	20	30	ms	
Viewing angle	Top-Bottom	VAtb	90°	100°	—	deg (°)	5
	Left-Right	VAlr	100°	120°	—	deg (°)	
V-R characteristic	V_{10}	V_{10}	1.2	1.5	1.8	V	6
	V_{50}	V_{50}	1.8	2.1	2.4	V	
	V_{90}	V_{90}	2.5	2.8	3.1	V	

Ta = 25°C, with front light turning on

Item		Symbol	Min.	Typ.	Max.	Unit	Notes
Luminance		Lcfl	19	26	—	cd/m^2	7
Luminance uniformity		Flunif	—	1.3	1.6	—	8
Contrast ratio		CRfl	6	8	—	—	9
White chromaticity	x	xflon	0.26	0.287	0.313	CIE	10
	y	yflon	0.276	0.301	0.326	CIE	

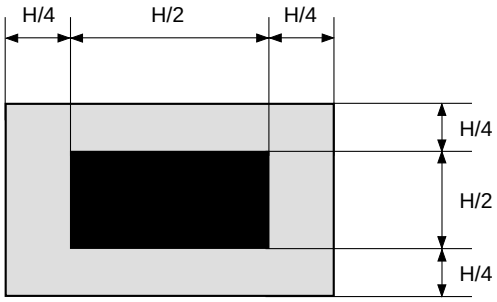
Image Persistence

Display a completely white screen for 20 minutes then continuously display the test pattern shown below for a minimum of two-hours. Then display a completely white screen. A visible image of the box pattern shall not persist more than two seconds viewed through 2% ND filter. Pattern is black box 80 pixels wide and 160 pixels in length at minimum luminance, centered horizontally and vertically in the active area. The reminder of the screen is white.



Cross Modulation

Cross modulation (cross talk) shall be inspected with following test pattern with 2% ND filter. Pattern is black box 80 pixels wide and 160 pixels in length at minimum luminance, centered horizontally and vertically in the active area. The reminder is of the screen is 50% gray.



There shall be no visible difference of luminance around the black box through 2% ND filter.

Notes:

1. Reflectivity (R)
   In the system-1 (see Fig. 1 (a), (b)), calculate the reflectance factor by using the formula (1).

   $$R = R\,(White) = \frac{\text{Output from the "White" displayed panel}}{\text{Output from the reflectance standard}} \times \text{reflectance factor of the reflectance standard} \quad \ldots(1)$$

2. Contrast Ratio (CR)
   In the system-1 (see Fig. 1(a), (b)), measure the reflectance factor of "White" and "Black" respectively and calculate by using the formula (2).

   $$CR = \frac{R\,(White)}{R\,(Black)} \quad \ldots(2)$$

3. White Chromaticity (xfloff, yfloff)
   In the system-2 (see Fig. 2), measure the white chromaticity. The illumination source and viewing area are D65 and 2° respectively.

4. Response Time (Ton, Toff)
   In the system-3 (see Fig. 3), measure the electro-optical response time.

5. Viewing Angle (VAtb, VAlr)
   In the measurement system-1 (see Fig. 1 (c)), viewing area is defined by the area which makes the CR ≥ 2.

6. V-R Characteristic (V_{90}, V_{50}, V_{10})
   In the system-1 (see Fig.1 (a), (b)), measure the signal amplitude across the liquid crystal where R (relative) = 90% and R (relative) = 50% and R (relative) = 10% (see Fig. 4).

7. Luminance (Lcfl)
   In the measurement system-4 (see Fig. 5), measure the luminance and calculate by using the formula (3).

   Lcfl = (Luminance (1) + Luminance (3) + Luminance (5) + Luminance (7) + Luminance (9)) / 5 …(3)

8. Luminance Uniformity (Flunif)
   In the measurement system-4 (see Fig. 5), measure the luminance and calculate by using the formula (4).

   Flunif = Luminance (maximum spot) / Luminance (minimum spot) …(4)

9. Contrast Ratio (CRfl)
   In the measurement system-4 (see Fig. 5(a)), measure the luminance of “White” and “Black” respectively and calculate by using the formula (5).

   $$CRfl = \frac{\text{Luminance (White)}}{\text{Luminance (Black)}} \quad \ldots(5)$$

10. White Chromaticity (xflon, yflon)
    In the system-4 (see Fig. 5(a)), measure the white chromaticity.

Basic Measurement Condition

(1) Driving voltage
    typical condition
(2) Measurement temperature
    +25°C unless otherwise specified.
(3) Measurement point
    One point on the center of the panel unless otherwise specified.
(4) Light source and viewing area
    D65 and 2°
(5) Display "White": All R, G and B signal data are high (signal amplitude across the liquid crystal: ±0.5V).
    Display "Black": All R, G and B signal data are low (signal amplitude across the liquid crystal: ±4.8V).

Front light is turned off unless otherwise specified.

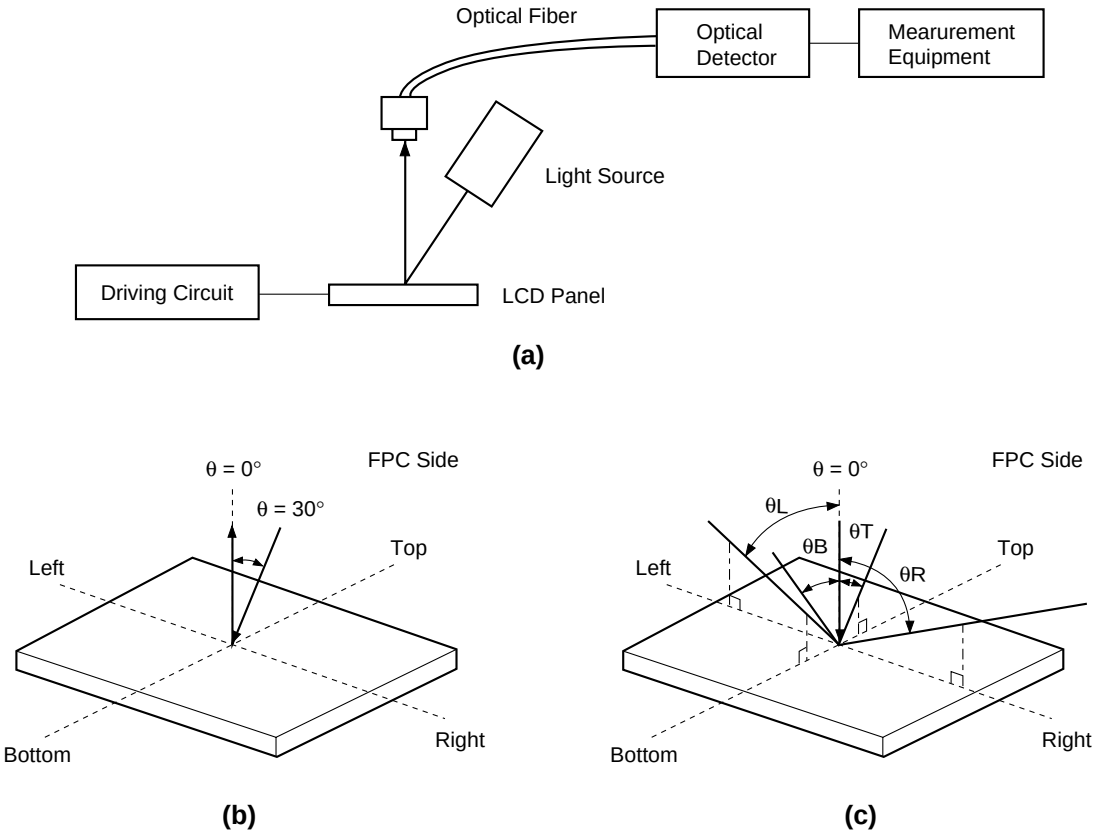


Fig. 1. Measurement System-1

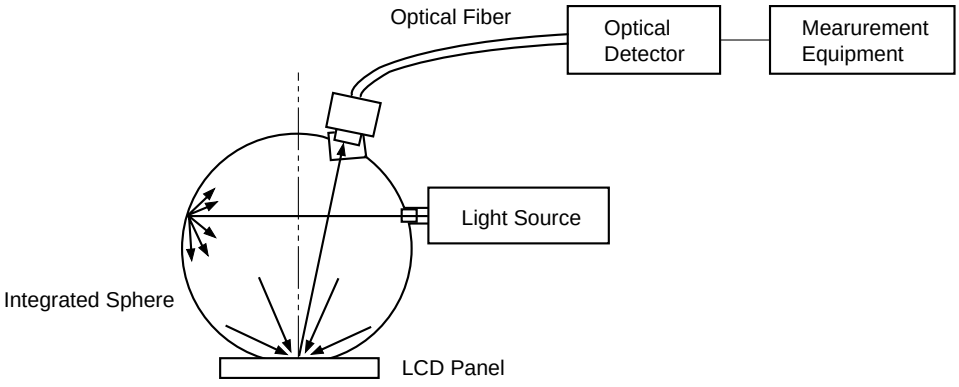


Fig. 2. Measurement System-2

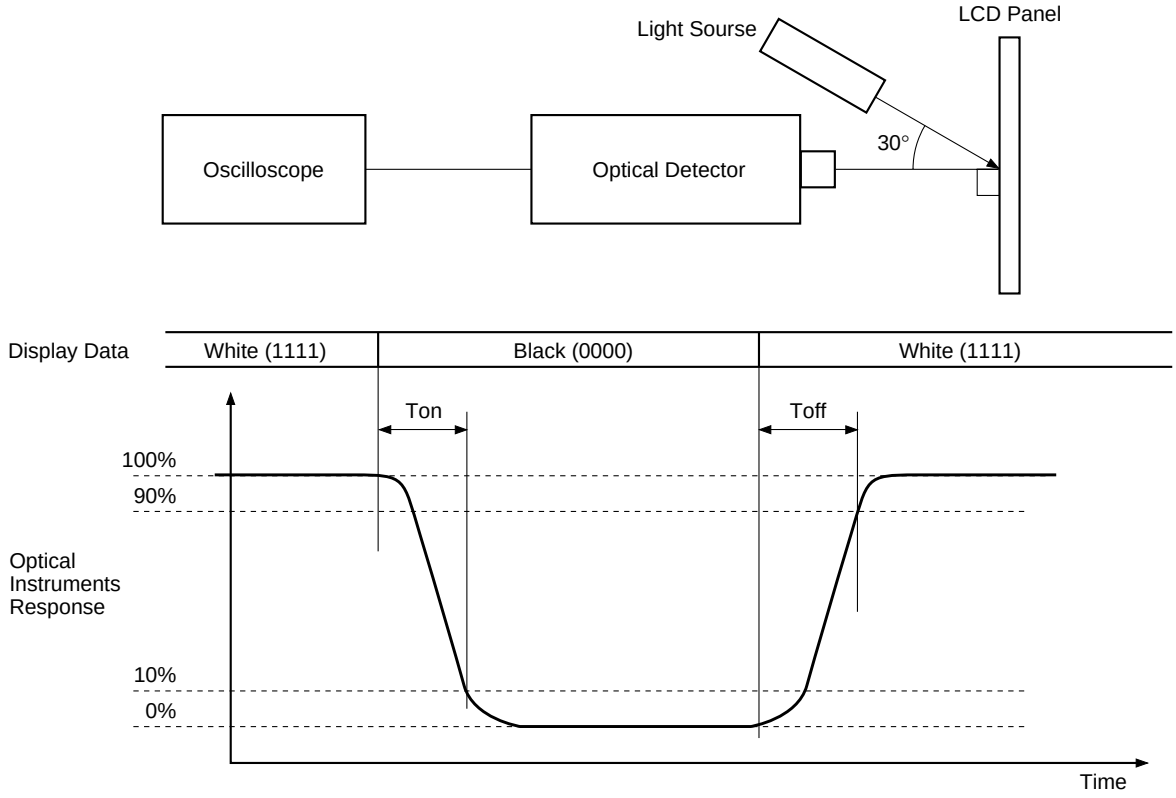
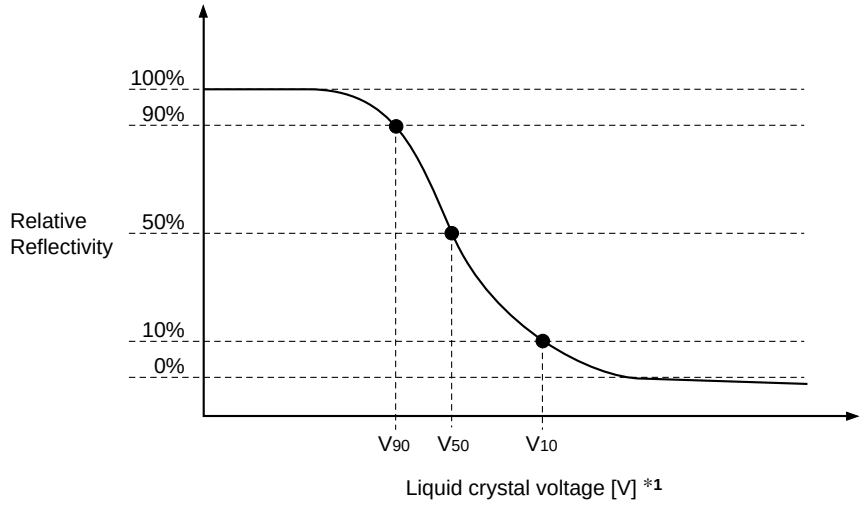
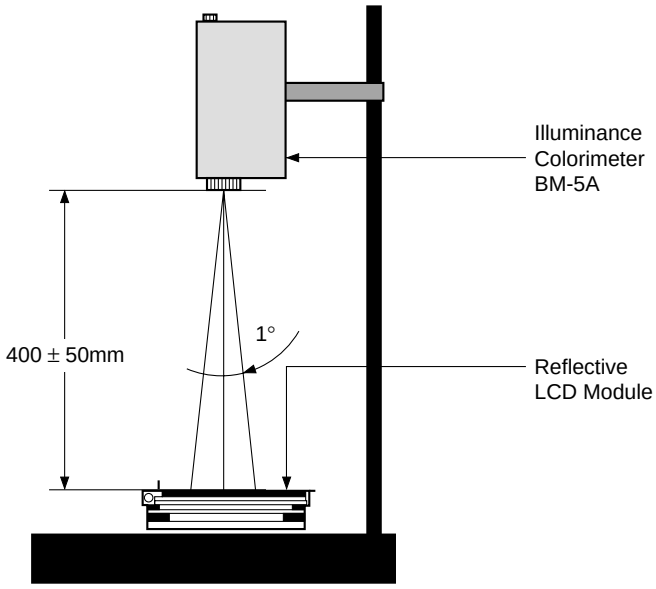


Fig. 3. Measurement System-3

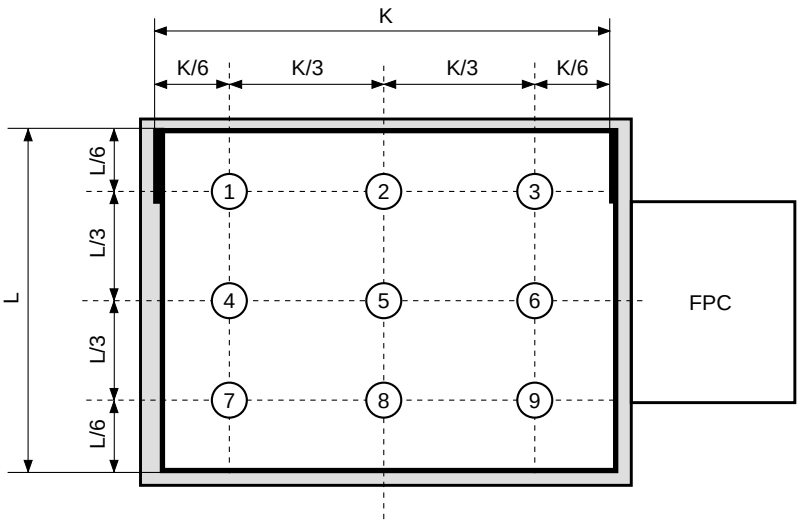


*1 Liquid crystal voltage = | Selected voltage level – Common voltage + Reference voltage center – Common voltage center |
See page 20 for "Selected Reference Voltage Levels".

Fig. 4. V-R Characteristics



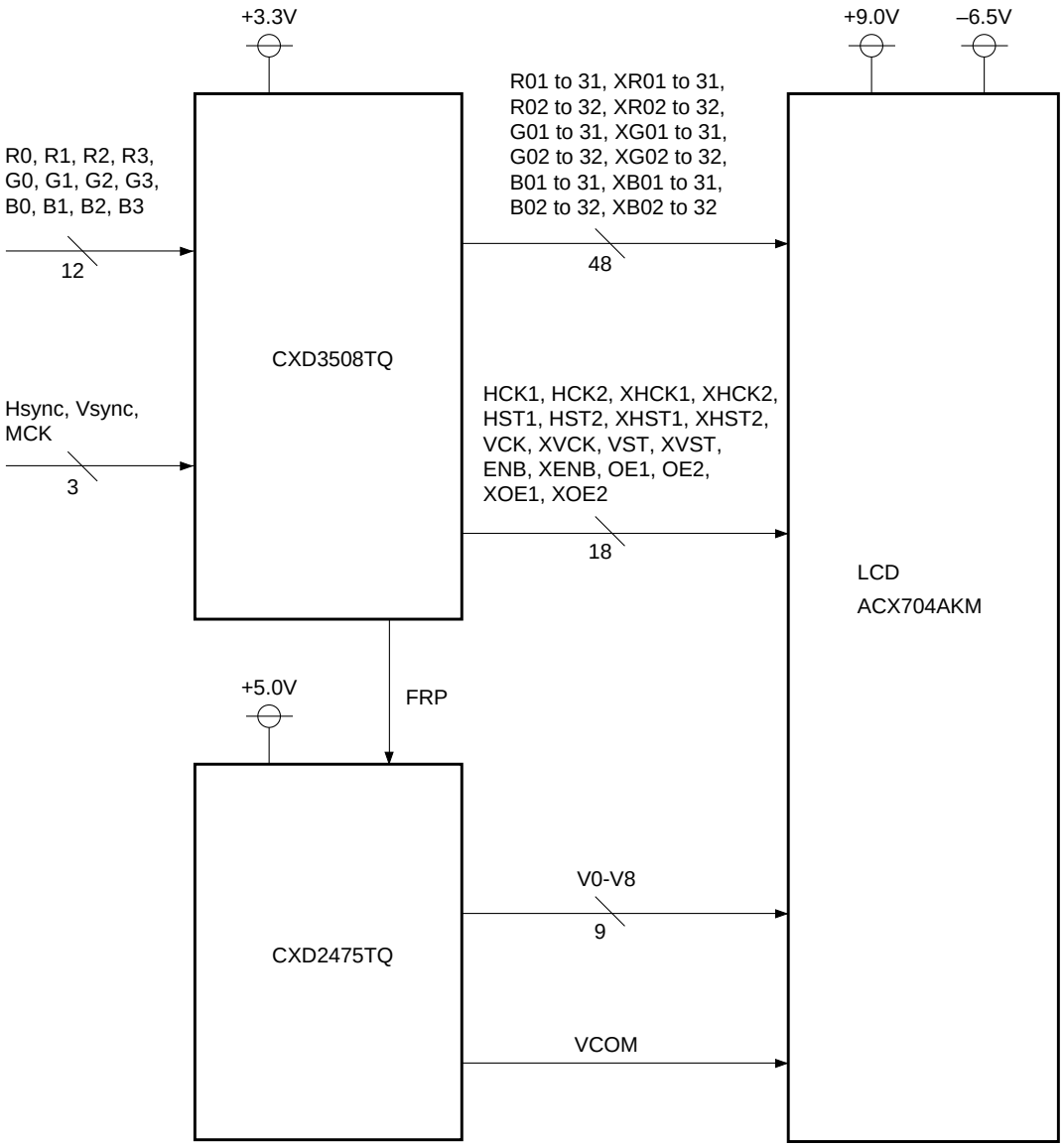
(a) The apparatus for luminance measurement



(b) The spot locations for luminance measurement

Fig. 5. Measurement System-4

System Configuration



Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install grounded conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

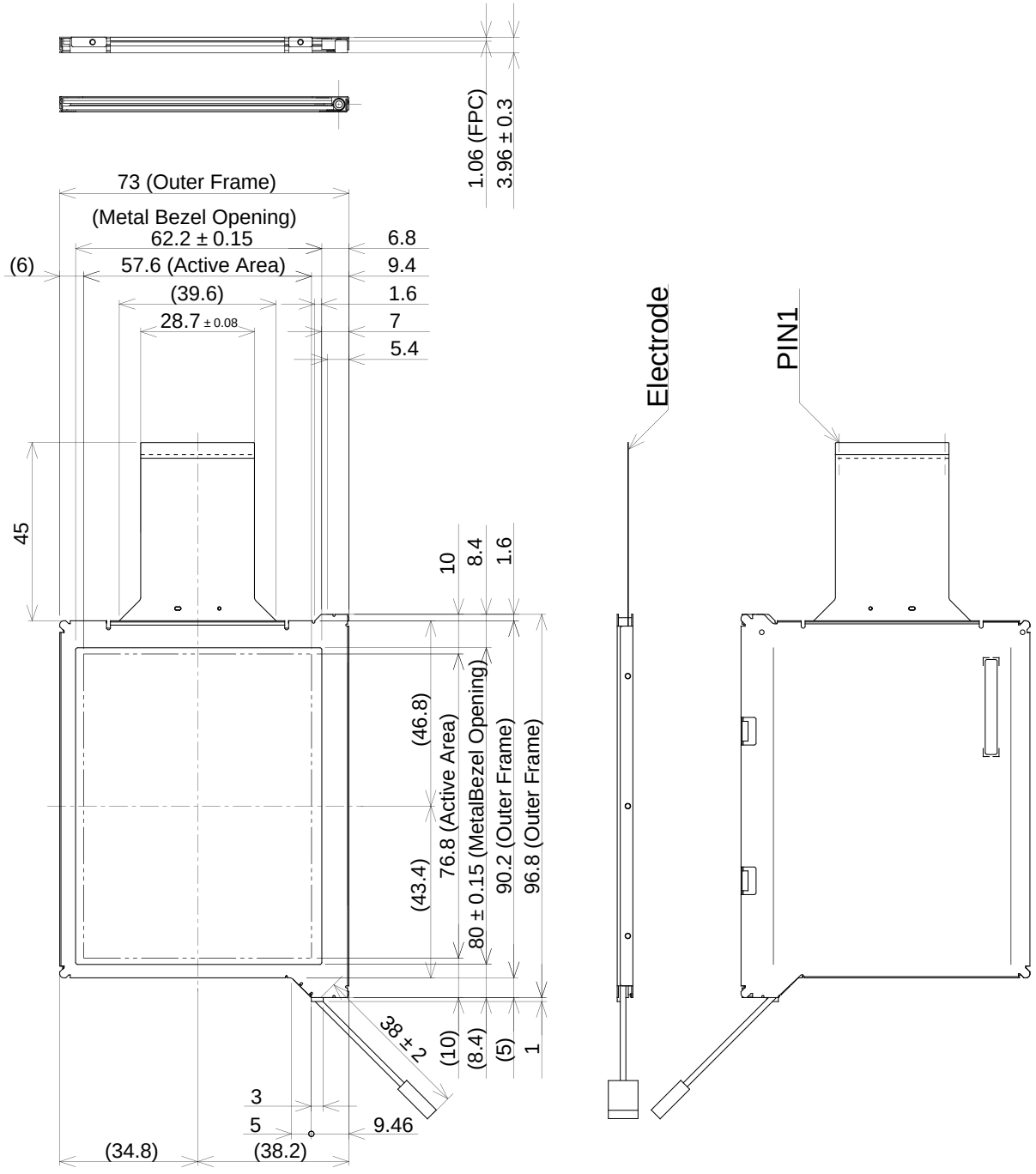
(2) Protection from dust and dirt

a) Operate in a clean environment.
b) Do not touch the front light surface. The surface is easily scratched.
c) Use ionized air to blow dust off the panel.

(3) Others

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the module.
c) Do not twist or bend the module.
d) Keep the module away from heat sources.
e) Do not dampen the module with water or other solvents.
f) Avoid storage or use the module at high temperatures or high humidity, as this may result in damage.

Package Outline Unit: mm



5)Mass:56g
4)FPC-connector:FF02(JAE)
3)CCFL-connector:BHSR-02VS-1(JST)
2)The rotation angle of the active area relative to H and V is ± 1°.
Note 1)Tolerance with no indication(± 0.2)