SONY

CXD3607R

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD3607R is a timing generator IC which generates the timing pulses required by Progressive Scan CCD image sensors as well as signal processing circuits.

Features

- Base oscillation frequency 57.3MHz
- High-speed/low-speed shutter function
- Supports FINE and DRAFT mode drive (15 frames/s, 60 frames/s possible)
- Random trigger shutter function (Supports TRIG and TRIGOUT mode drive)
- Horizontal driver for CCD image sensor
- Vertical driver for CCD image sensor

Applications

Progressive scan CCD cameras

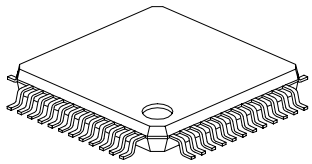
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX285 (Type 2/3, 1450K pixels)

48 pin LQFP (Plastic)



Absolute Maximum Ratings

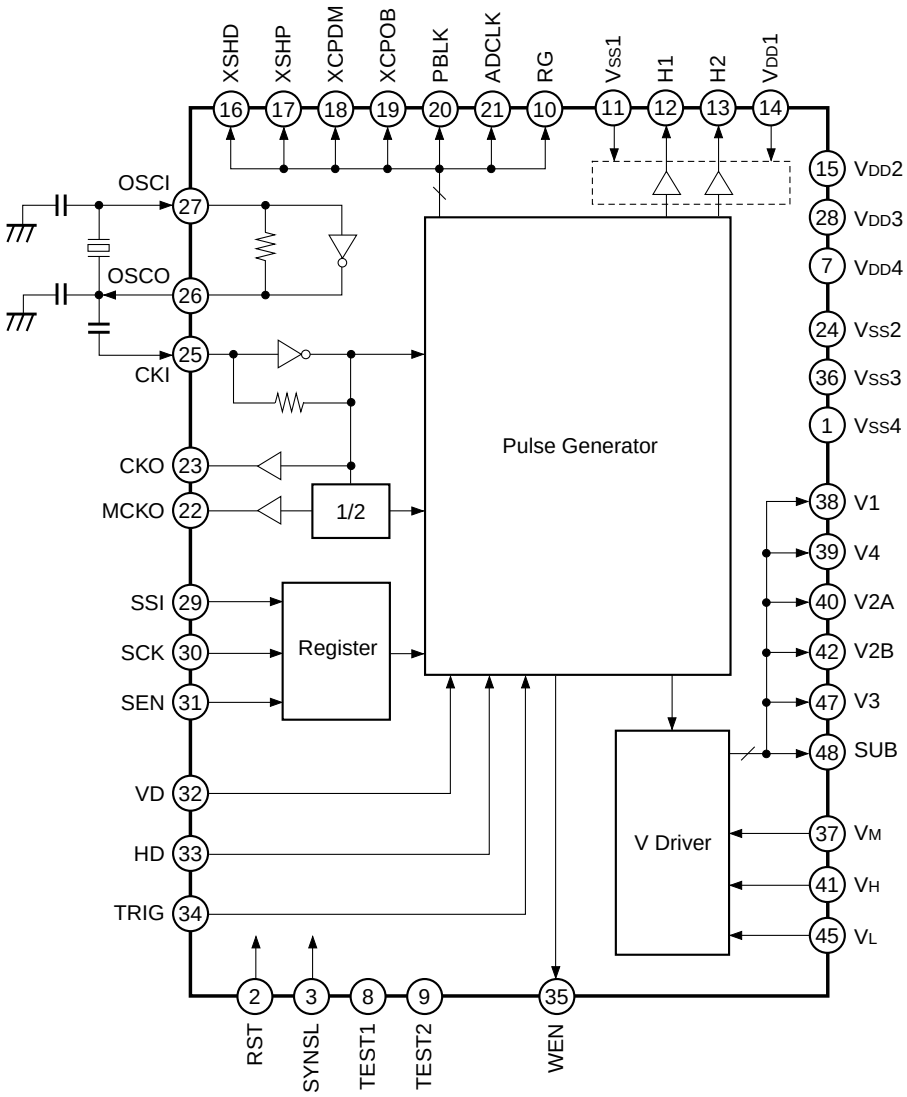
• Supply voltage	$V_{DD}a$, b	Vss – 0.3 to +7.0	V
	V_L	–10.0 to Vss	V
	V_H	V_L – 0.3 to +26.0	V
• Input voltage	V_I	Vss – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_{O1}	Vss – 0.3 to V_{DD} + 0.3	V
	V_{O2}	V_L – 0.3 to Vss + 0.3	V
	V_{O3}	V_L – 0.3 to V_H + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

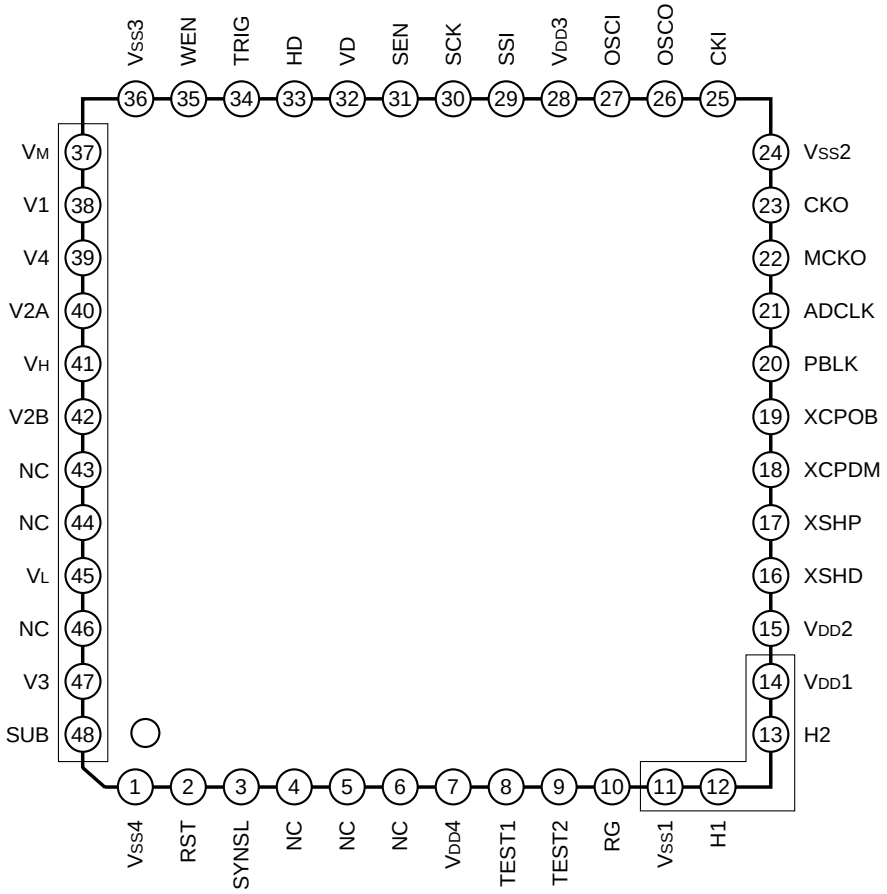
• Supply voltage	$V_{DD}a$	4.75 to 5.25	V
	$V_{DD}b$	3.0 to 3.6	V
	V_M	0.0	V
	V_H	14.55 to 15.45	V
	V_L	–7.5 to –6.5	V
• Operating temperature			
	Topr	–20 to +75	°C

E01318-PS

Block Diagram



Pin Configuration (Top View)



* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{SS}4$	—	GND (GND for common logic block)
2	RST	I	Internal system reset input. (High: Normal operation, Low: Reset operation) Normally apply reset during power-on.
3	SYNSL	I	Control input used to switch sync system. (High: CKI sync, Low: MCKO sync) With pull-down resistor
4	NC	—	(Leave open.)
5	NC	—	(Leave open.)
6	NC	—	(Leave open.)
7	$V_{DD}4$	—	3.3V power supply. (Power supply for common logic block)
8	TEST1	I	IC test pin 1 (Normally fix to GND.)
9	TEST2	I	IC test pin 2 (Normally fix to GND.) With pull-down resistor
10	RG	O	CCD reset gate pulse output.
11	$V_{SS}1$	—	GND (GND for H1 and H2 pins)
12	H1	O	Horizontal CCD drive clock output.
13	H2	O	Horizontal CCD drive clock output.
14	$V_{DD}1$	—	5.0V power supply. (Power supply for H1 and H2 pins)
15	$V_{DD}2$	—	3.3V power supply. (Power supply for common logic block)
16	XSHD	O	CCD data level sample-and-hold pulse output.
17	XSHP	O	CCD precharge level sample-and-hold pulse output.
18	XCPDM	O	CCD dummy signal clamp pulse output.
19	XCPOB	O	CCD optical black signal clamp pulse output.
20	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning.
21	ADCLK	O	Clock output for analog/digital conversion IC.
22	MCKO	O	System clock output for signal processing IC. (28.6MHz)
23	CKO	O	Inverter output. (57.3MHz)
24	$V_{SS}2$	—	GND (GND for common logic block)
25	CKI	I	Inverter input. (57.3MHz)
26	OSCO	O	Inverter output for oscillation. (57.3MHz)
27	OSCI	I	Inverter input for oscillation. (57.3MHz)
28	$V_{DD}3$	—	3.3V power supply. (Power supply for common logic block)
29	SSI	I	Serial interface data input for internal mode settings.
30	SCK	I	Serial interface clock input for internal mode settings.
31	SEN	I	Serial interface strobe input for internal mode settings.
32	VD	I	Vertical sync signal input.
33	HD	I	Horizontal sync signal input.
34	TRIG	I	Trigger pulse input.
35	WEN	O	Memory write timing pulse output.

Pin No.	Symbol	I/O	Description
36	$V_{SS}3$	—	GND (GND for common logic block)
37	V_M	—	GND (GND for vertical driver)
38	V1	O	CCD vertical register clock output.
39	V4	O	CCD vertical register clock output.
40	V2A	O	CCD vertical register clock output.
41	V_H	—	15.0V power supply. (Power supply for vertical driver)
42	V2B	O	CCD vertical register clock output.
43	NC	—	(Leave open.)
44	NC	—	(Leave open.)
45	V_L	—	–7.0V power supply. (Power supply for vertical driver)
46	NC	—	(Leave open.)
47	V3	O	CCD vertical register clock output.
48	SUB	O	CCD electronic shutter pulse output.

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	$V_{DD}1$	$V_{DD}a$		4.75	5.0	5.25	V
Supply voltage 2	$V_{DD}2$ to 4	$V_{DD}b$		3.0	3.3	3.6	V
Supply voltage 3	V_H	V_H		14.55	15.0	15.45	V
Supply voltage 4	V_M	V_M		—	0	—	V
Supply voltage 5	V_L	V_L		–7.5	–7.0	–6.5	V
Input voltage 1*1	RST, TEST1, SSI, SCK, SEN, VD, HD, TRIG	Vt_+		0.8$V_{DD}b$			V
		Vt_-				0.2$V_{DD}b$	V
Input voltage 2 *1, *2	SYNSL, TEST2	Vt_+		0.8$V_{DD}b$			V
		Vt_-				0.2$V_{DD}b$	V
Output voltage 1	XCPDM, XCPOB, PBLK, ADCLK, WEN	V_{OH1}	Feed current where I_{OH} = –3.3mA	$V_{DD}b$ – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 2	XSHD, XSHP, CKO	V_{OH2}	Feed current where I_{OH} = –6.6mA	$V_{DD}b$ – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 3	RG, MCKO	V_{OH3}	Feed current where I_{OH} = –10.4mA	$V_{DD}b$ – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 7.2mA			0.4	V
Output voltage 4	H1, H2	V_{OH4}	Feed current where I_{OH} = –22.0mA	$V_{DD}a$ – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 14.4mA			0.4	V
Output current 1	V1, V2A, V2B, V3, V4	I_{OL}	V1, V2A, V2B, V3, V4 = –8.25V	10.0			mA
		V_{OM1}	V1, V2A, V2B, V3, V4 = –0.25V			–5.0	mA
		V_{OM2}	V2A, V2B = 0.25V	5.0			mA
		V_{OH}	V2A, V2B = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 These input pins are Schmitt trigger inputs, and have a protective diode on the power supply side in the IC. Therefore, they do not support 5V input.

*2 These input pins are with pull-down resistor in the IC.

Note) This table shows the conditions for 3.3V drive.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth	—	—	$V_{DD}b/2$	—	V
Input voltage	OSCI	V_{IH}	—	$0.7V_{DD}b$	—	—	V
		V_{IL}	—	—	—	$0.3V_{DD}b$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –9mA	$V_{DD}b/2$	—	—	V
		V_{OL}	Pull-in current where I_{OL} = 9mA	—	—	$V_{DD}b/2$	V
Feedback resistor	OSCI OSCO	RFB	V_{IN} = $V_{DD}b$ or V_{SS}	500k	2M	5M	Ω
Oscillator frequency	OSCI OSCO	f	—	30	—	75	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth	—	—	$V_{DD}b/2$	—	V
Input voltage		V_{IH}	—	$0.7V_{DD}b$	—	—	V
		V_{IL}	—	—	—	$0.3V_{DD}b$	V
Input amplitude		V_{IN}	fmax 75MHz sine wave	0.3	—	—	Vp-p

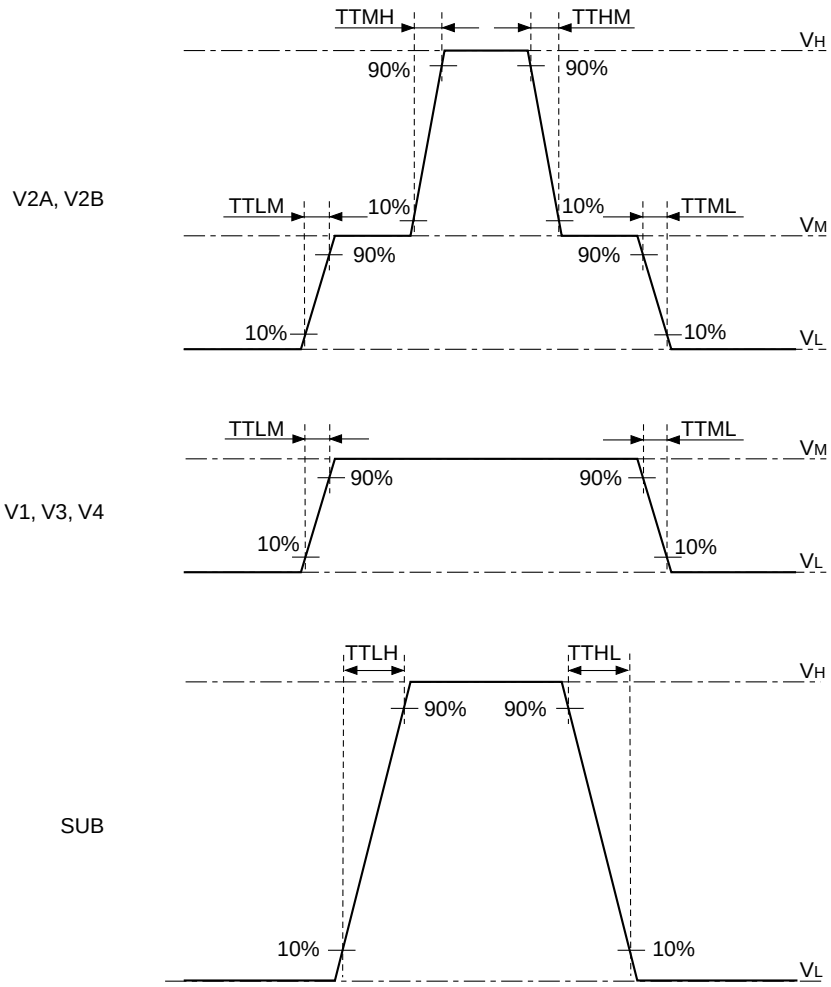
Note) Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

Switching Characteristics (V_H = 15.0V, V_M = GND, V_L = –7.0V)

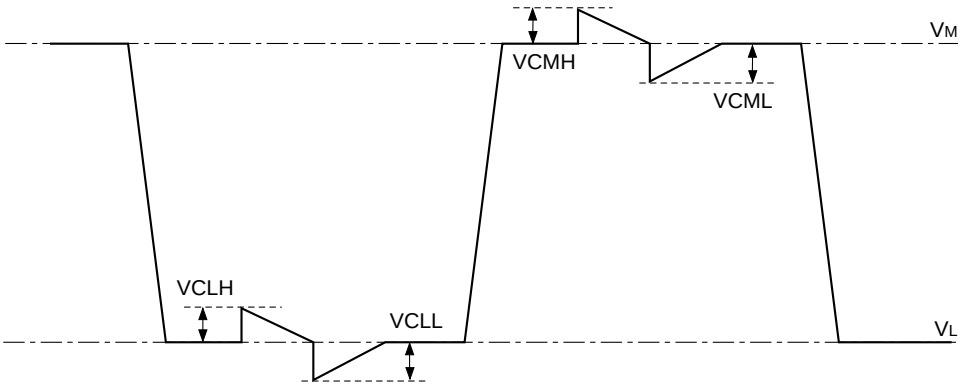
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	V_L to V_M	200	350	500	ns
	TTMH	V_M to V_H	200	350	500	ns
	TTLH	V_L to V_H	30	60	90	ns
Fall time	TTML	V_M to V_L	200	350	500	ns
	TTHM	V_H to V_M	200	350	500	ns
	TTHL	V_H to V_L	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

1. The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2. For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (V_H, V_L) and GND.
3. To protect the CCD image sensor, clamp the SUB pin output at V_H before input to the CCD image sensor. See the CCD image sensor data sheet for details.

Switching Waveforms

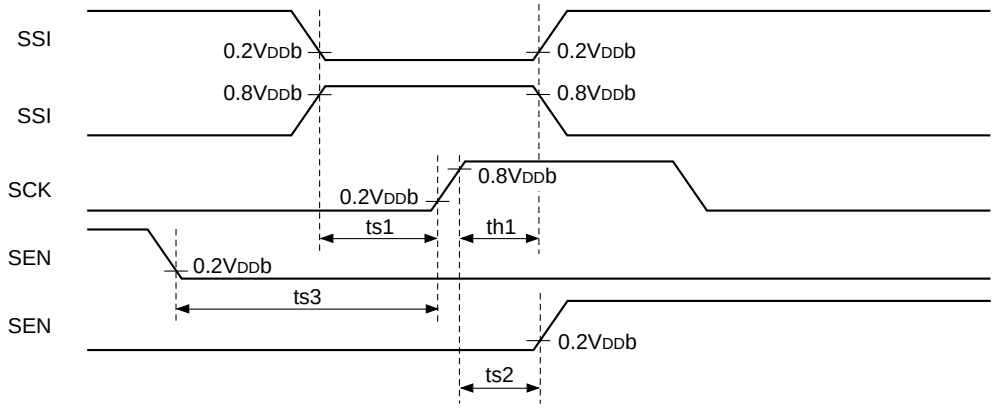


Waveform Noise



AC Characteristics

AC characteristics between the serial interface clocks

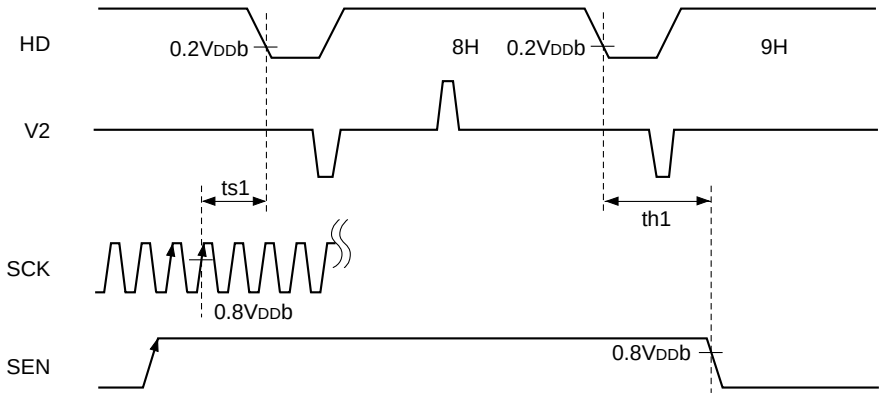


(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SCK	20			ns
th1	SSI hold time, activated by the rising edge of SCK	20			ns
ts2	SCK setup time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SCK	20			ns

Serial interface clock internal loading characteristics

Example: During FINE mode



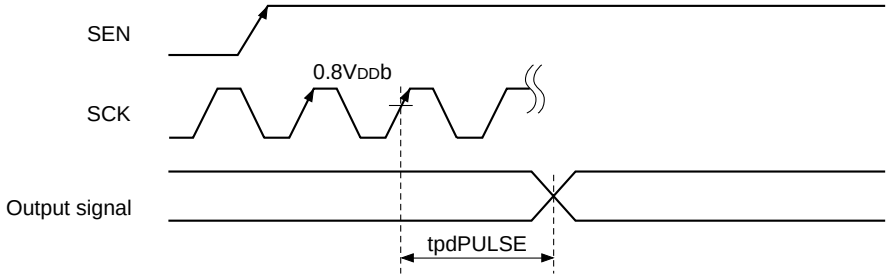
* Be sure to maintain a constantly high SEN logic level from around the falling edge of the HD 8H after the falling edge of VD to around the 9H falling edge and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	Second SCK clock setup time after the rising edge of SEN, activated by the falling edge of HD	5			ns
th1	SEN hold time, activated by the falling edge of 9H HD	30			µs

Serial interface clock output variation characteristics

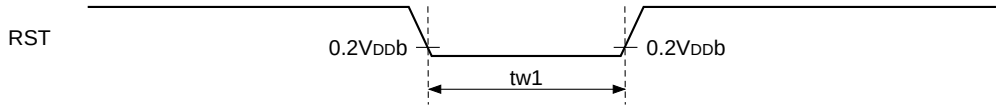
The serial interface data “Standby setting” is loaded to the CXD3607R and controlled at the rising edge of the second SCK clock after the rising edge of SEN.



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of the second SCK clock after the rising edge of SEN	10		100	ns

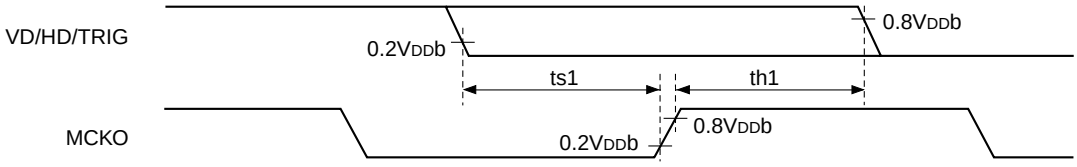
RST loading characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

VD, HD and TRIG loading characteristics

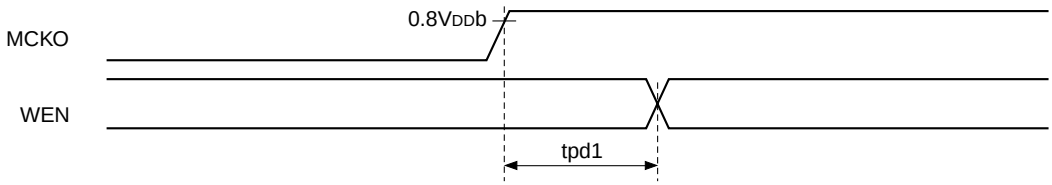


MCKO load capacitance = 16pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VD/HD/TRIG setup time, activated by the rising edge of MCKO	20			ns
th1	VD/HD/TRIG hold time, activated by the rising edge of MCKO	5			ns

Output variation characteristics



WEN load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until WEN changes after the rise of MCKO	–6		0	ns

Description of Operation

Pulses output from the CXD3607R are controlled mainly by the RST and SYNSL pins and by the serial interface data.

Control by the RST Pin

System reset is performed by setting the CXD3607R RST pin (Pin 2) low. After reset is canceled, the serial data block is "XSHP, XSHD logic phase adjustment setting" D0 bit = 1 and all other bits = 0.
In addition, when RST = low, some circuit operations in the IC are stopped as shown in the Pin Status Table below.

Pin Status Table (RST = low)

Pin No.	Symbol	I/O status	Pin No.	Symbol	I/O status
1	$V_{SS}4$	—	25	CKI	ACT
2	RST	L	26	OSCO	ACT
3	SYNSL	ACT	27	OSCI	ACT
4	NC	—	28	$V_{DD}3$	—
5	NC	—	29	SSI	DIS
6	NC	—	30	SCK	DIS
7	$V_{DD}4$	—	31	SEN	DIS
8	TEST1	—	32	VD	DIS
9	TEST2	—	33	HD	DIS
10	RG	ACT	34	TRIG	DIS
11	$V_{SS}1$	—	35	WEN	L
12	H1	ACT	36	$V_{SS}3$	—
13	H2	ACT	37	V_M	—
14	$V_{DD}1$	—	38	V1	V_L
15	$V_{DD}2$	—	39	V4	V_L
16	XSHD	ACT	40	V2A	V_M
17	XSHP	ACT	41	V_H	—
18	XCPDM	H	42	V2B	V_M
19	XCPOB	H	43	NC	—
20	PBLK	H	44	NC	—
21	ADCLK	ACT	45	V_L	—
22	MCKO	ACT	46	NC	—
23	CKO	ACT	47	V3	V_M
24	$V_{SS}2$	—	48	SUB	V_L

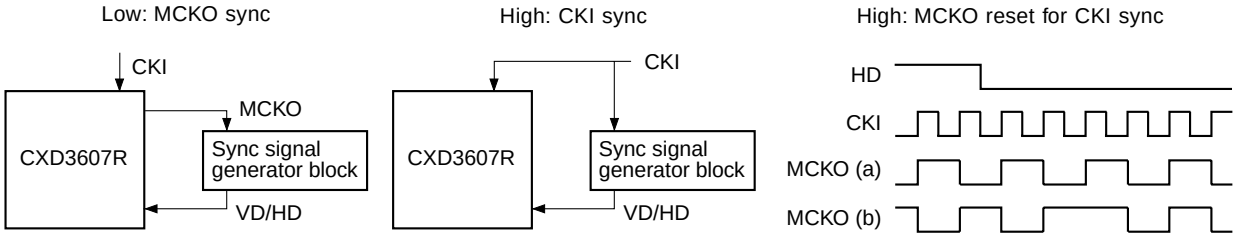
Note) ACT means that the circuit is operating, and DIS means that loading is stopped.
L indicates a low output level, and H a high output level in the controlled status.
V_M and V_L indicate the voltage levels applied to V_M (Pin 37) and V_L (Pin 45), respectively.

Control by the SYNSL Pin

The CXD3607R sync system can be switched by the CXD3607R SYNSL pin (Pin 3).

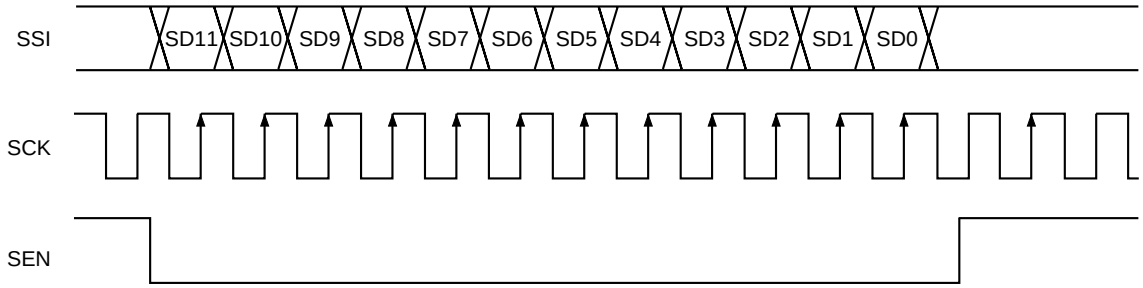
Low: MCKO sync (Normally use with this system configuration.)
Select this when sync signals VD and HD are generated by the MCKO output of the CXD3607R. The VD and HD inputs are loaded to the CXD3607R at the rising edge of the MCKO pulse.

High: CKI sync
Select this when sync signals VD and HD are generated by the CKI input of the CXD3607R. The VD and HD inputs are loaded to the CXD3607R at the rising edge of the CKI pulse, and the two MCKO logic phases (a) and (b) existing after power-on can be aligned at the initial HD input by resetting the internal clock.



Control by the Serial Interface Data

The CXD3607R loads the serial interface data in the following format at the rising edge of the second SCK clock after the rising edge of SEN.
* Make sure that SCK does not stop even while SEN is high.



In addition, the data are actually reflected at the following positions.

Data other than the following	→ Reflected at the falling edge of the HD 8H after the falling edge of VD.
2. Special drive data “SUB stop setting”	→ Reflected at the falling edge of the HD 9H after the falling edge of VD.
4. Shutter data “Shutter SUB setting”	→ Reflected at the falling edge of the HD 9H after the falling edge of VD.
5. TRIG data	→ Reflected at the falling edge of the HD 1H after the falling edge of TRIG. (Only when the TRIG function setting is 1: TRIG function enabled)
6. Other data “Standby setting”	→ Reflected at the rising edge of the second SCK clock after the rising edge of SEN.

There are six categories of serial interface data: drive mode data, special drive data, logic phase adjustment data, shutter data, TRIG data and other data. The details of the data for each category are described below.
* After reset is canceled, the serial data block is “XSHP, XSHD logic phase adjustment setting” D0 bit = 1 and all other bits = 0.

1. Drive mode data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Description of settings
0	1	1	1	0	1	1	0	X	D2	D1	D0	Drive mode setting, TRIG function setting

2. Special drive data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Description of settings
0	0	1	0	1	0	X	X	X	X	D1	D0	SG and SUB stop settings

3. Logic phase adjustment data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Description of settings
1	0	0	1	1	D1	D0	0	0	0	0	0	XSHP logic phase adjustment setting
		1	0	0	D1	D0	0	0	0	0	0	XSHD logic phase adjustment setting
			0	1	D1	D0	0	0	0	0	0	ADCLK logic phase adjustment setting

4. Shutter data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Description of settings
1	1	0	0	1	0	D5	D4	D3	D2	D1	D0	Shutter V setting
					1	D11	D10	D9	D8	D7	D6	
			1	0	0	D5	D4	D3	D2	D1	D0	Shutter SUB setting
					1	D11	D10	D9	D8	D7	D6	

5. TRIG data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Description of settings
0	1	1	1	1	0	0	0	D3	D2	D1	D0	SG and SUB stop settings High-speed sweep setting Clamp pulse stop setting
						0	1	D3	D2	D1	D0	SG generation position setting
						1	0	D7	D6	D5	D4	
						1	1	X	D10	D9	D8	
					1	0	0	D3	D2	D1	D0	SUB setting
							1	D7	D6	D5	D4	

6. Other data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Description of settings
1	1	1	1	1	0	0	X	X	X	X	D0	Standby setting

Detailed Description of each Data

1. Drive mode data

(1) Drive mode setting

The CXD3607R drive mode can be switched as follows.

* TRIGOUT mode is the mode which stops the SG pulse (ternary value output of the V2A and V2B pulses) and the corresponding V pulse of FINE mode. Note that this is different from the special drive data “SG stop setting”.

D1	D0	Description of operation
0	0	DRAFT mode
0	1	FINE mode
1	X	TRIGOUT mode

(2) TRIG function setting (valid in DRAFT, FINE and TRIGOUT modes)

The CXD3607R random trigger shutter function disabled/enabled setting can be switched as follows.

* For details, see “Special Drive Sequence (Random trigger shutter drive)”.

D2	Description of operation
0	TRIG function disabled
1	TRIG function enabled

2. Special drive data

(1) SG stop setting (valid in DRAFT and FINE modes)

SG pulse (ternary value output of the V2A and V2B pulses) stopped/not stopped can be selected by the D0 setting.

* When SG stopped is selected, the corresponding V pulse is not stopped.
* When SG stopped is selected, WEN becomes inactive during that VD period.

D0	Description of operation
0	SG not stopped
1	SG stopped

(2) SUB pulse stop setting (valid in DRAFT, FINE and TRIGOUT modes)

SUB pulse stopped/not stopped can be selected by the D1 setting.

D1	Description of operation
0	SUB not stopped
1	SUB stopped

3. Logic phase adjustment data

(1) XSHP and XSHD logic phase adjustment setting

The XSHP and XSHD logic phase adjustment can be selected by the D1 and D0 setting.

* The default when reset is 90°.
* For details, see the high-speed phase timing chart.

D1	D0	Description of operation
0	0	0°
0	1	90° (default)
1	0	180°
1	1	270°

(2) ADCLK logic phase adjustment setting

The ADCLK logic phase adjustment can be selected by the D1 and D0 setting.

* The default when reset is 0° (pulse delayed 90° relative to MCKO).
* For details, see the high-speed phase timing chart.

D1	D0	Description of operation
0	0	0° (default)
0	1	90°
1	0	180°
1	1	270°

4. Shutter data

(1) Shutter V setting (valid in DRAFT and FINE modes)

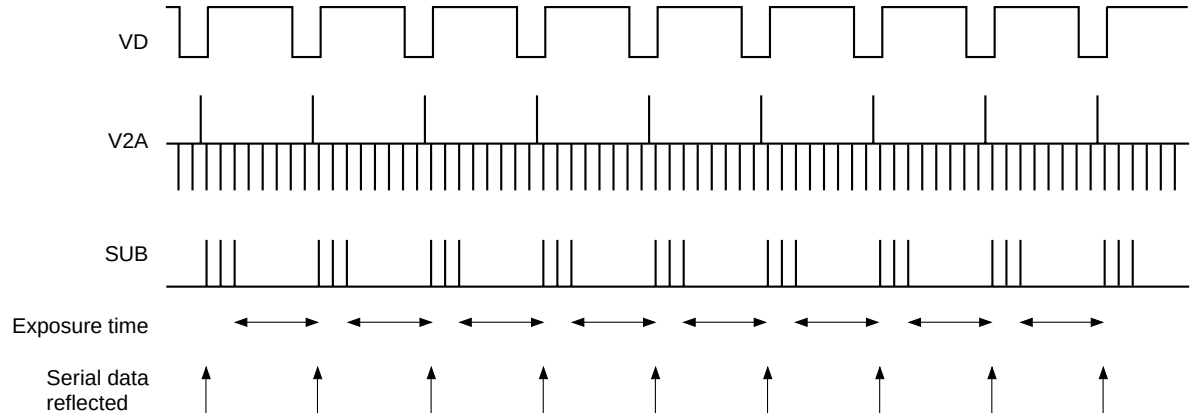
The SG stopped VD period, that is to say the exposure time, can be adjusted from 0 to 4095V in 1V units by the D11 to D0 setting. Setting all 0 results in the high-speed shutter corresponding to the shutter SUB setting.

* During the SG stopped VD period, data other than 5. TRIG data and 6. Other data are not reflected.
* During the SG stopped VD period, only the SG pulse is stopped, and the corresponding V pulse is not stopped.
* During the SG stopped VD period, PBLK, XCPOB and XCPDM are active, and WEN is inactive.

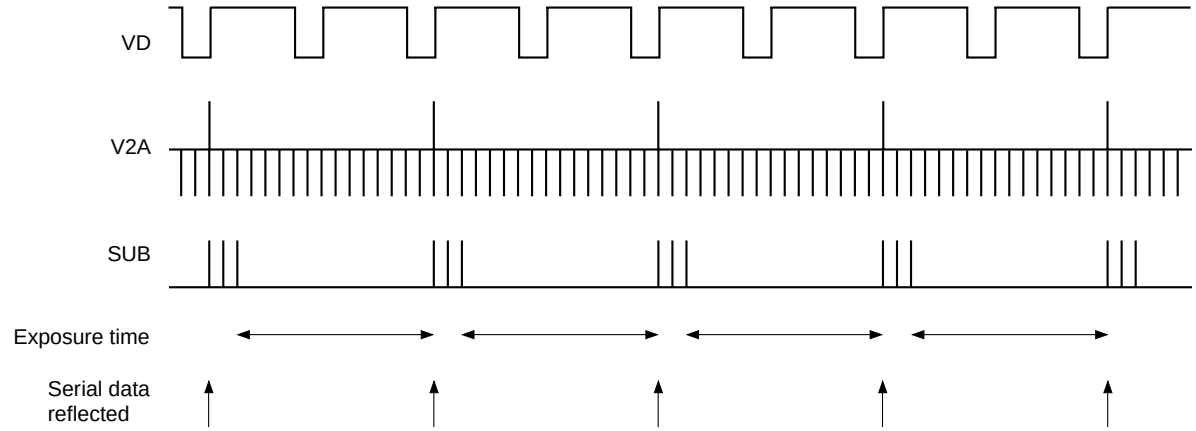
The SG stopped VD period (V) for each serial setting value and the shutter V setting outline diagrams (for SG stopped VD periods 0V and 1V) are shown below.

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SG stopped VD period (V)
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	1	0	2
						:						:
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

Shutter V setting: 0V = high-speed shutter



Shutter V setting: 1V

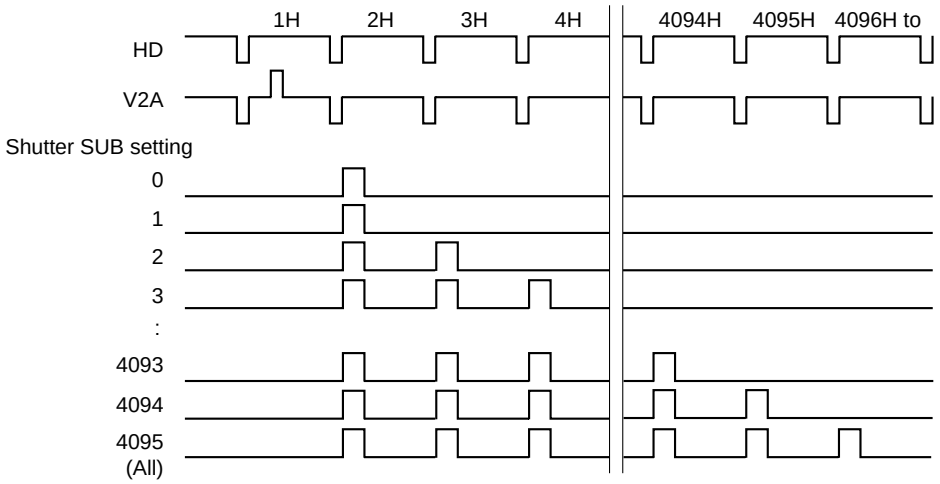


(2) Shutter SUB setting (valid in DRAFT, FINE and TRIGOUT modes)

The charge drain period by the SUB pulse can be adjusted from 1 to 4095H in 1H units by the D11 to D0 setting. The number of SUB pulses for each serial setting value is shown below.

* Setting values in excess of the maximum number of pulses per VD period (example: 1068 pulses for VD = 1068H) are fixed to the maximum number of pulses.
* When performing long-time exposure with the shutter V setting, setting values in excess of the maximum number of pulses per VD period are fixed to the maximum number of pulses.
* Setting all 1 results in all SUB output (ALL), for any VD period.

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Number of SUB pulses
0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	0	1	1	3
:												:
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	All



5. TRIG data

(1) SG stop setting (valid only during TRIG drive)

SG pulse (ternary value output of the V2A and V2B pulses) stopped/not stopped during TRIG drive can be selected by the D0 setting.

* When SG stopped is selected, the corresponding V pulse is not stopped.

D0	Description of operation
0	SG not stopped (TRIG drive)
1	SG stopped (TRIG drive)

(2) SUB stop setting (valid only during TRIG drive)

SUB pulse stopped/not stopped during TRIG drive can be selected by the D1 setting.

D1	Description of operation
0	SUB not stopped (TRIG drive)
1	SUB stopped (TRIG drive)

(3) High-speed sweep setting (valid only during TRIG drive)

High-speed sweep on/off during TRIG drive can be selected by the D2 setting.
(For details, see Chart-4 to Chart-7.)

D2	Description of operation
0	High-speed sweep on (TRIG drive)
1	High-speed sweep off (TRIG drive)

* The number of V transfers (stages) for high-speed sweep differs according to the drive mode during TRIG pulse input.
(For details, see Chart-12 and Chart-13.)
DRAFT mode: 20 (stages/H) × 53 (H) = 1060 (stages)
FINE/TRIGOUT mode: 5 (stages/H) × 210 (H) = 1050 (stages)

(4) Clamp pulse stop setting (valid only during TRIG drive)

XCPDM, XCPOB and PBLK stopped/not stopped from SG pulse generation until 7H after the falling edge of the next valid VD during TRIG drive can be selected by the D3 setting.
(For details, see Chart-4 to Chart-7.)

D3	Description of operation
0	Clamp pulses not stopped (TRIG drive)
1	Clamp pulses stopped (TRIG drive)

(5) SG generation position setting (valid only during TRIG drive)

The SG pulse (ternary value output of the V2A and V2B pulses) generation position during TRIG drive can be selected from 2 to 2048H counting from the next HD after the falling edge of the TRIG pulse by the D10 to D0 setting. The SG generation position (H) for each serial setting value is shown below.
(For details, see Chart-4 to Chart-7.)

D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SG generation position (H)
0	0	0	0	0	0	0	0	0	0	0	2
0	0	0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	0	0	1	1	4
:											:
1	1	1	1	1	1	1	1	1	0	1	2046
1	1	1	1	1	1	1	1	1	1	0	2047
1	1	1	1	1	1	1	1	1	1	1	2048

* When high-speed sweep is on, a SG generation prohibited area exists. When this area is designated, the SG pulse is generated at the position indicated below. When the drive mode during TRIG pulse input is:
  DRAFT mode: When the prohibited area 2 to 57H is designated, the SG pulse is generated at 58H.
  FINE/TRIGOUT mode: When the prohibited area 2 to 214H is designated, the SG pulse is generated at 215H.
* VD input is not accepted until 2H after the SG generation position (H), and is accepted from 3H onward. (Example: When the SG generation position is 58H, VD input is not accepted from 1 to 59H, and is accepted from 60H onward.)

(6) SUB setting (valid only during TRIG drive)

The number of SUB pulses during TRIG drive can be selected by the D7 to D0 setting. The number of SUB pulses for each serial setting value is shown below.

D7	D6	D5	D4	D3	D2	D1	D0	Number of SUB pulses
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:								:
1	1	0	1	0	1	0	1	213
1	1	0	1	0	1	1	0	214
1	1	0	1	0	1	1	1	215

* When high-speed sweep is off, the number of SUB pulses is two regardless of the drive mode during TRIG pulse input and the SUB setting value.
* When high-speed sweep is on, the maximum number of SUB pulses is as follows according to the drive mode during TRIG pulse input. Setting values in excess of the maximum number of pulses are fixed to the maximum number of pulses. (For details, see Chart-4 to Chart-7.)
  DRAFT mode: Max. 58 pulses
  FINE/TRIGOUT mode: Max. 215 pulses

6. Other data

(1) Standby setting

Standby operation can be selected by the D0 setting. The Pin Status Table during standby operation is shown below.

* The standby setting bit is loaded at the rising edge of the second SCK clock after the rising edge of SEN, and control is applied immediately.
* Serial data is loaded as normal during standby operation.

D0	Description of operation
0	Normal operation
1	Standby operation

Pin Status Table (Standby setting bit = 1)

Pin No.	Symbol	I/O status	Pin No.	Symbol	I/O status
1	$V_{SS}4$	—	25	CKI	ACT
2	RST	ACT	26	OSCO	ACT
3	SYNSL	ACT	27	OSCI	ACT
4	NC	—	28	$V_{DD}3$	—
5	NC	—	29	SSI	ACT
6	NC	—	30	SCK	ACT
7	$V_{DD}4$	—	31	SEN	ACT
8	TEST1	—	32	VD	DIS
9	TEST2	—	33	HD	DIS
10	RG	L	34	TRIG	DIS
11	$V_{SS}1$	—	35	WEN	L
12	H1	L	36	$V_{SS}3$	—
13	H2	L	37	V_M	—
14	$V_{DD}1$	—	38	V1	V_M
15	$V_{DD}2$	—	39	V4	V_M
16	XSHD	L	40	V2A	V_H
17	XSHP	L	41	V_H	—
18	XCPDM	L	42	V2B	V_H
19	XCPOB	L	43	NC	—
20	PBLK	L	44	NC	—
21	ADCLK	L	45	V_L	—
22	MCKO	ACT	46	NC	—
23	CKO	ACT	47	V3	V_M
24	$V_{SS}2$	—	48	SUB	V_H

Note) ACT means that the circuit is operating, and DIS means that loading is stopped.
L indicates a low output level, and H a high output level in the controlled state.
V_M and V_L indicate the voltage levels applied to V_M (Pin 37) and V_L (Pin 45), respectively.

Detailed Description of Output Pins

The CXD3607R generates special pulses that are used by signal processing circuits, etc. These details are described below.

• WEN (Pin 30)

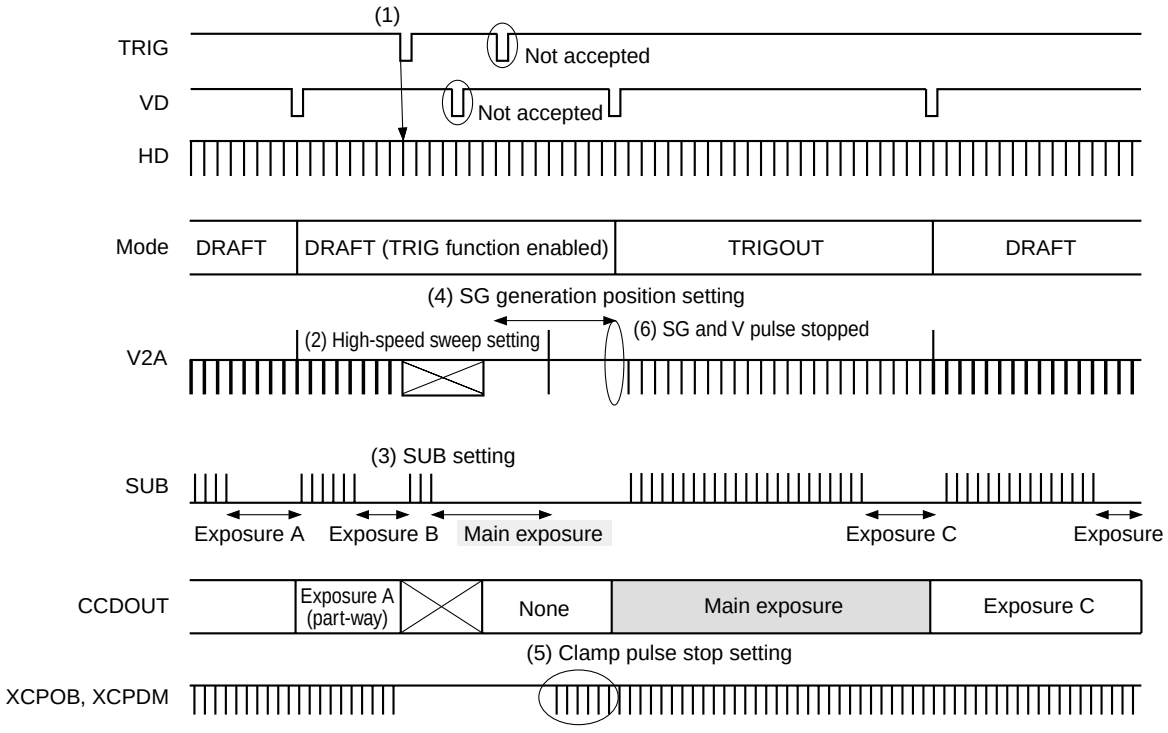
The CXD3607R outputs a WEN signal that indicates the effective line period output from the CCD image sensor. The WEN signal is high during the vertical effective line period. For details, see the vertical timing charts for each drive mode.

* When SG stopped is selected by the SG stop setting, WEN is inactive during the SG stopped VD period.
* When performing long-time exposure with the shutter V setting, WEN is inactive during the SG stopped VD period.

Special Drive Sequence (Random trigger shutter drive)

Cameras using the CXD3607R can perform random trigger shutter drive which allows image capturing at an optional timing. The TRIG pulse is loaded from the TRIG pin at the rising edge of MCKO, and reflected from the falling edge of the next HD.

The random trigger shutter drive sequence in DRAFT mode is shown below.



(1) If the drive mode data “TRIG function setting” is 1: Enabled at the falling edge of the TRIG pulse, operation switches to TRIG drive.
   * Operation cannot be guaranteed for a TRIG pulse low-active period of 2H or less.
   * The TRIG pulse is valid when input with the falling edge synchronized to the falling edge of VD.
   * The TRIG pulse is not accepted after switching to TRIG drive.
   * The VD pulse is not accepted for until 2H after SG generation after switching to TRIG drive. Serial data is also not reflected by the falling edge of VD during this period. (Example: When SG is generated at 58H, VD is not accepted from 1 to 59H)

(2) Operation switches to TRIG drive mode and high-speed sweep for vertical register block charge drain starts from the falling edge of the next HD after the falling edge of the input TRIG pulse. The number of high-speed sweep stages differs according to the drive mode at the falling edge of the TRIG pulse as follows. DRAFT: 20 (stages/H) × 53 (H) = 1060 (stages), FINE/TRIGOUT: 5 (stages/H) × 210 (H) = 1050 (stages). High-speed sweep off can also be selected by the TRIG data “High-speed sweep setting”.

(3) The charge drain period using the SUB pulse can be selected by the TRIG data “SUB setting”.
When high-speed sweep is on, the maximum number of SUB pulses is as follows according to the drive mode at the falling edge of the TRIG pulse. DRAFT: max. 58 pulses, FINE/TRIGOUT: max. 215 pulses.
When high-speed sweep is off, the number of SUB pulses is two regardless of the drive mode at the falling edge of the TRIG pulse and the SUB setting value.

(4) The SG pulse generation position can be selected by the TRIG data “SG generation position setting”. After SG pulse output, V transfer is not performed and standby mode is established until the next VD input.

(5) The clamp pulses can also be stopped after SG pulse generation by the TRIG data “Clamp pulse stop setting”.

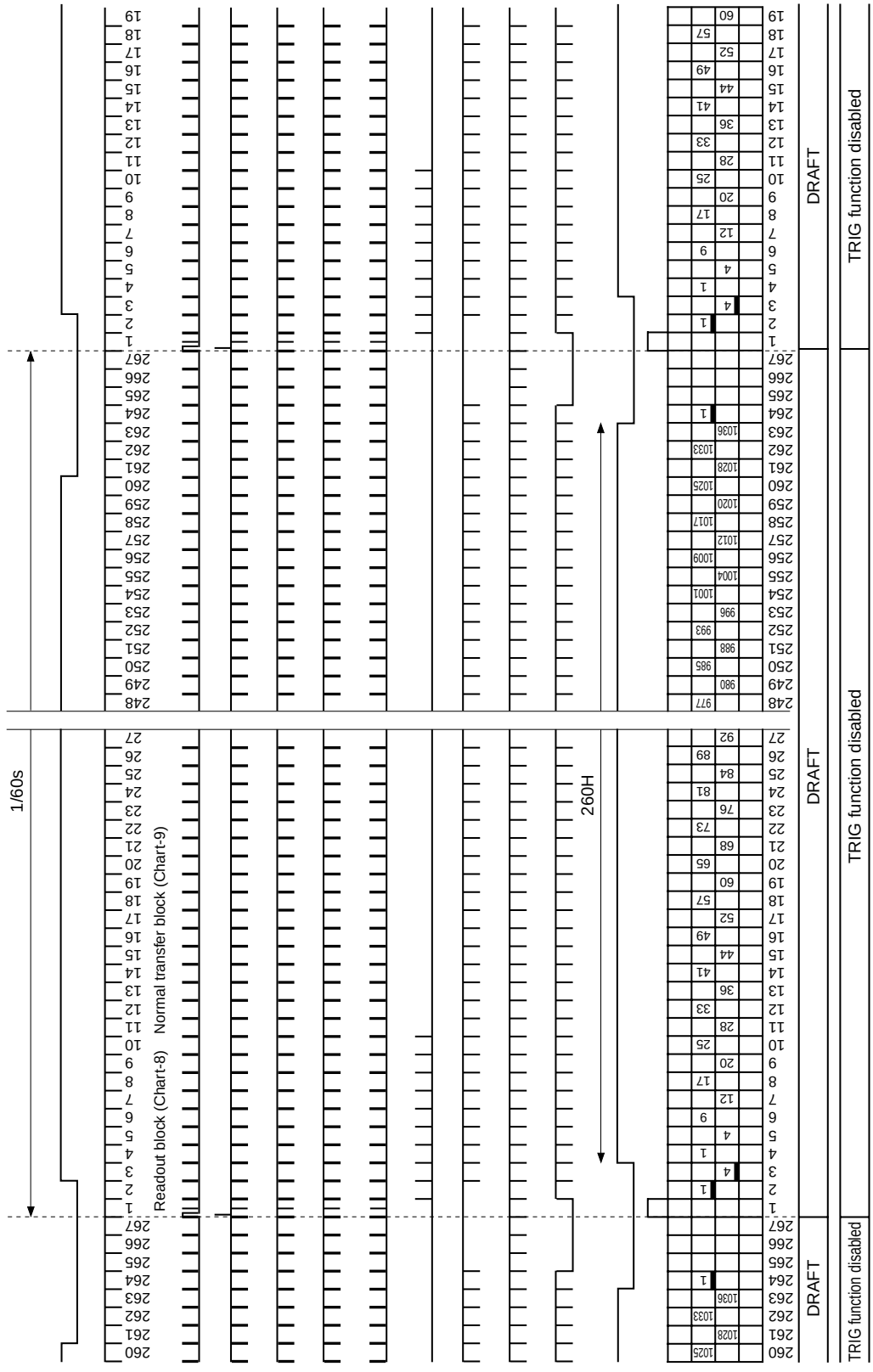
(6) Be sure to drive in TRIGOUT mode during the next VD period after TRIG drive. (Operation in other modes can be not guaranteed.)
   * TRIG drive ends at the first VD input 3H onward after SG pulse generation. Even when operation shifted to TRIG drive during long-time exposure using the “Shutter V setting”, note that serial data is always reflected at the first VD input 3H onward after SG pulse generation.

Specifications for Each Drive Mode and A Table Corresponding Timing Charts

Drive mode	Frame rate (s)	Total number of HD (H)	High-speed sweep H period (H)	Number of high-speed sweep stages (stage)	Vertical timing chart	Readout block H chart	Normal transfer block H chart	High-speed sweep block H chart
DRAFT	1/60	267	0	0	Chart-1	Chart-8	Chart-9	—
FINE	1/15	1068	0	0	Chart-2	Chart-10	Chart-11	—
TRIGOUT	1/15	1068	0	0	Chart-3	—	Chart-11	—
DRAFT → TRIG (high-speed sweep on)	—	—	53 (fixed)	1060 (fixed)	Chart-4	Chart-10	—	Chart-12
DRAFT → TRIG (high-speed sweep off)	—	—	0	0	Chart-5	Chart-10	—	—
FINE/TRIGOUT → TRIG (high-speed sweep on)	—	—	210 (fixed)	1050 (fixed)	Chart-6	Chart-10	—	Chart-13
FINE/TRIGOUT → TRIG (high-speed sweep off)	—	—	0	0	Chart-7	Chart-10	—	—

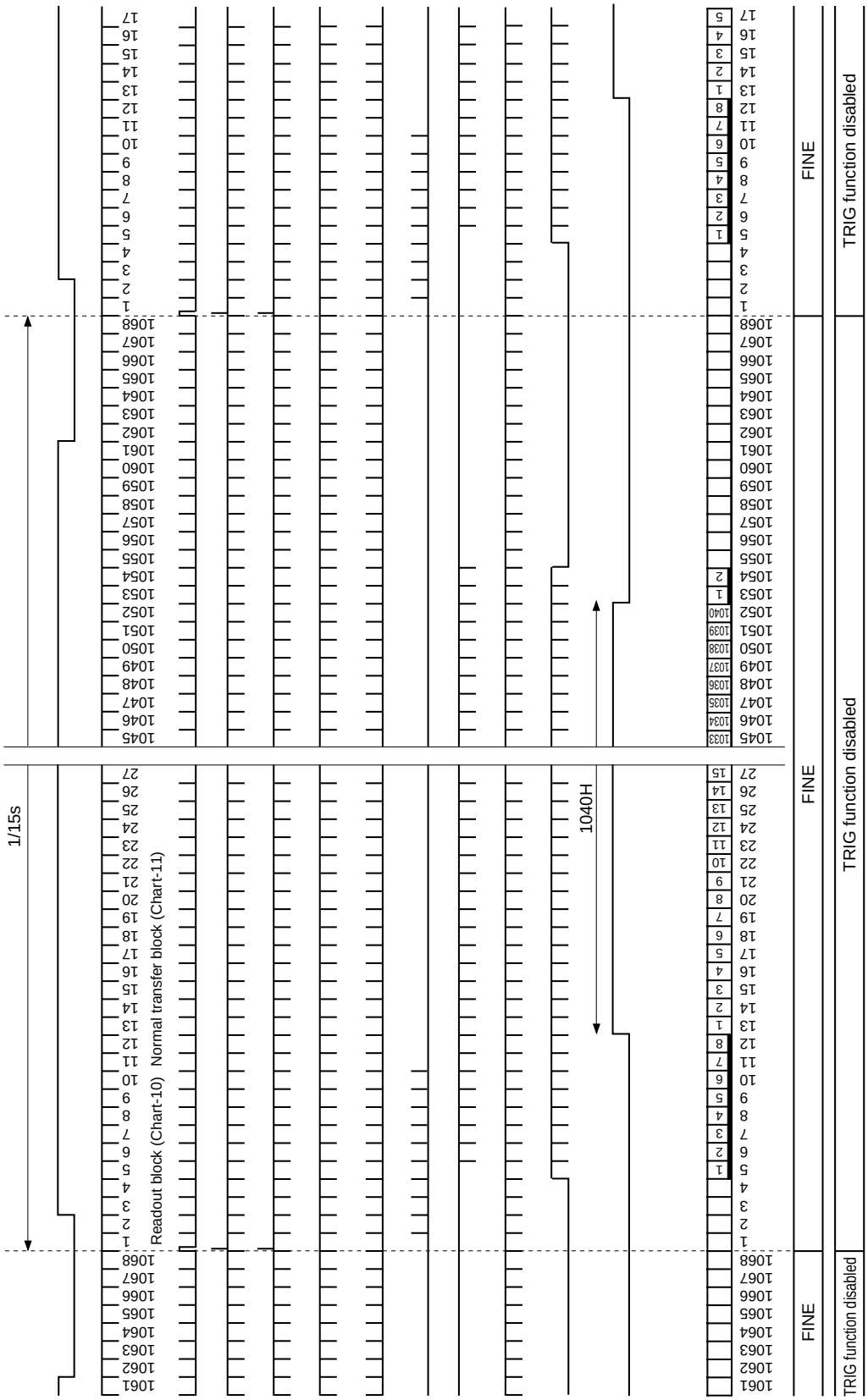
Chart-1 Vertical Timing Chart

MODE
DRAFT mode



* The number of SUB pulses is determined by the serial interface data.

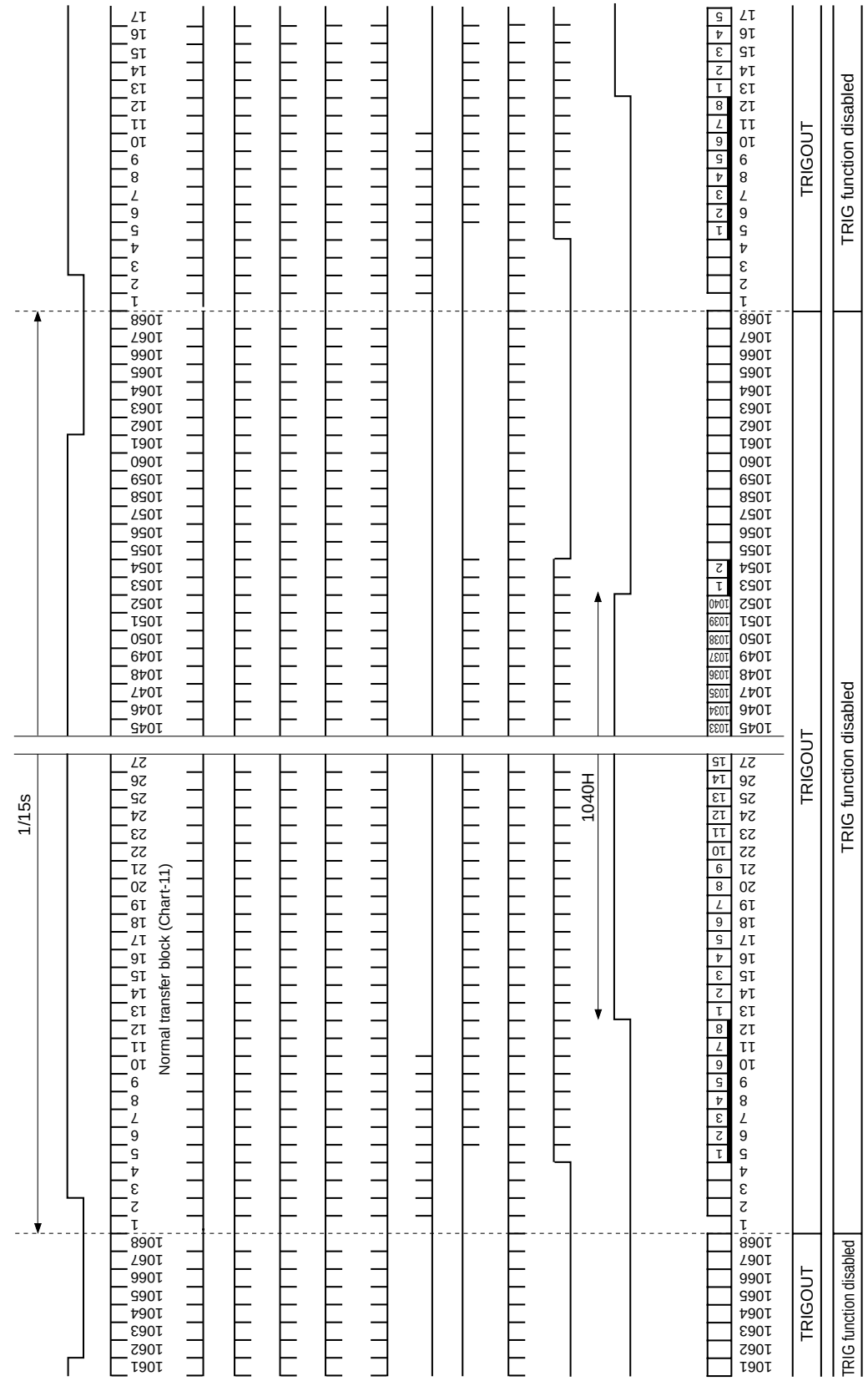
Chart-2 Vertical Timing Chart **MODE** FINE mode



* The number of SUB pulses is determined by the serial interface data.

Chart-3 Vertical Timing Chart

MODE
TRIGOUT mode



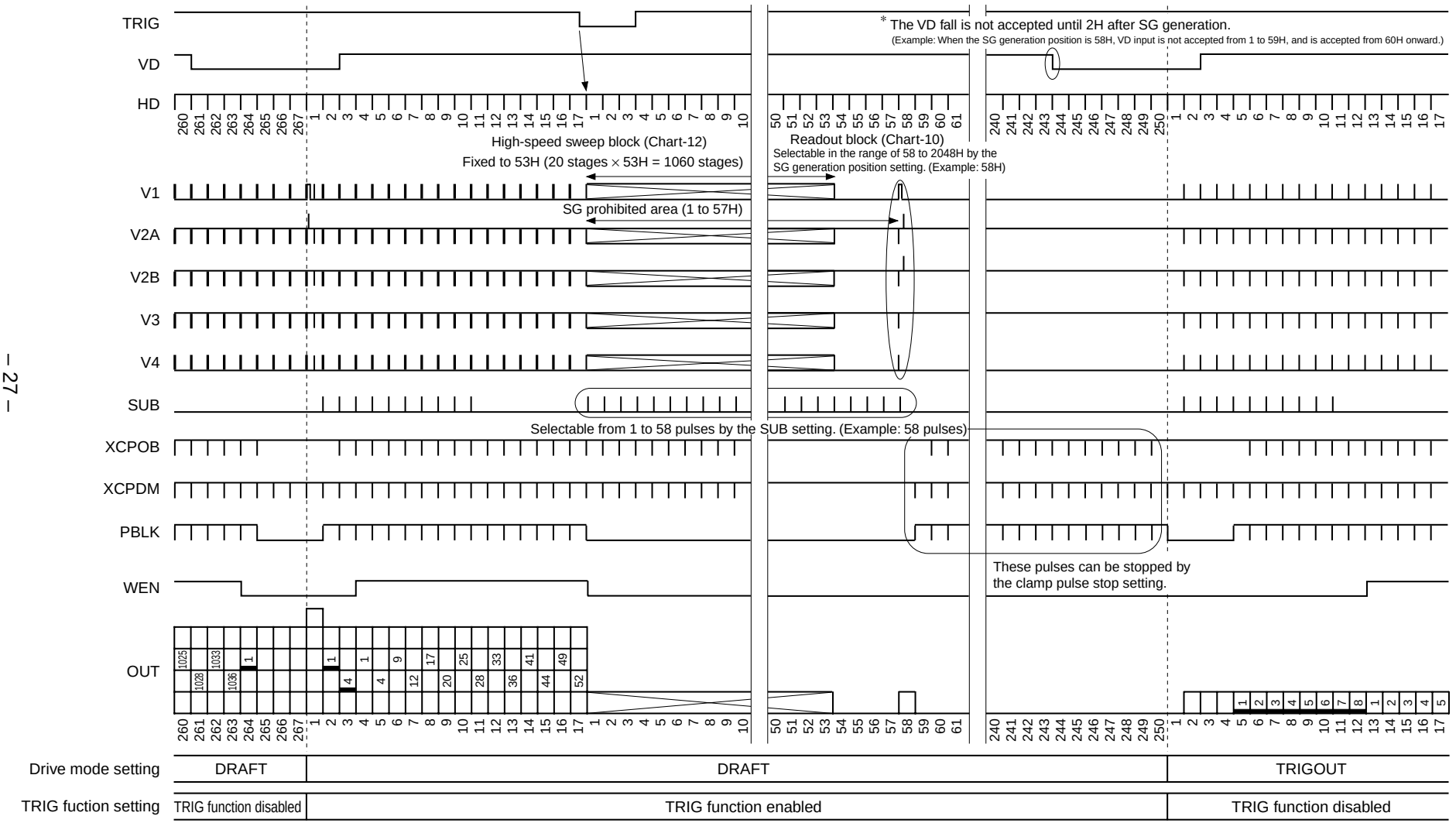
* The number of SUB pulses is determined by the serial interface data.

Chart-4 Vertical Timing Chart

MODE

DRAFT mode → TRIG drive

(High-speed sweep on, SG generation position: 58H, SUB setting: 58 pulses)



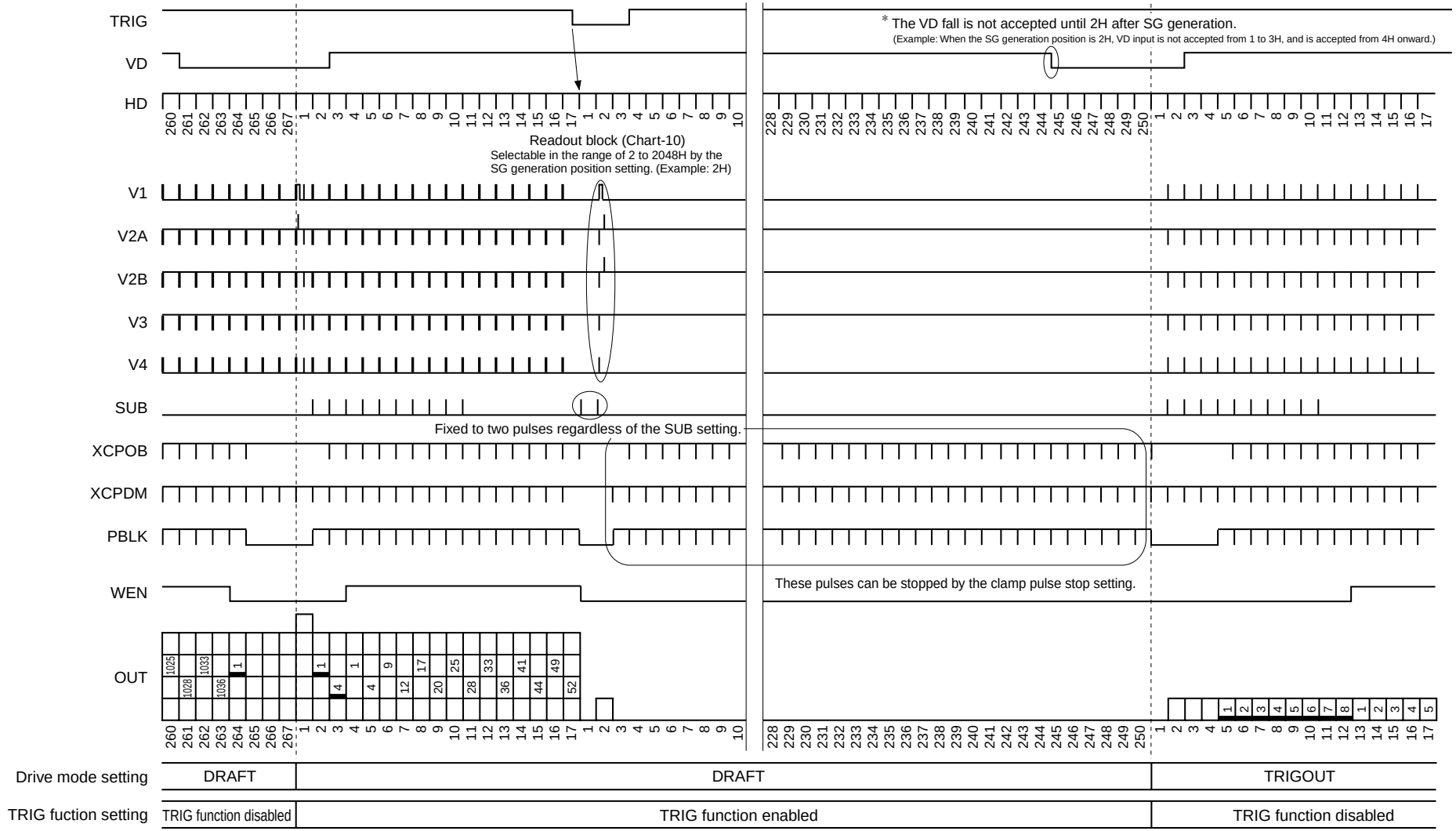
* The number of SUB pulses is determined by the serial interface data.

Chart-5 Vertical Timing Chart

MODE

DRAFT mode → TRIG drive

(High-speed sweep off, SG generation position: 2H, SUB setting: fixed to 2 pulses)



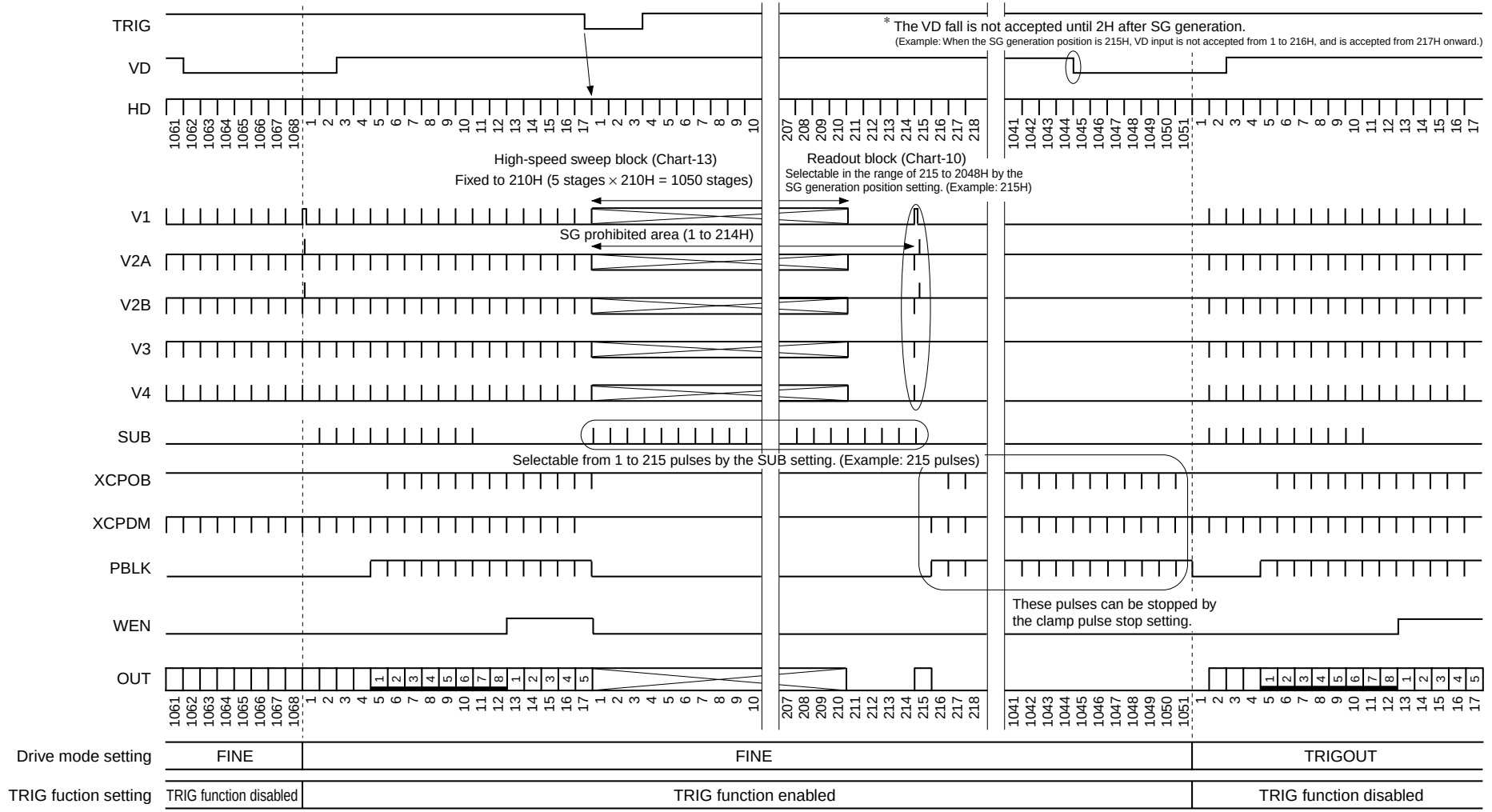
* The number of SUB pulses is determined by the serial interface data.

Chart-6 Vertical Timing Chart

MODE

FINE/TRIGOUT mode → TRIG drive

(High-speed sweep on, SG generation position: 215H, SUB setting: 215 pulses)



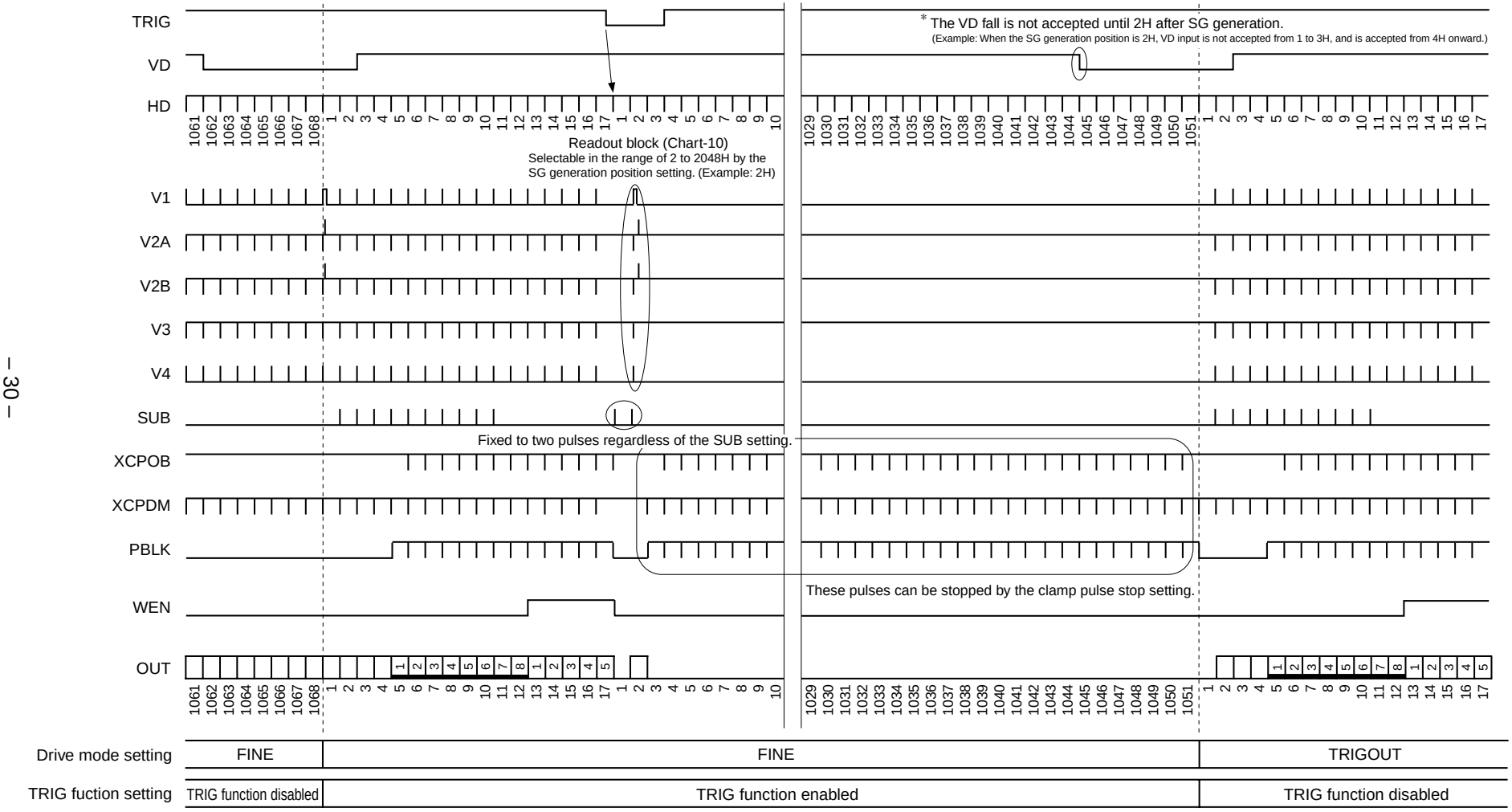
* The number of SUB pulses is determined by the serial interface data.

Chart-7 Vertical Timing Chart

MODE

FINE/TRIGOUT mode → TRIG drive

(High-speed sweep off, SG generation position: 2H, SUB setting: fixed to 2 pulses)

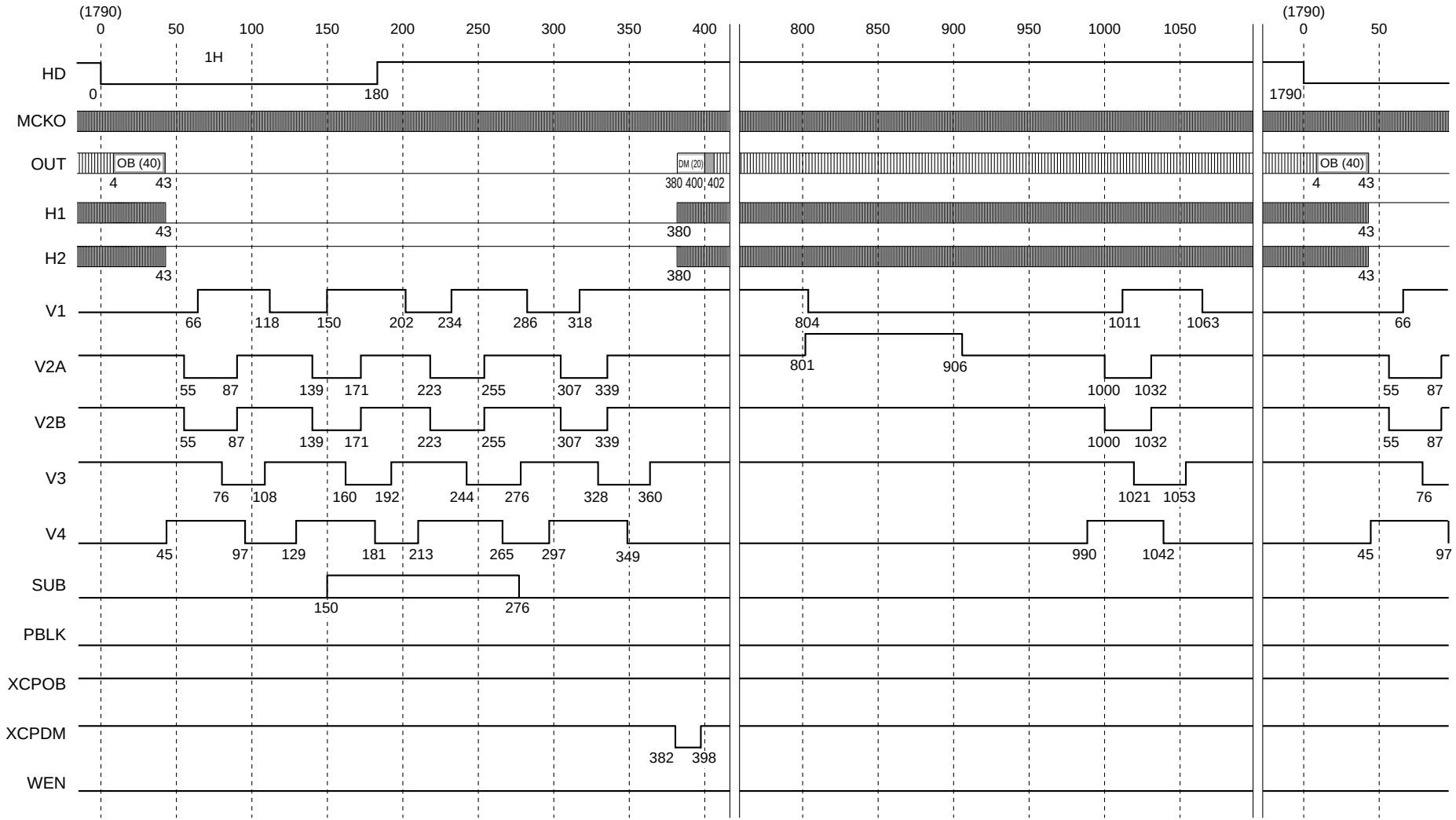


* The number of SUB pulses is determined by the serial interface data.

Chart-8 Horizontal Timing Chart

MODE

DRAFT mode readout block

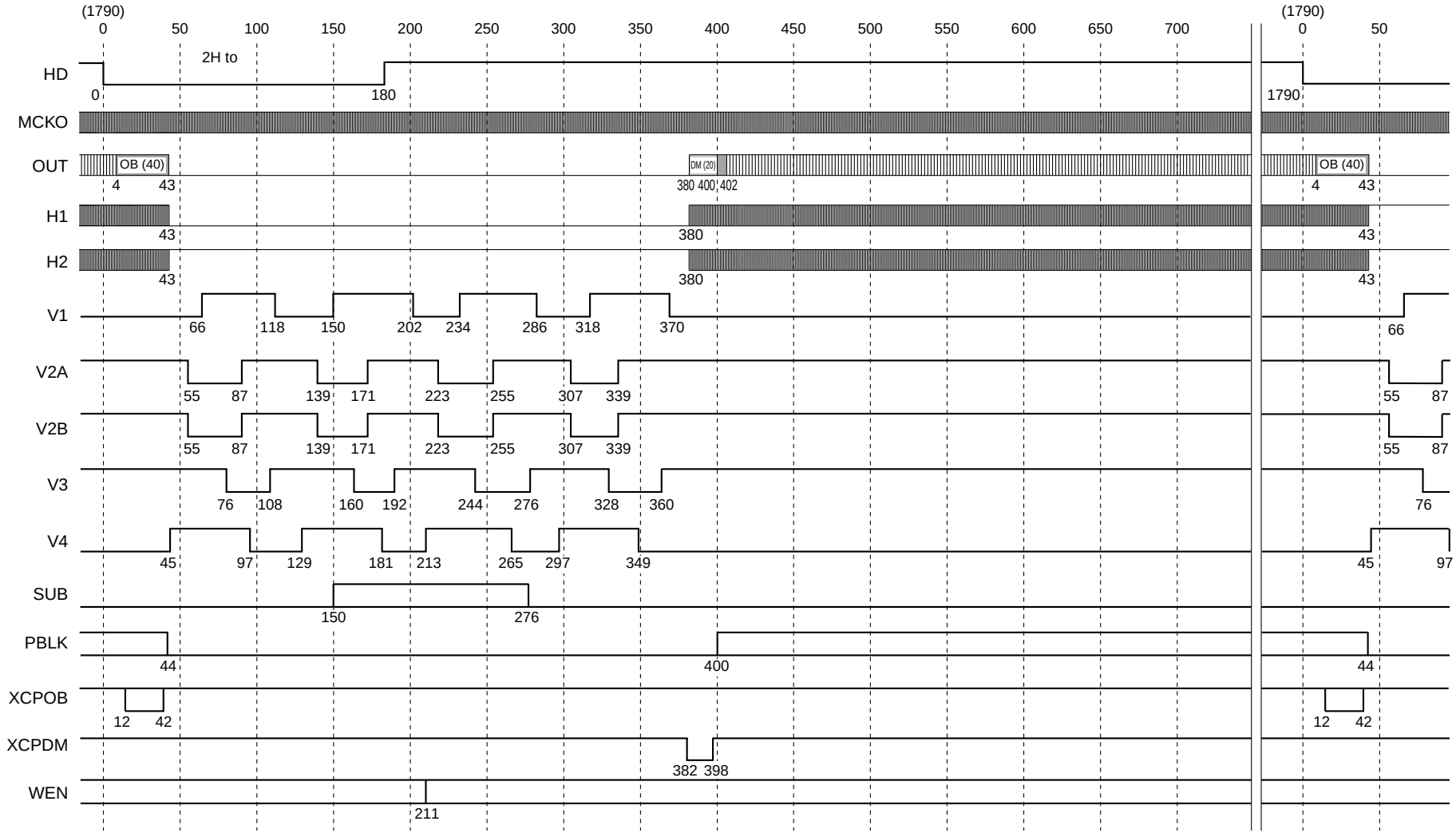


* The HD of this chart indicates the actual CXD3607R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

Chart-9 Horizontal Timing Chart

MODE

DRAFT mode normal transfer block

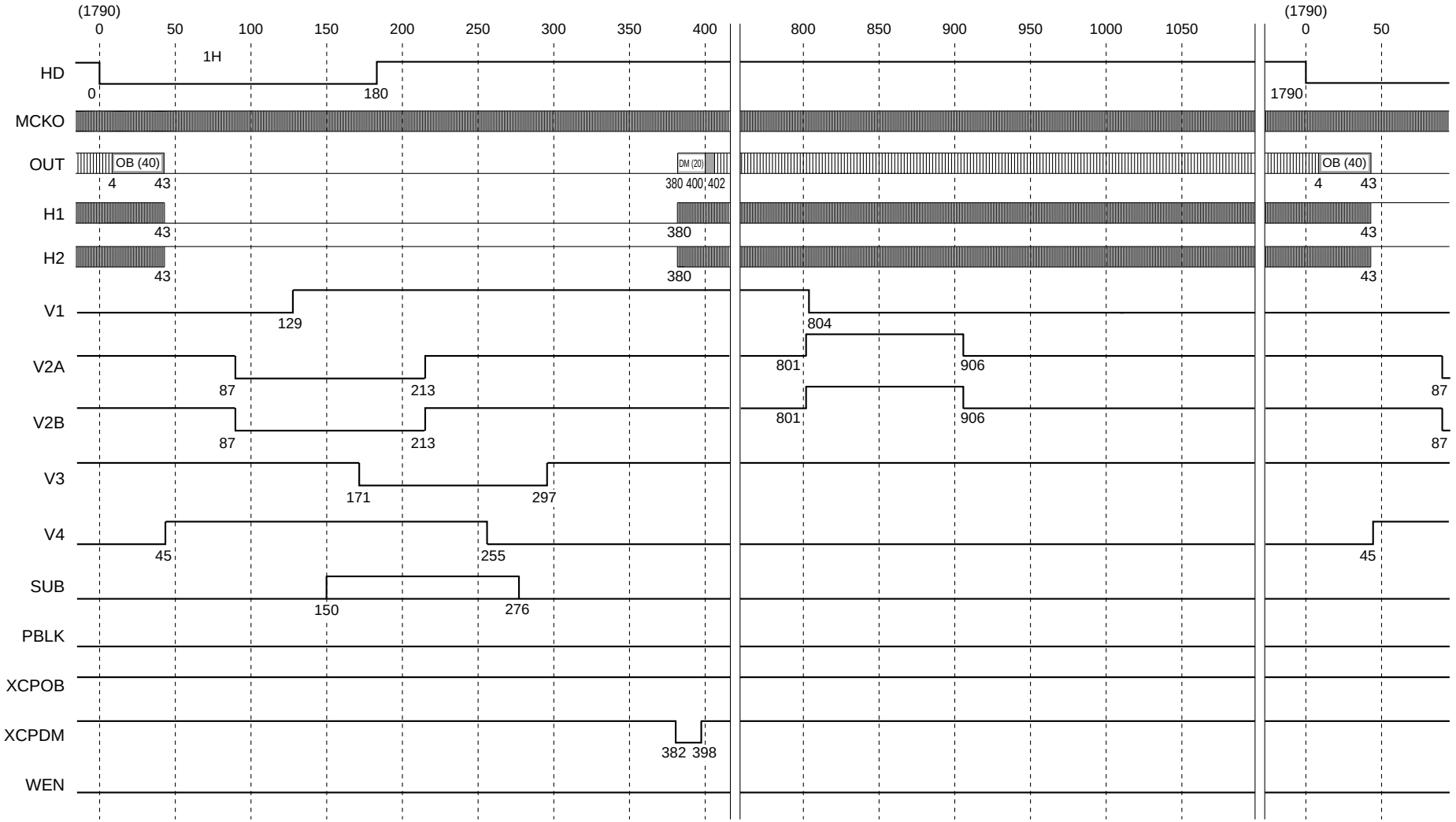


* The HD of this chart indicates the actual CXD3607R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

Chart-10 Horizontal Timing Chart

MODE

FINE mode readout block

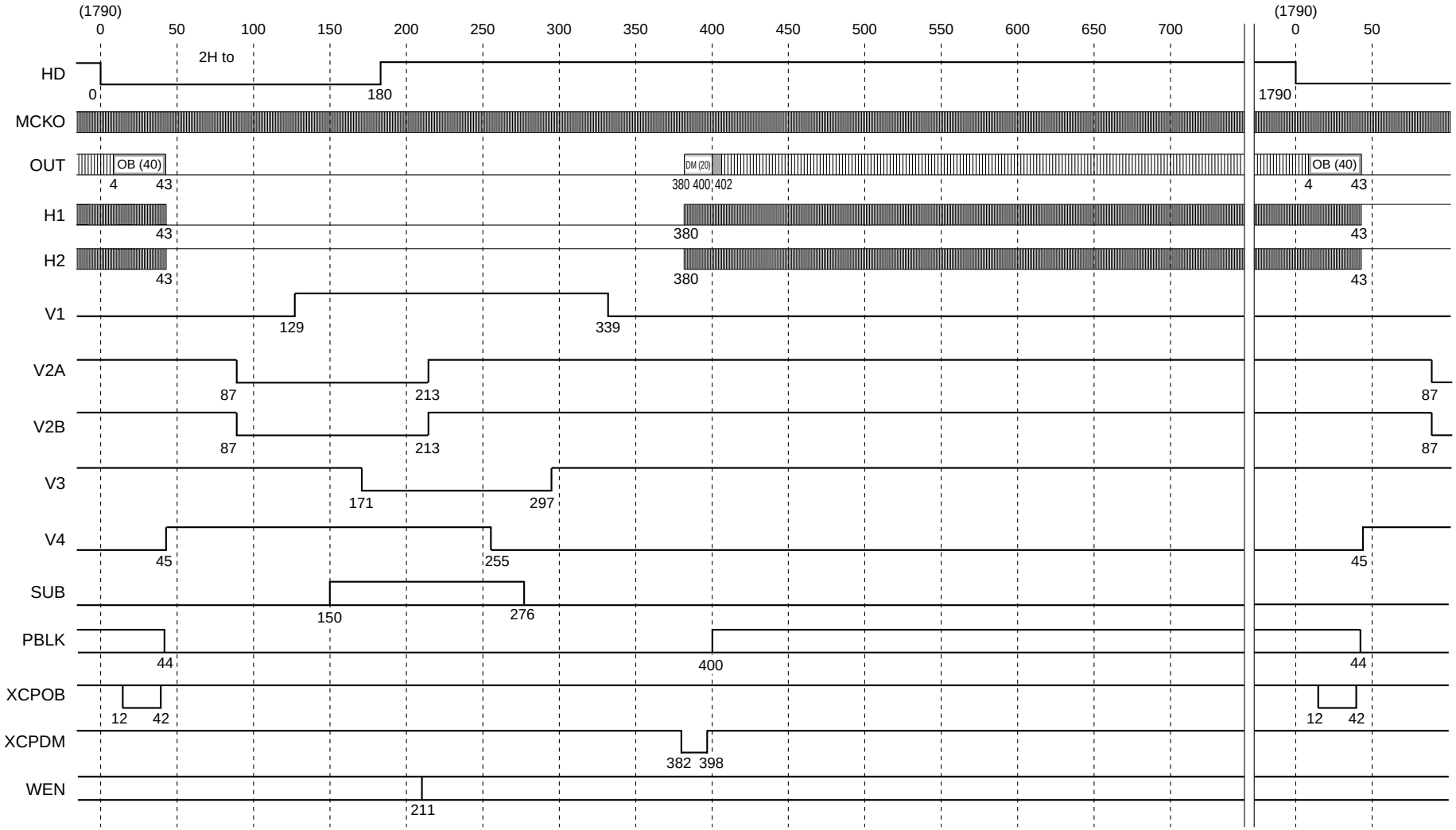


* The HD of this chart indicates the actual CXD3607R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

Chart-11 Horizontal Timing Chart

MODE

FINE/TRIGOUT mode normal transfer block

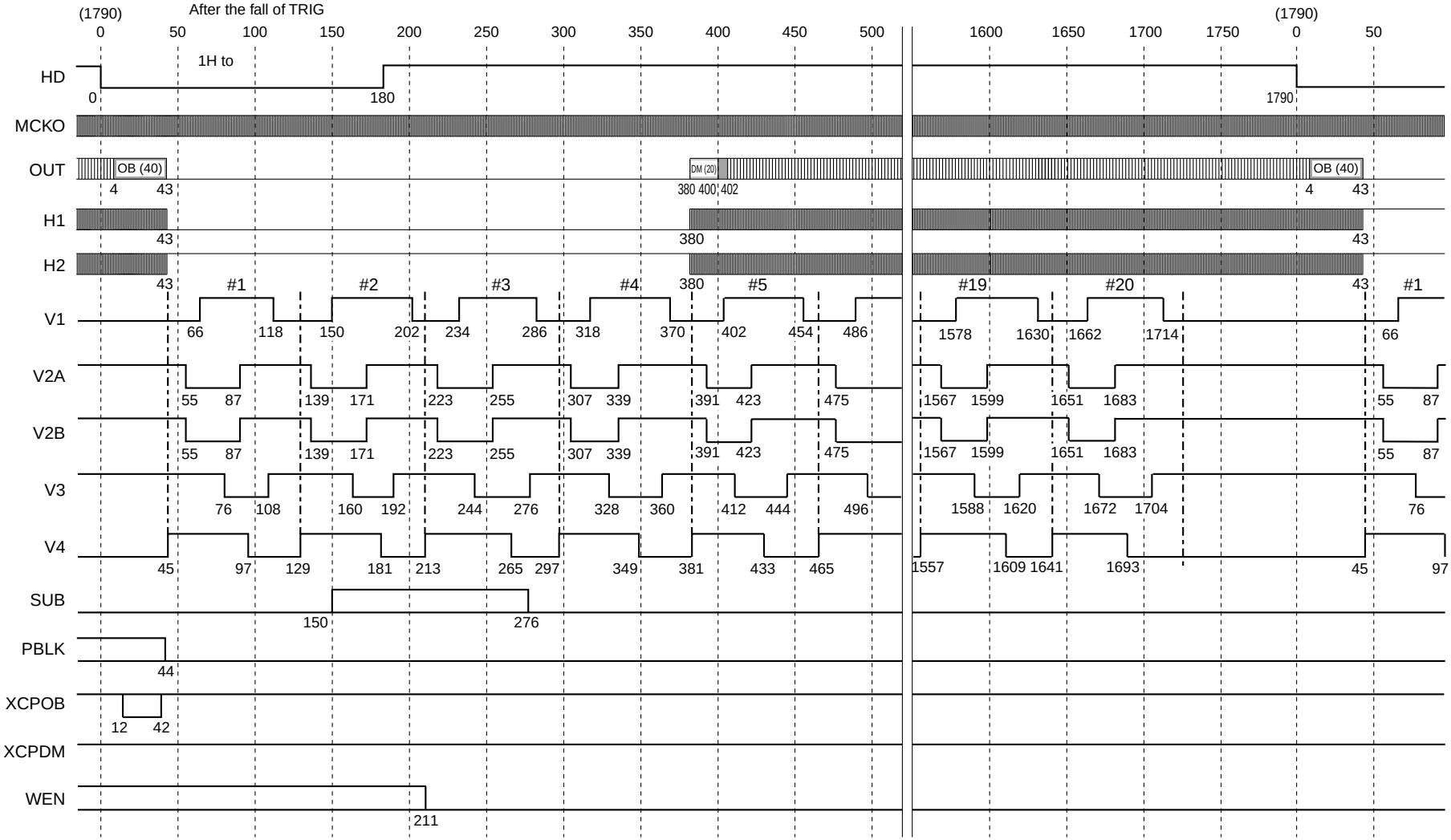


* The HD of this chart indicates the actual CXD3607R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

Chart-12 Horizontal Timing Chart

MODE

DRAFT mode → TRIG drive high-speed sweep block

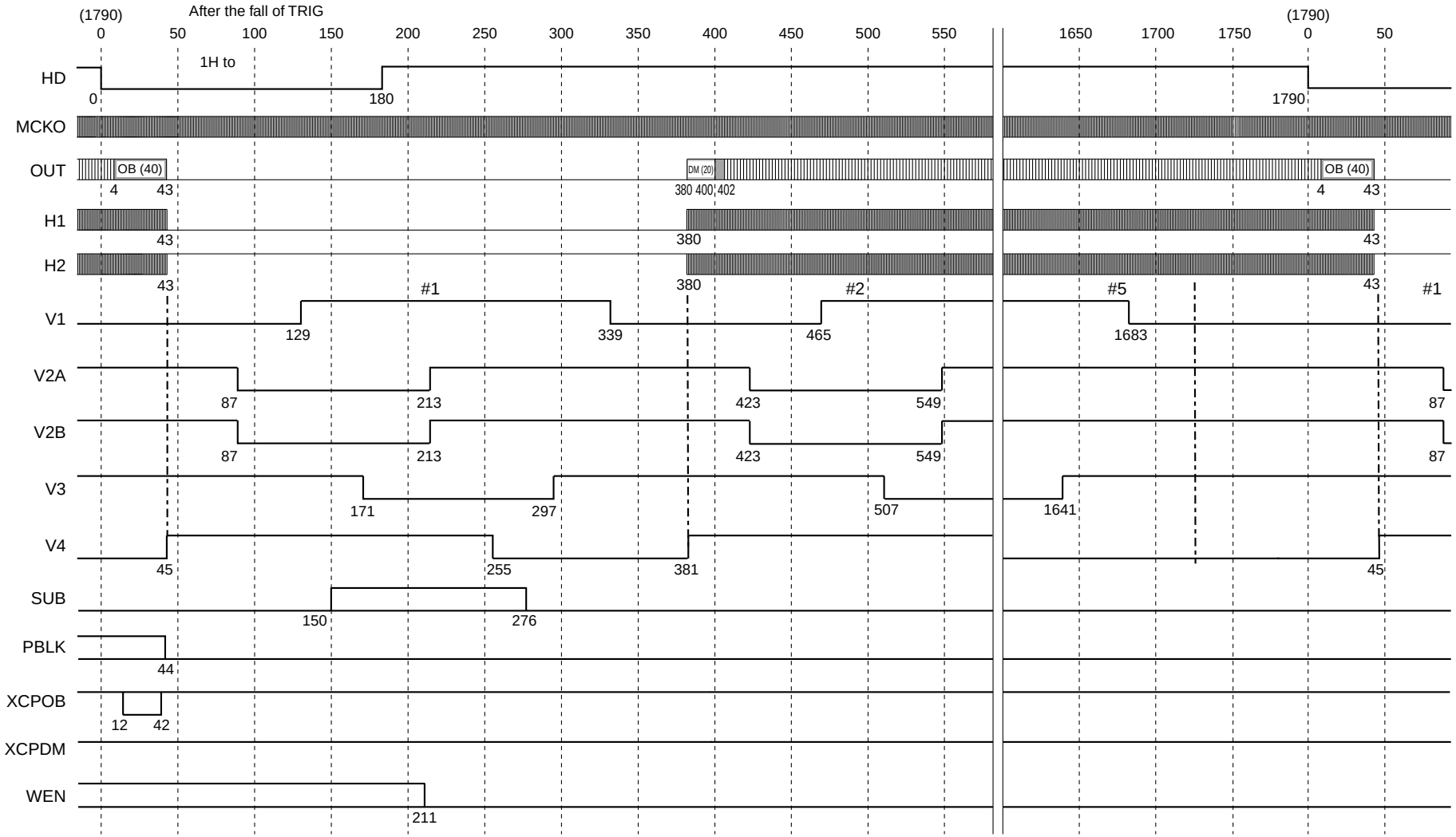


* The HD of this chart indicates the actual CXD3607R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

Chart-13 Horizontal Timing Chart

MODE

FINE/TRIGOUT mode → TRIG drive high-speed sweep block



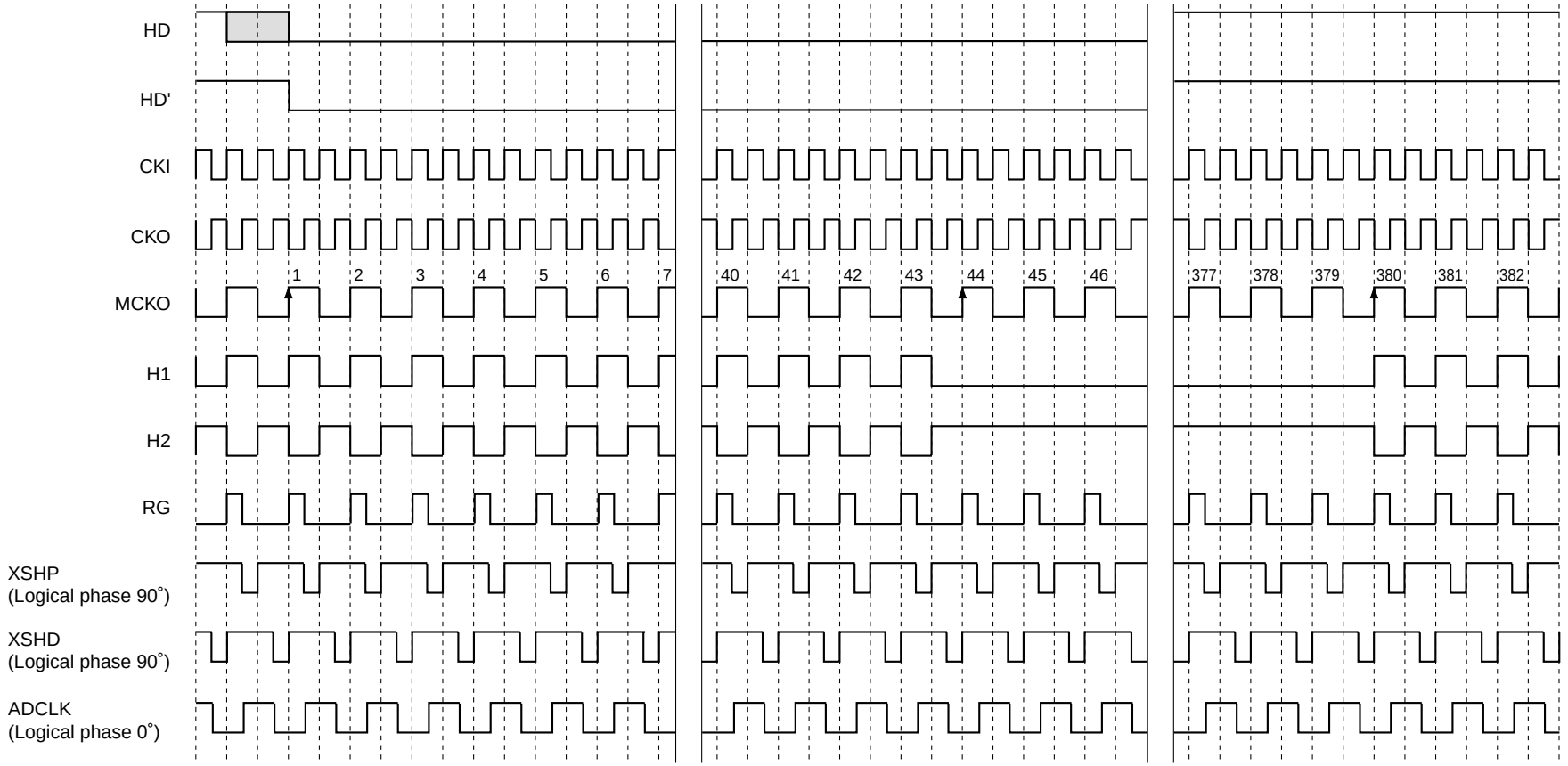
* The HD of this chart indicates the actual CXD3607R load timing.

* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.

Chart-14 High-Speed Phase Timing Chart

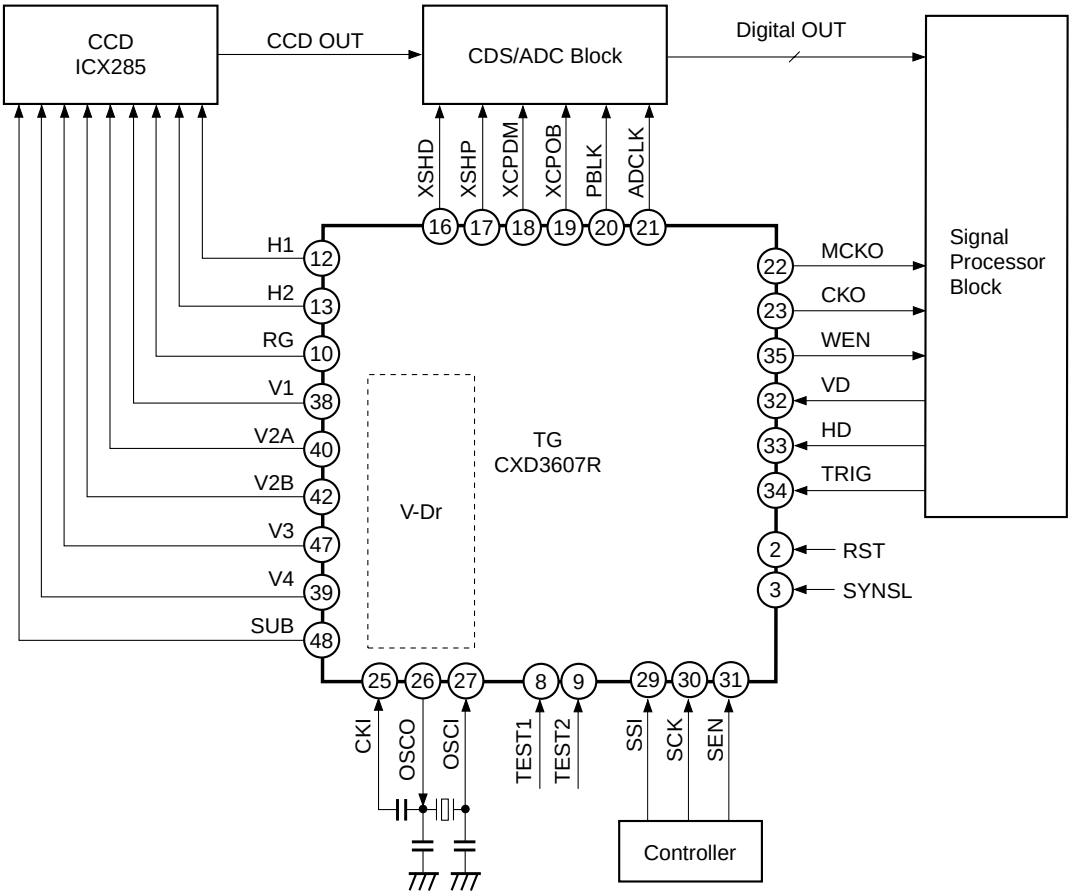
MODE

DRAFT/FINE/TRIGOUT mode



* HD' indicates the HD which is the actual CXD3607R load timing. (when MCKO sync is selected)
* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
* The logical phases of XSHP, XSHD and ADCLK can be specified by the serial interface data.

Application Circuit Block Diagram

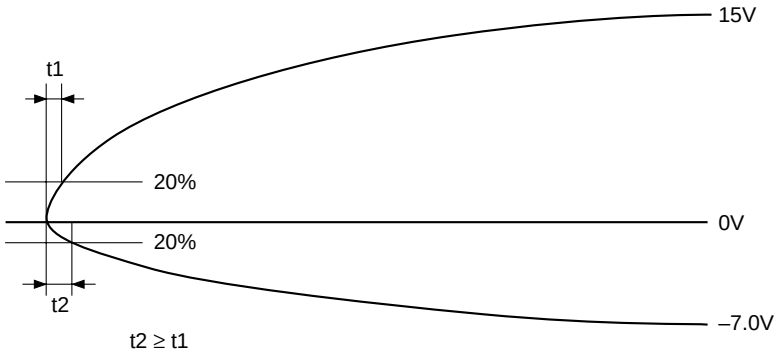


This block diagram shows the connection relationship with each block, and is not an actual circuit diagram.
See the CCD image sensor data sheet for a concrete example of circuit connection with a CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes for Power-on

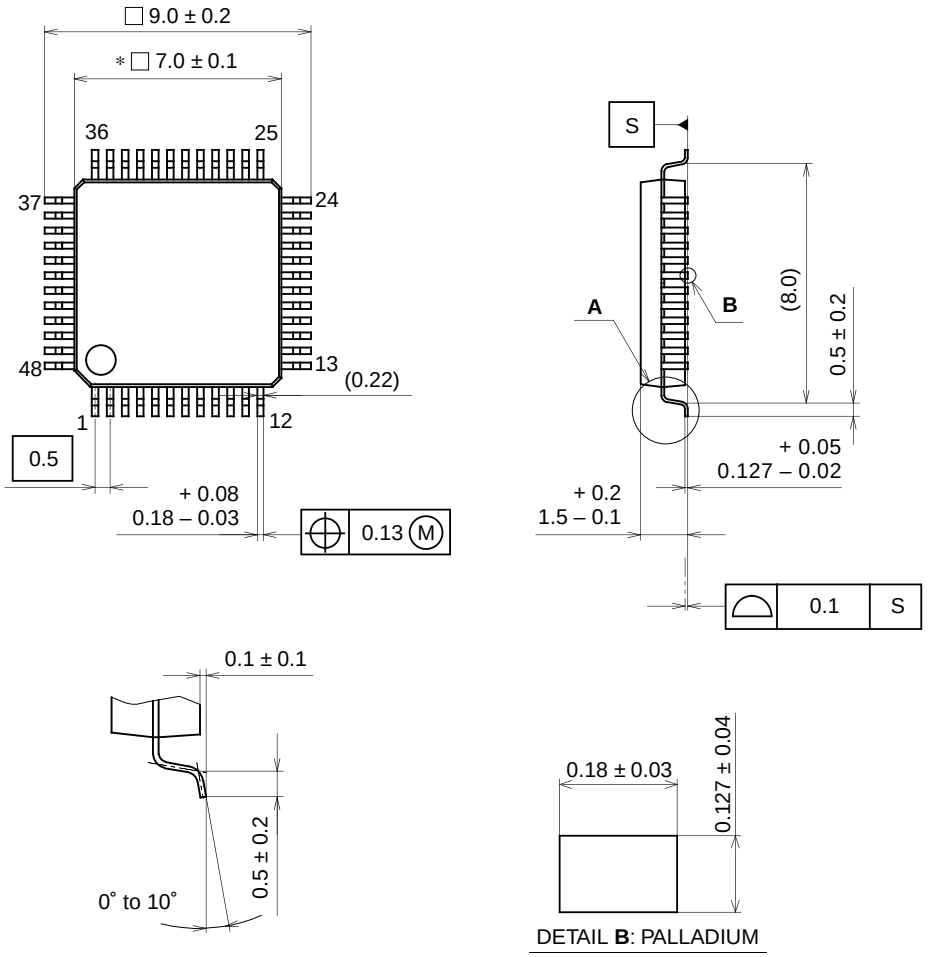
Of the four –7.0V, +15.0V, +3.3V, +5.0V power supplies, be sure to start up the –7.0V and +15.0V power supplies in the following order to prevent the SUB pin of the CCD image sensor from going to negative potential.



t2 ≥ t1

Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g