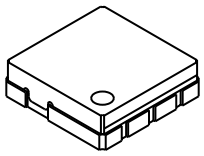
SONY

CXG1117K

Power Amplifier Module for JCDMA

8 pin LCC (Ceramic)



Description

The CXG1117K is the power amplifier module which operates at a single power supply. This IC is designed using the Sony's original p-Gate HFET process.

Features

- Single power supply operation:
  V_{DD1} = V_{DD2} = 3.5V (High mode),
  1.7V (Low mode),
  V_{GG} = 2.95V
- Ultrasmall package: 0.065cc (6.2mm × 6.2mm × 1.7mm)
- High efficiency: ηadd = 36.5% (@900MHz, P_{OUT} = 27.5dBm)
- Output power (high/low mode switching supported):
  P_{OUT} ≤ 19dBm: Low mode (V_{DD1} = V_{DD2} = 1.7V)
  P_{OUT} = 19 to 27.5dBm: High mode (V_{DD1} = V_{DD2} = 3.5V)
- Gain: Gp = 26dB (@900MHz)

Applications

Power amplifier for JCDMA system cellular phones

Structure

p-Gate HFET module

Recommended Operating Conditions

V_{DD} = 3.3 to 4.2V (High Mode)
1.7V (Low Mode)
V_{GG} = 2.95V±1%

Absolute Maximum Ratings

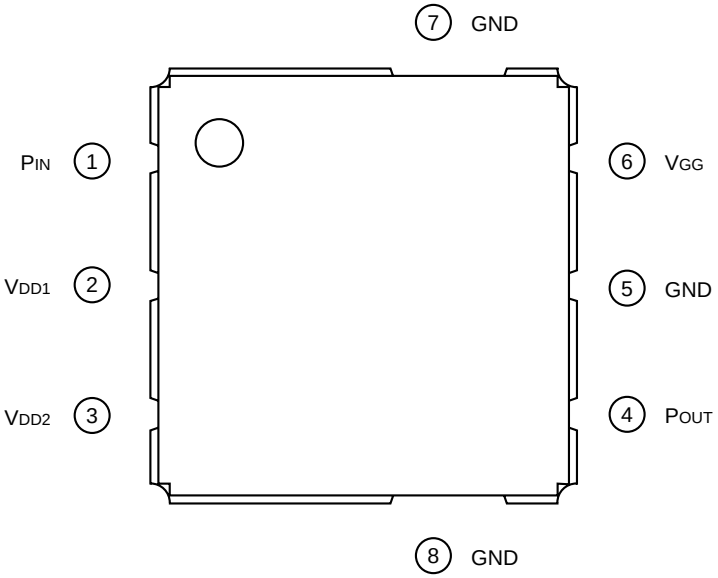
• Operating case temperature	Tcase	–30 to +85	°C
• Storage temperature	Tstg	–30 to +125	°C
• Bias voltage	V_{DD1}, V_{DD2}	6	V
• Bias voltage	V_{GG}	3.3 (V_{DD1} = V_{DD2} = 3.5V)	V
• Input power	P_{IN}	8	dBm

GaAs module is ESD sensitive devices. Special handling precautions are required.

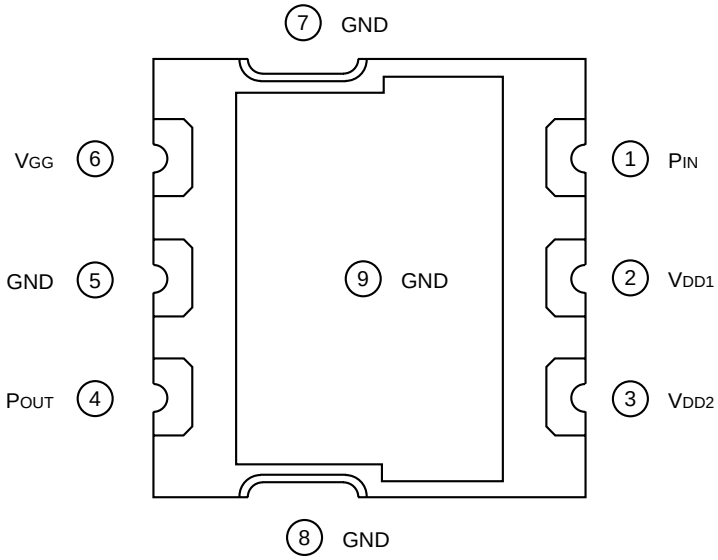
E01304A25-PS

package Outline/Pin Configuration

Front



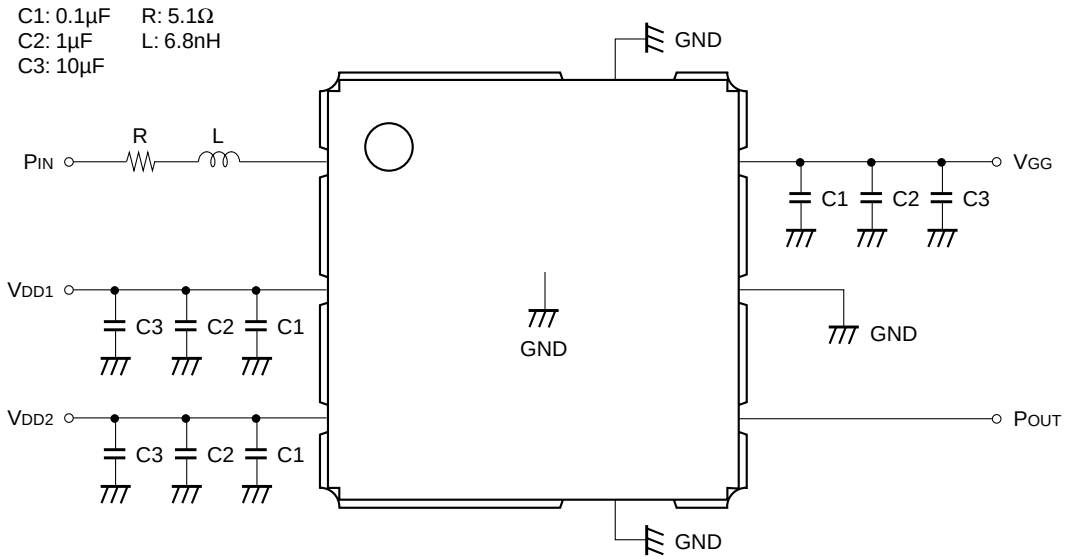
Back



Electrical Characteristics (ZS = ZL = 50Ω, IS-95 Modulation, Ta = 25°C)

Item	Conditions	Min.	Typ.	Max.	Unit
Frequency		887		925	MHz
Current consumption 1	P_{OUT} = 27.5dBm, V_{DD} = 3.5V, V_{GG} = 2.95V		440	475	mA
Current consumption 2	P_{OUT} = 14dBm, V_{DD} = 1.7V, V_{GG} = 2.95V		105	125	mA
Gain	P_{OUT} = 27.5dBm, V_{DD} = 3.5V, V_{GG} = 2.95V	24	26		dB
ACPR1 (High mode)	P_{OUT} = 27.5dBm, V_{DD} = 3.5V, V_{GG} = 2.95V, ±900kHz offset, 30kHz band width		–51	–45	dBc
ACPR2 (High mode)	P_{OUT} = 27.5dBm, V_{DD} = 3.5V, V_{GG} = 2.95V, ±1.98MHz offset, 30kHz band width		–59	–56	dBc
ACPR1 (Low mode)	P_{OUT} = 19dBm, V_{DD} = 1.7V, V_{GG} = 2.95V, ±900kHz offset, 30kHz band width		–53	–45	dBc
ACPR2 (Low mode)	P_{OUT} = 19dBm, V_{DD} = 1.7V, V_{GG} = 2.95V, ±1.98MHz offset, 30kHz band width		–60	–56	dBc
2nd, 3rd harmonics	P_{OUT} = 27.5dBm, V_{DD} = 3.5V, V_{GG} = 2.95V		–40	–30	dBc
Input VSWR	V_{DD} = 3.5V, V_{GG} = 2.95V		1.3	2.5	
Gate current	V_{GG} = 2.95V, $P_{OUT} \leq$ 27.5dBm		2.5	5	mA
Gain deviation for bias variation	V_{DD} = 3.5V → 1.7V V_{GG} = 2.95V, P_{OUT} = 17dBm		3	4.5	dB
Gain deviation within band	P_{OUT} = 27.5dBm, V_{DD} = 3.5V, V_{GG} = 2.95V		1.2	2	dB

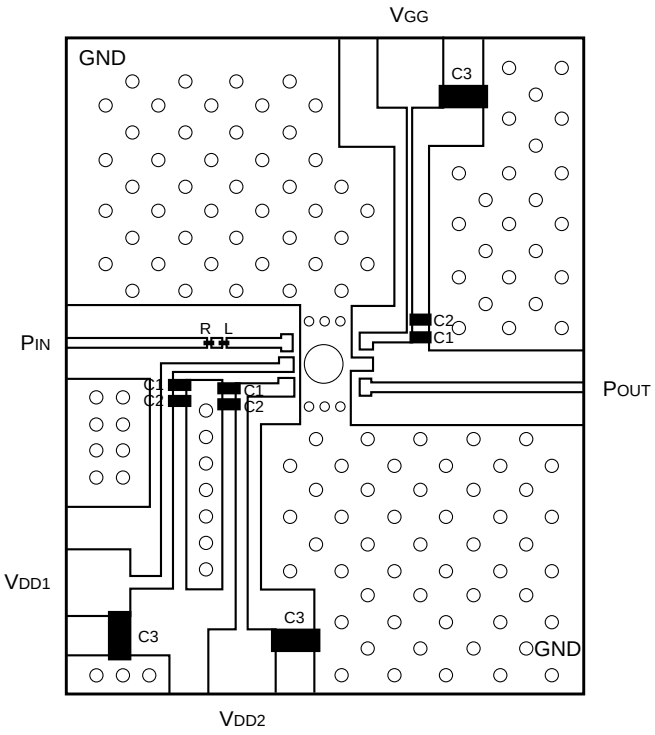
Recommended External Circuit



Recommended Evaluation Board

Board material: Glass fabric-base epoxy
Size: 40mm × 50mm × 0.6mm
Relative dielectric constant: 4.6

Front



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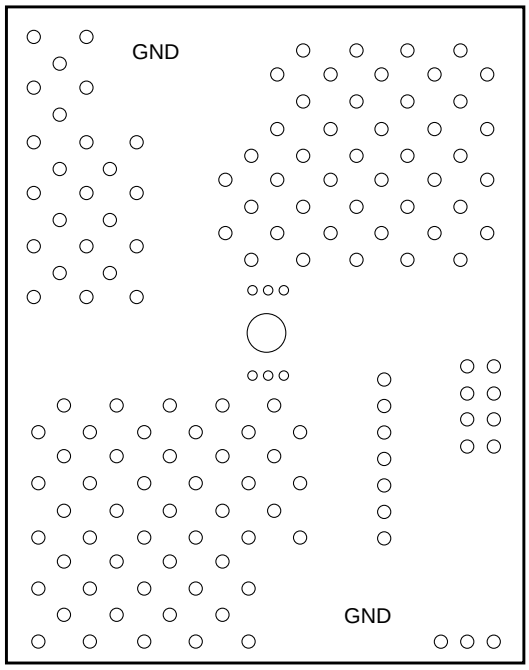
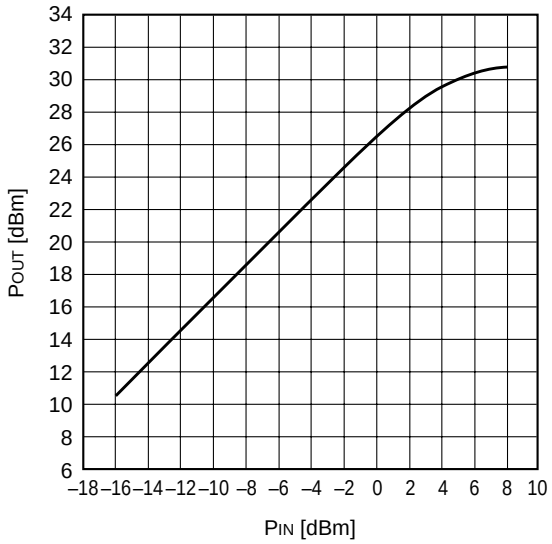


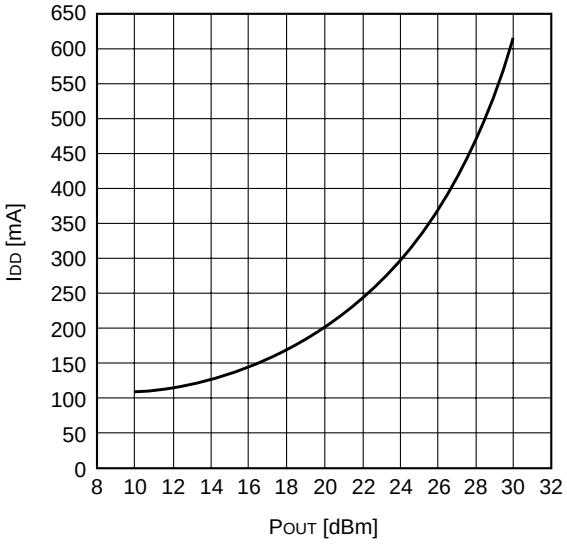
Example of Representative Characteristics

Conditions: f = 900MHz
V_{DD1} = V_{DD2} = 3.5V, V_{GG} = 2.95V
Ta = 25°C

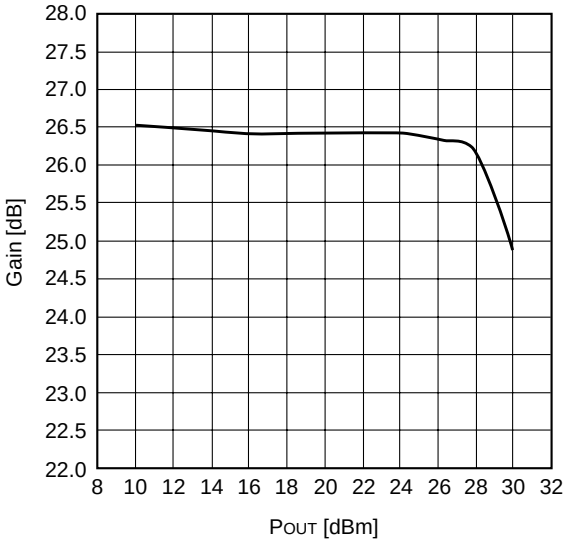
POUT vs. PIN



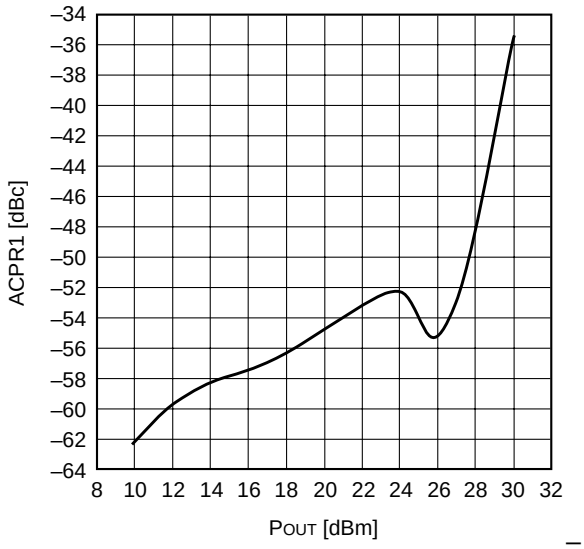
IDD vs. POUT



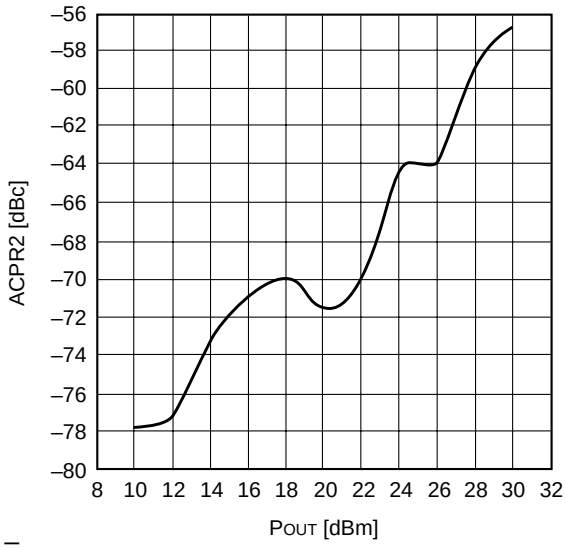
Gain vs. POUT



ACPR1 vs. POUT

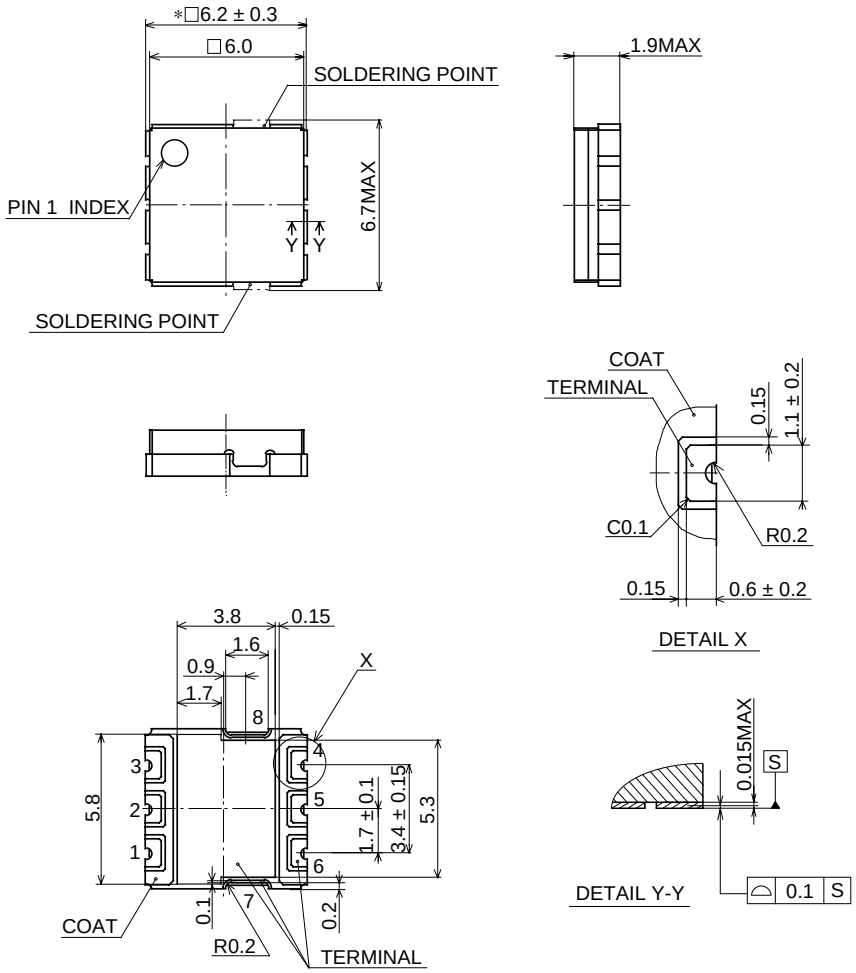


ACPR2 vs. POUT



Package Outline Unit: mm

8PIN LCC (Ceramic)



Dimension " ∗"dose not inculude cutting burr.

SONY CODE	LCC-8C-601
EIAJ CODE	————————
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.8g