

Triple Low Noise Amplifier/Dual Mixer

Description

The CXG1130AER is a triple low noise amplifier/dual mixer. This IC is designed using the Sony's GaAs J-FET process.

Features

- Single 3V power supply operation
- 2-pin control by the on-chip logic circuit
- High gain: $G_p = 16.5\text{dB}$ (LNA typ.)
 $G_c = 10\text{dB}$ (MIX typ.)
- Low noise figure: $NF = 1.5$ to 1.6dB (LNA typ.)
 $NF = 4.5\text{dB}$ (MIX typ.)
- Low LO input power operation
- 24-pin VQFN small package

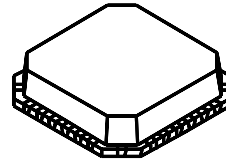
Applications

800MHz/1.5GHz Japan digital cellular phones (PDC)

Structure

GaAs J-FET MMIC

24 pin VQFN (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V _{DD}	4.5	V
• Input power	P _{IN}	+13	dBm
• Current consumption	I _{DD}	15	mA
• Operating temperature	T _{opr}	-35 to +85	°C
• Storage temperature	T _{stg}	-65 to +150	°C

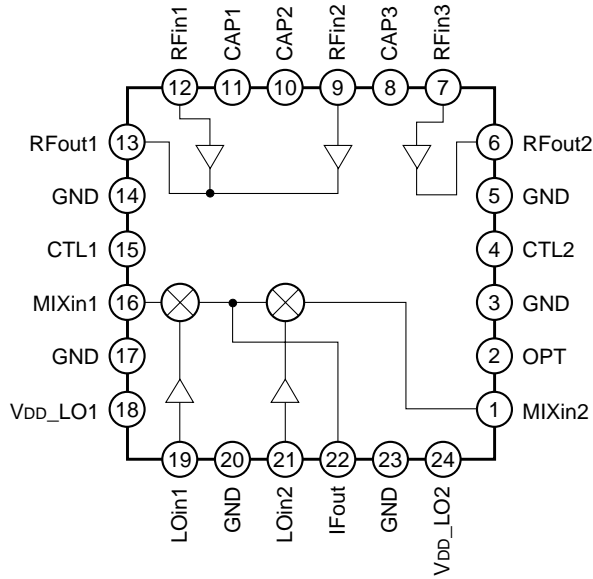
Recommended Operating Conditions

• Supply voltage	V _{DD}	2.7 to 3.3	V
• Control voltage	V _{CTL} (H)	2.4 to 3.3	V
	V _{CTL} (L)	0 to 0.3	V

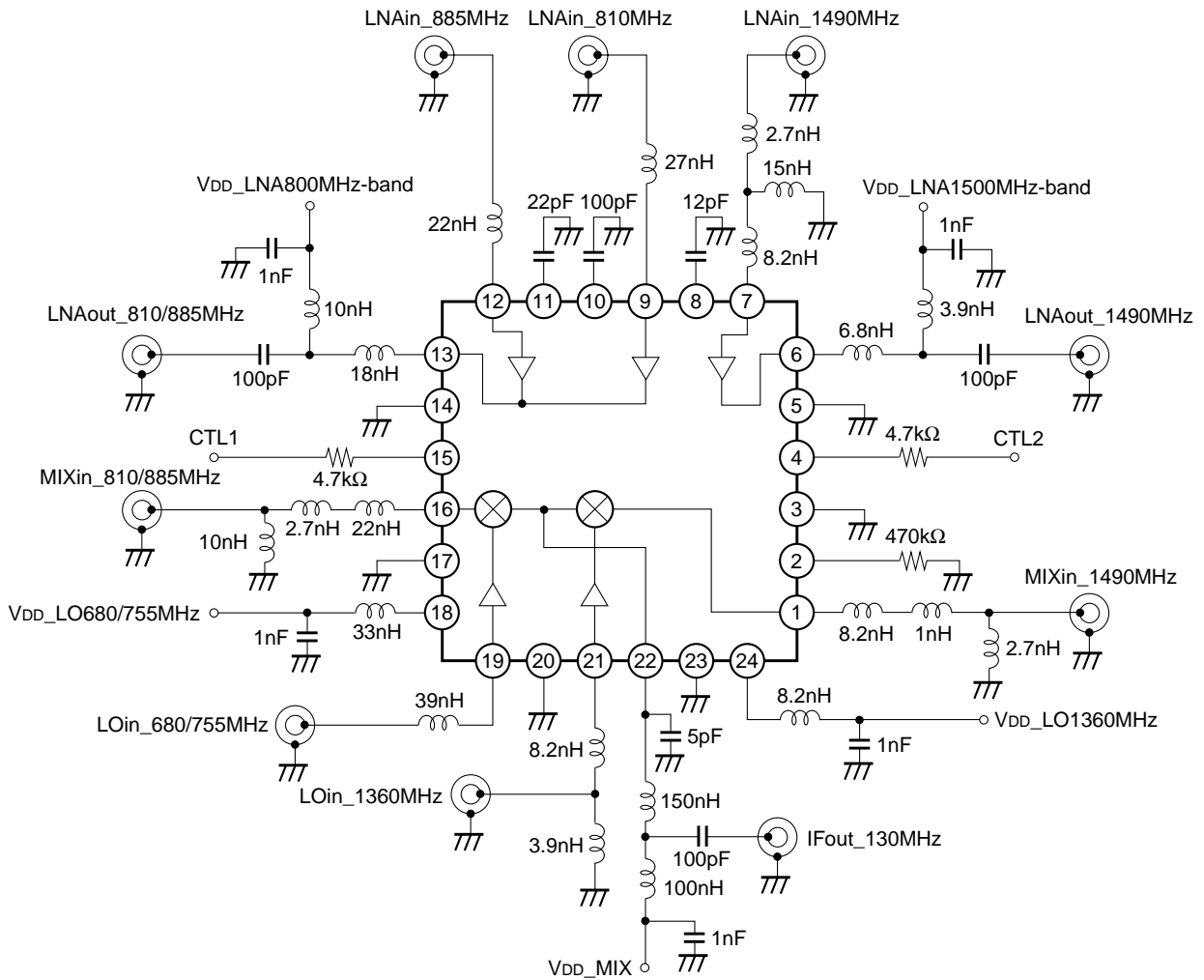
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

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Block Diagram and Pin Configuration



Recommended Evaluation Circuit



Electrical Characteristics

The normalized values are those when the Sony's recommended evaluation board is used.

800MHz Band Low Noise Amplifier

Conditions: Unless otherwise specified, $V_{DD} = 3.0V$, $V_{CTL} (H) = 3.0V$, $V_{CTL} (L) = 0V$, $f_{RF1} = 885MHz$, $f_{RF2} = 810MHz$
($T_a = 25^{\circ}C$)

Item	Symbol	Path	Frequency	V_{CTL1}	V_{CTL2}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I _{DD}	—	—	H	L	—	2.0	2.65	mA	When no signal
			—	L	L	—	2.0	2.65		
Control current	I _{CTL1}	—	—	H	L	—	60	90	μA	
			—	L	L	-5	0	5		
Power gain	G _p	RF _{IN1} → RF _{OUT1}	f _{RF1}	H	L	14.5	16.5	18.5	dB	When a small signal
				L	L	—	-20	-15		
		RF _{IN2} → RF _{OUT1}	f _{RF2}	H	L	—	-25	-20		
				L	L	14.5	16.5	18.5		
Noise figure	NF	RF _{IN1} → RF _{OUT1}	f _{RF1}	H	L	—	1.3	2.0	dB	
		RF _{IN2} → RF _{OUT1}	f _{RF2}	L	L	—	1.5	2.0		
Input IP3	IIP3	RF _{IN1} → RF _{OUT1}	f _{RF1}	H	L	-10	-6.5	—	dBm	*1
		RF _{IN2} → RF _{OUT1}	f _{RF2}	L	L	-11	-8	—		
Isolation	Iso	RF _{OUT1} → RF _{IN1}	f _{RF1}	H	L	22	26	—	dB	When a small signal
		RF _{OUT1} → RF _{IN2}	f _{RF2}	L	L	18	22	—		

*1 Conversion from the IM3 suppression ratio for two-wave input: $f_{RFOffset} = 100kHz$, $P_{RF} = -30dBm$.

1.5GHz Band Low Noise Amplifier

Conditions: Unless otherwise specified, $V_{DD} = 3.0V$, $V_{CTL} (H) = 3.0V$, $V_{CTL} (L) = 0V$, $f_{RF3} = 1490MHz$
($T_a = 25^{\circ}C$)

Item	Symbol	Path	Frequency	V_{CTL1}	V_{CTL2}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I _{DD}	—	—	—	H	—	2.9	3.7	mA	When no signal
Control current	I _{CTL2}	—	—	—	H	—	90	120	μA	
Power gain	G _p	RF _{IN3} → RF _{OUT2}	f _{RF3}	—	H	14	16	18	dB	When a small signal
Noise figure	NF	RF _{IN3} → RF _{OUT2}	f _{RF3}	—	H	—	1.6	2.1	dB	
Input IP3	IIP3	RF _{IN3} → RF _{OUT2}	f _{RF3}	—	H	-9	-6	—	dBm	*1
Isolation	Iso	RF _{OUT2} → RF _{IN3}	f _{RF3}	—	H	20	23	—	dB	When a small signal

*1 Conversion from the IM3 suppression ratio for two-wave input: $f_{RFOffset} = 100kHz$, $P_{RF} = -30dBm$.

800MHz Band Mixer

Conditions: Unless otherwise specified, $V_{DD} = 3.0V$, $V_{CTL} (H) = 3.0V$, $V_{CTL} (L) = 0V$,

$f_{RF1} = 885MHz$, $f_{RF2} = 810MHz$, $f_{LO} = f_{RF} - 130MHz$, $P_{LO} = -15dBm$

($T_a = 25^{\circ}C$)

Item	Symbol	RF frequency	V _{CTL1}	V _{CTL2}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I _{DD}	—	—	L	—	5	6.5	mA	When no signal
Control current	I _{CTL2}	—	—	L	-5	0	5	μA	
Conversion gain	G _c	f _{RF1}	—	L	9	10	11.5	dB	When a small signal
		f _{RF2}	—	L	8.5	9.5	11		
Noise figure	NF	f _{RF1}	—	L	—	5	6.5	dB	
		f _{RF2}	—	L	—	4	5.5		
Input IP3	IIP3	f _{RF1}	—	L	-1	+2	—	dBm	*1
		f _{RF2}	—	L	-0.5	+2.5	—		
LO → RF leak	PI _k	f _{RF1}	—	L	—	-21	-18	dBm	f _{LO} = 755MHz
		f _{RF2}	—	L	—	-24	-21		f _{LO} = 680MHz

*1 Conversion from the IM3 suppression ratio for two-wave input: $f_{RfOffset} = 100kHz$, $P_{RF} = -25dBm$.

1.5GHz Band Mixer

Conditions: Unless otherwise specified, $V_{DD} = 3.0V$, $V_{CTL} (H) = 3.0V$, $V_{CTL} (L) = 0V$,

$f_{RF3} = 1490MHz$, $f_{LO} = 1360MHz$, $P_{LO} = -15dBm$

($T_a = 25^{\circ}C$)

Item	Symbol	RF frequency	V _{CTL1}	V _{CTL2}	Min.	Typ.	Max.	Unit	Measurement condition
Current consumption	I _{DD}	—	—	H	—	5.5	7.5	mA	When no signal
Control current	I _{CTL2}	—	—	H	—	90	120	μA	
Conversion gain	G _c	f _{RF3}	—	H	9	10	11.5	dB	When a small signal
Noise figure	NF	f _{RF3}	—	H	—	4.5	6	dB	
Input IP3	IIP3	f _{RF3}	—	H	-1	+2	—	dBm	*1
LO → RF leak	PI _k	f _{RF3}	—	H	—	-24	-21	dBm	f _{LO} = 1360MHz

*1 Conversion from the IM3 suppression ratio for two-wave input: $f_{RfOffset} = 100kHz$, $P_{RF} = -25dBm$.

Operation Logic

V _{CTL1}	V _{CTL2}	LNA1 (800MHz_U)	LNA2 (800MHz_L)	LNA3 (1.5GHz)	MIX1 (800MHz)	MIX2 (1.5GHz)
H	L	ON	OFF	OFF	ON	OFF
L	L	OFF	ON	OFF	ON	OFF
—	H	OFF	OFF	ON	OFF	ON

Example of Representative Characteristics

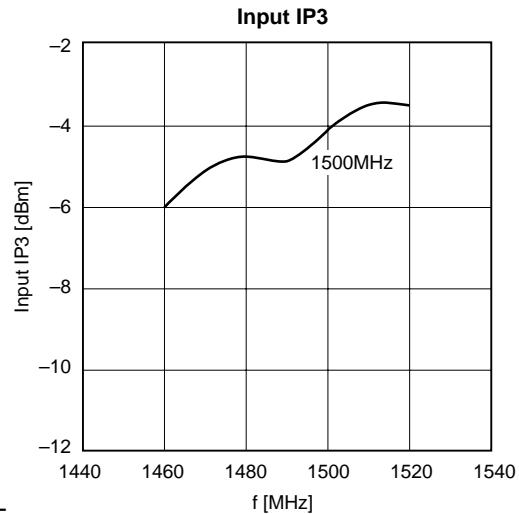
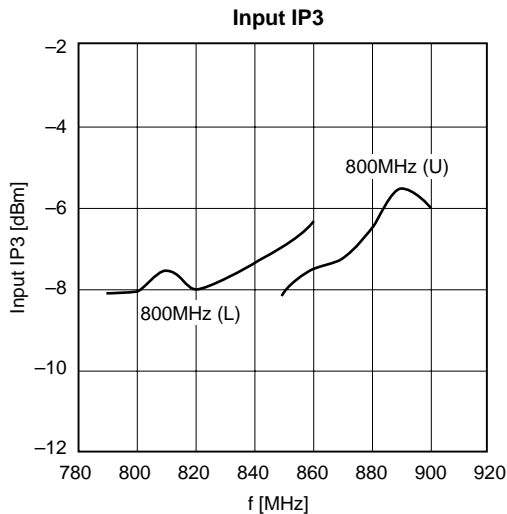
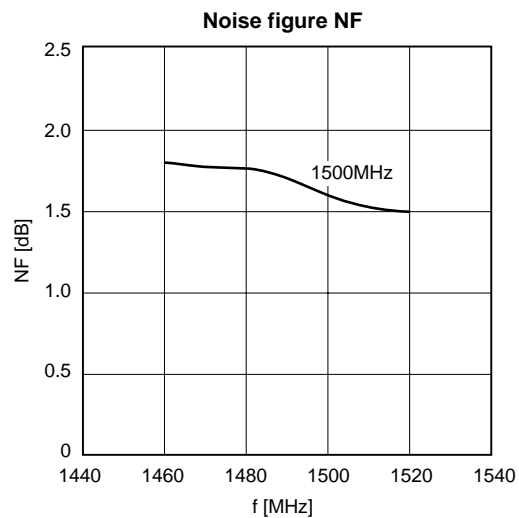
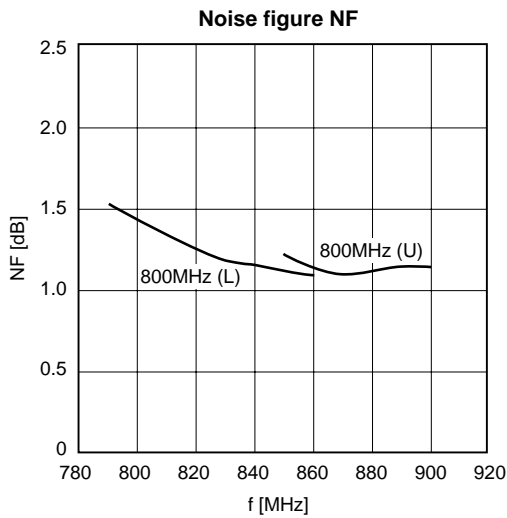
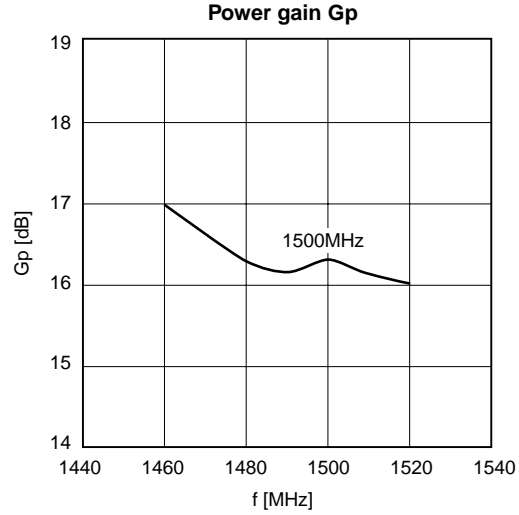
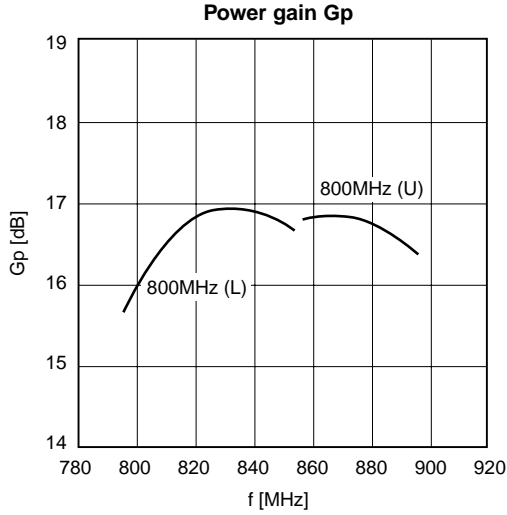
1. CXG1130AER frequency characteristics of main items in LNA block (25°C)

[Condition] $V_{DD} = 3V$, 800MHz_L (Pin 9 input → Pin 13 output): $V_{CTL1} = 0V$, $V_{CTL2} = 0V$,

800MHz_U (Pin 12 input → Pin 13 output): $V_{CTL1} = 3V$, $V_{CTL2} = 0V$,

1500MHz (Pin 7 input → Pin 6 output): $V_{CTL2} = 3V$

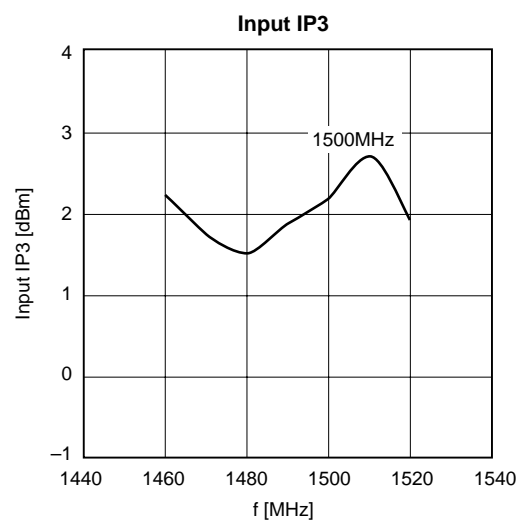
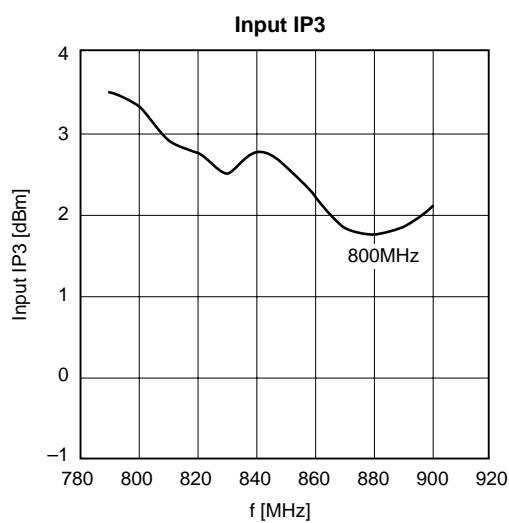
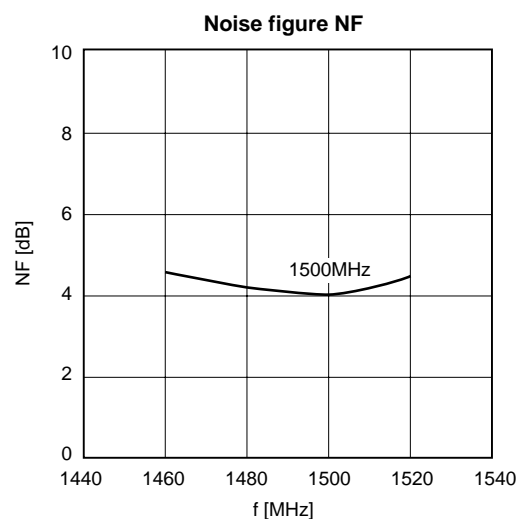
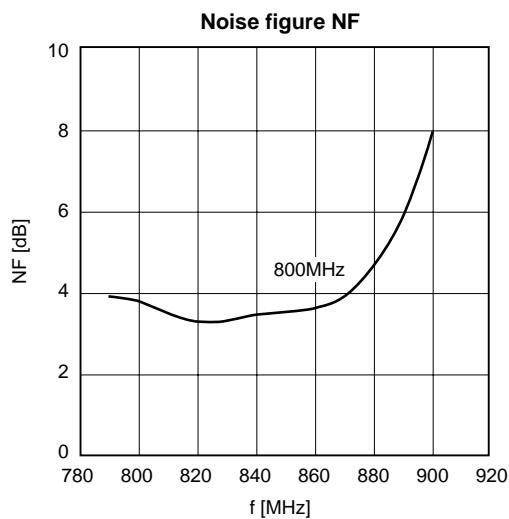
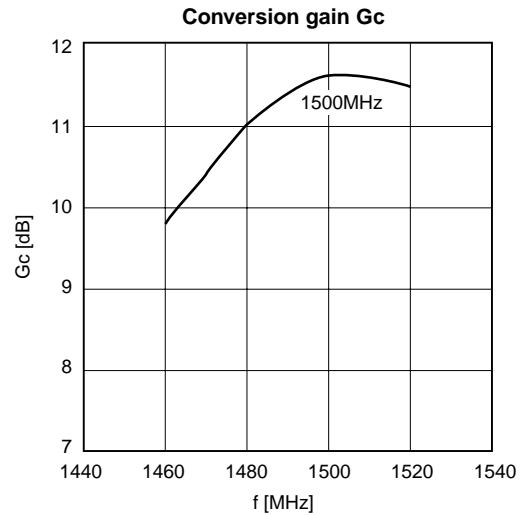
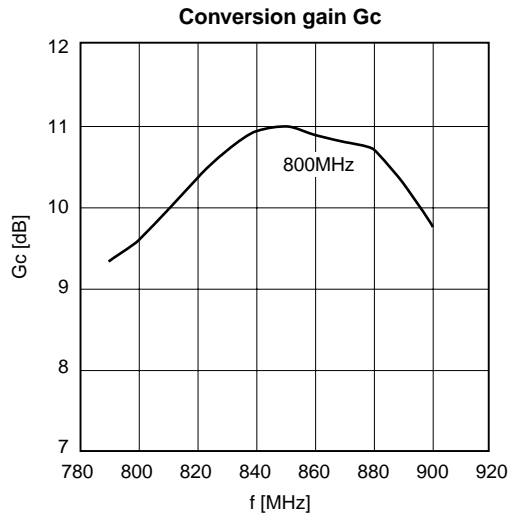
G_p and NF are those when a small signal is input. The input $IP3$ is converted from the IM3 suppression ratio for two-wave input: $f_{roffset} = 100kHz$, $P_{RF} = -30dBm$.



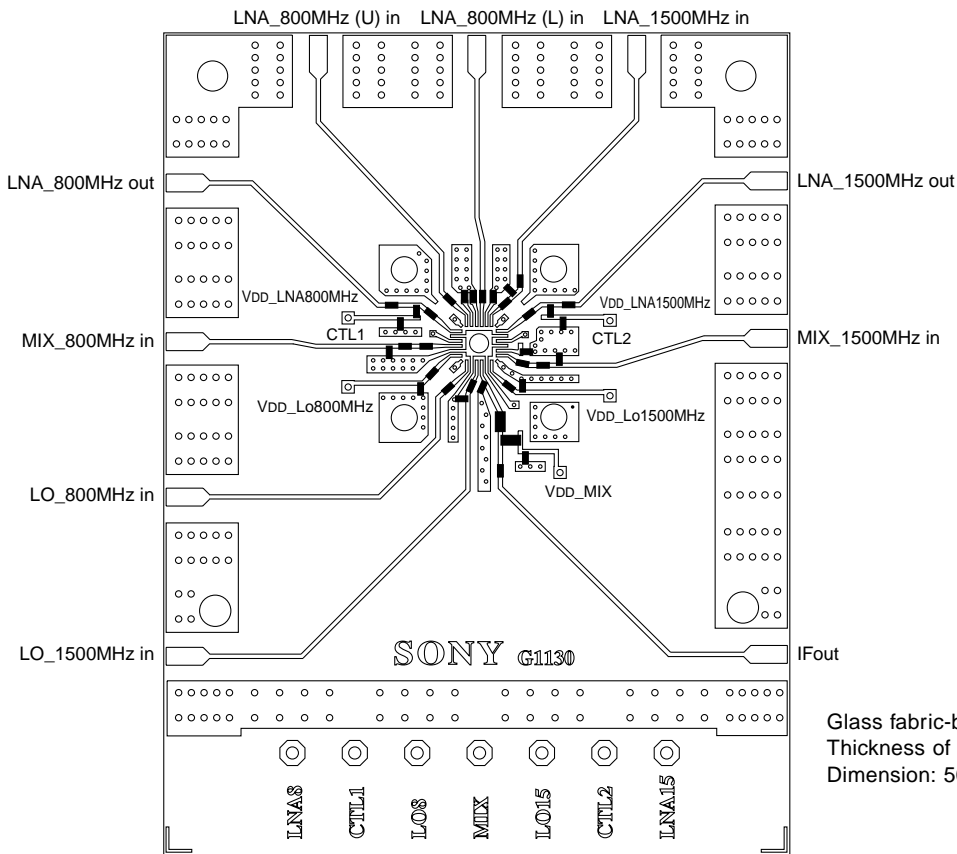
2. CXG1130AER frequency characteristics of main items in MIX block (25°C)

[Condition] $V_{DD} = 3V$, $f_{LO} = f_{RF} - 130MHz$, $P_{LO} = -15dBm$, 800MHz: $V_{CTL2} = 0V$, 1500MHz: $V_{CTL2} = 3V$

G_c and NF are those when a small signal is input. The input IP_3 is converted from the IM_3 suppression ratio for two-wave input: $f_{RFoffset} = 100kHz$, $P_{RF} = -25dBm$.

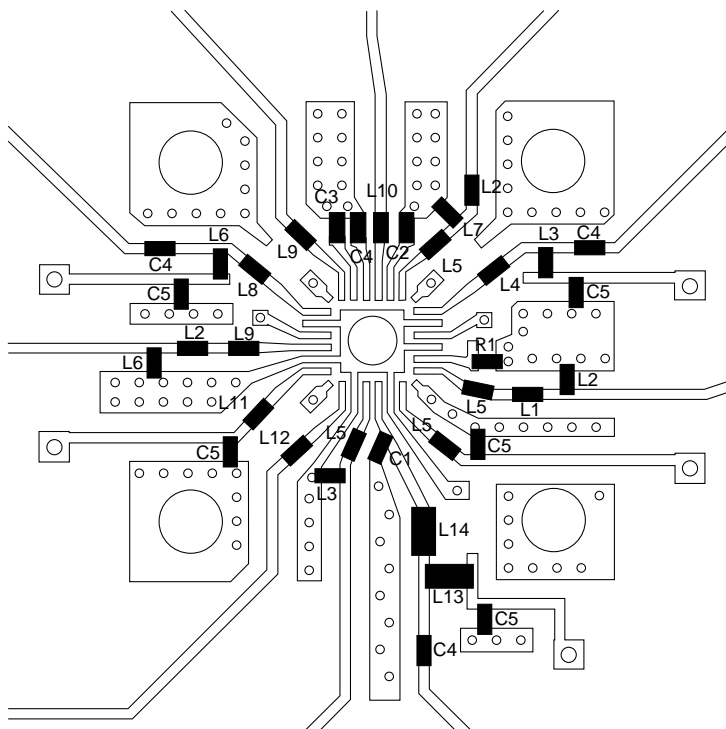


Recommended Evaluation Board



Glass fabric-base 4-layer epoxy board
 Thickness of film between layers 1 and 2: 0.2mm
 Dimension: 50mm x 66mm

Enlarged Diagram of External Circuit Block

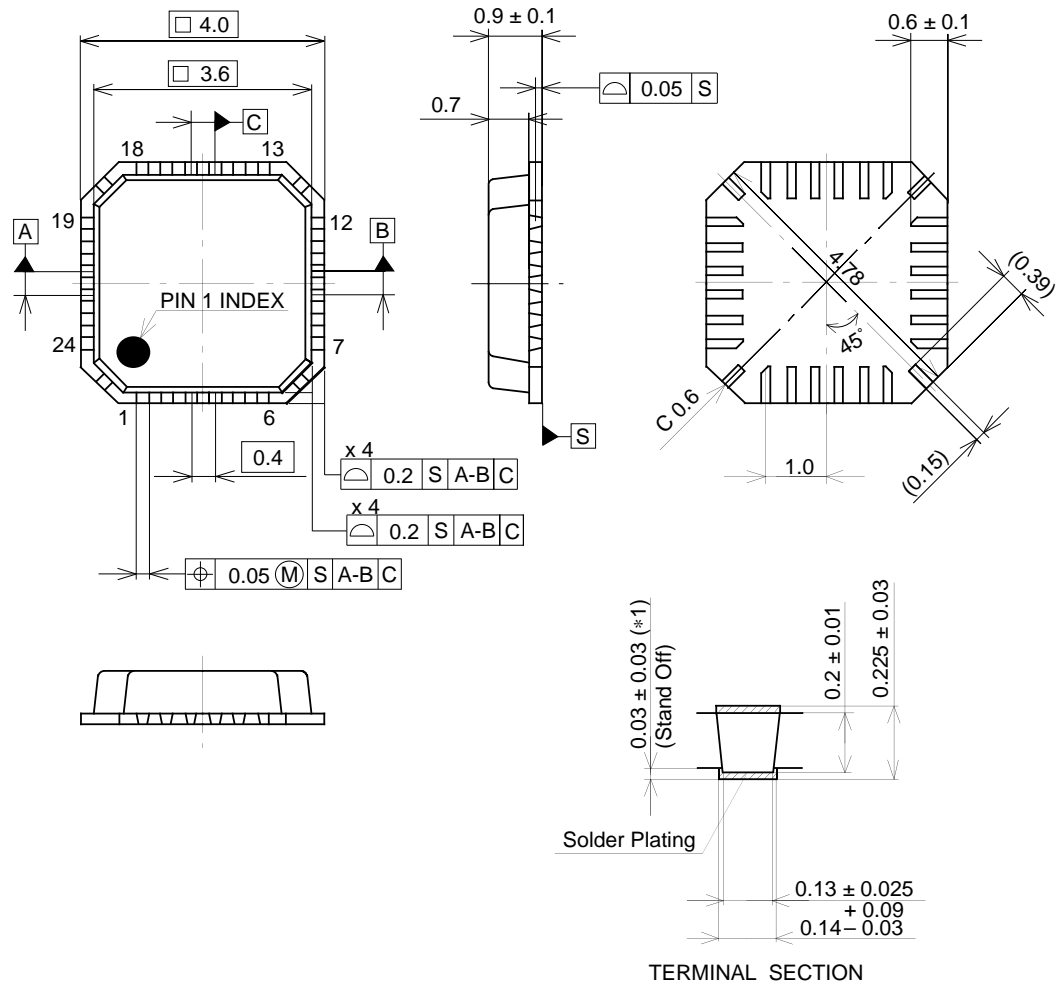


- L1 = 1nH
- L2 = 2.7nH
- L3 = 3.9nH
- L4 = 6.8nH
- L5 = 8.2nH
- L6 = 10nH
- L7 = 15nH
- L8 = 18nH
- L9 = 22nH
- L10 = 27nH
- L11 = 33nH
- L12 = 39nH
- L13 = 100nH
- L14 = 150nH
- C1 = 5pF
- C2 = 12pF
- C3 = 22pF
- C4 = 100pF
- C5 = 1nF
- R1 = 470Ω

Series resistors of 4.7kΩ to CTL1 and CTL2 are attached on the solder side of the board.

Package Outline Unit: mm

24PIN VQFN(PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

SONY CODE	VQFN-24P-03
EIAJ CODE	_____
JEDEC CODE	_____

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER PLATING	Sn-Bi Bi:1-4wt%
LEAD TREATMENT THICKNESS	5-18μm