SONY

CXP971000

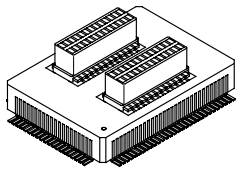
CMOS 16-bit Single Chip Microcomputer

Piggy/ evaluation type

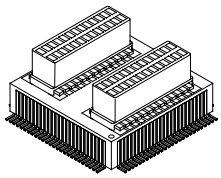
Description

The CXP971000 is a CMOS 16-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP972032/973032/973064.

100 pin PQFP (Ceramic)



(QFP supported)



(LQFP supported)

Features

- An efficient instruction set as a controller
  - Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
  - Highly quadratic instruction system, general-purpose register of eight 16-bit × 16-bank configuration
- Minimum instruction cycle time 50ns at 40MHz operation (2.7 to 3.6V)
- Incorporated EPROM CXP27V1000K
- Incorporated RAM capacity 23.5K bytes
- Peripheral functions
  - — A/D converter: 8-bit 12-analog input, successive approximation system, 3-stage FIFO (Conversion time: 1.55µs at 40MHz)
  - — Serial interface: Asynchronous serial interface (UART) 128-byte buffer RAM, 3 channels
  - — I^2C bus interface: 64-byte buffer RAM (supports master/slave and automatic transfer mode)
  - — Timers: 8-bit timer/counter, 2 channels (with timing output) 16-bit capture timer/counter (with timing output) 16-bit timer, 4 channels, watchdog timer
  - — PWM output circuit: 14-bit PWM, 4 channels (2-channel of binary output switch function by PPG)
  - — Programmable pattern generator: 16-bit output, 64-byte buffer RAM, 1 channel
  - — Remote control receive circuit: 8-bit pulse measurement counter, 10-stage FIFO
  - — Parallel interface: External register interface (8-bit parallel bus), 4-chip select
- Interruption 33 factors, 33 vectors, multi-interruption and priority selection possible
- Standby mode Sleep/stop
- Package 100-pin Ceramic PQFP
- Mask ROM CXP972032/973032/973064
- FLASH EEPROM incorporated type CXP973F064

Structure

Silicon gate CMOS IC

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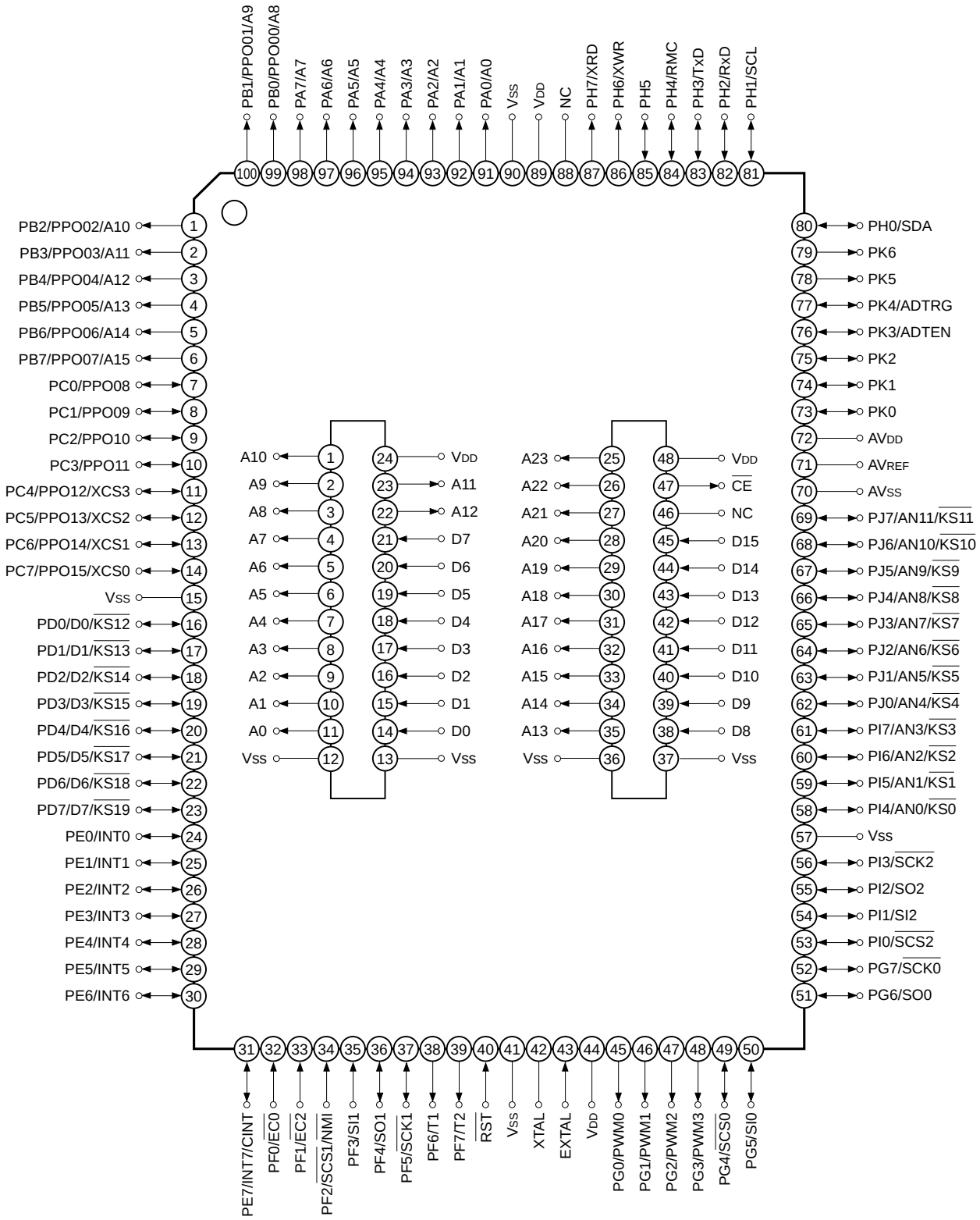
E00423A08-PS

Pin Assignment in Piggyback Mode (Top View) 100-pin QFP package

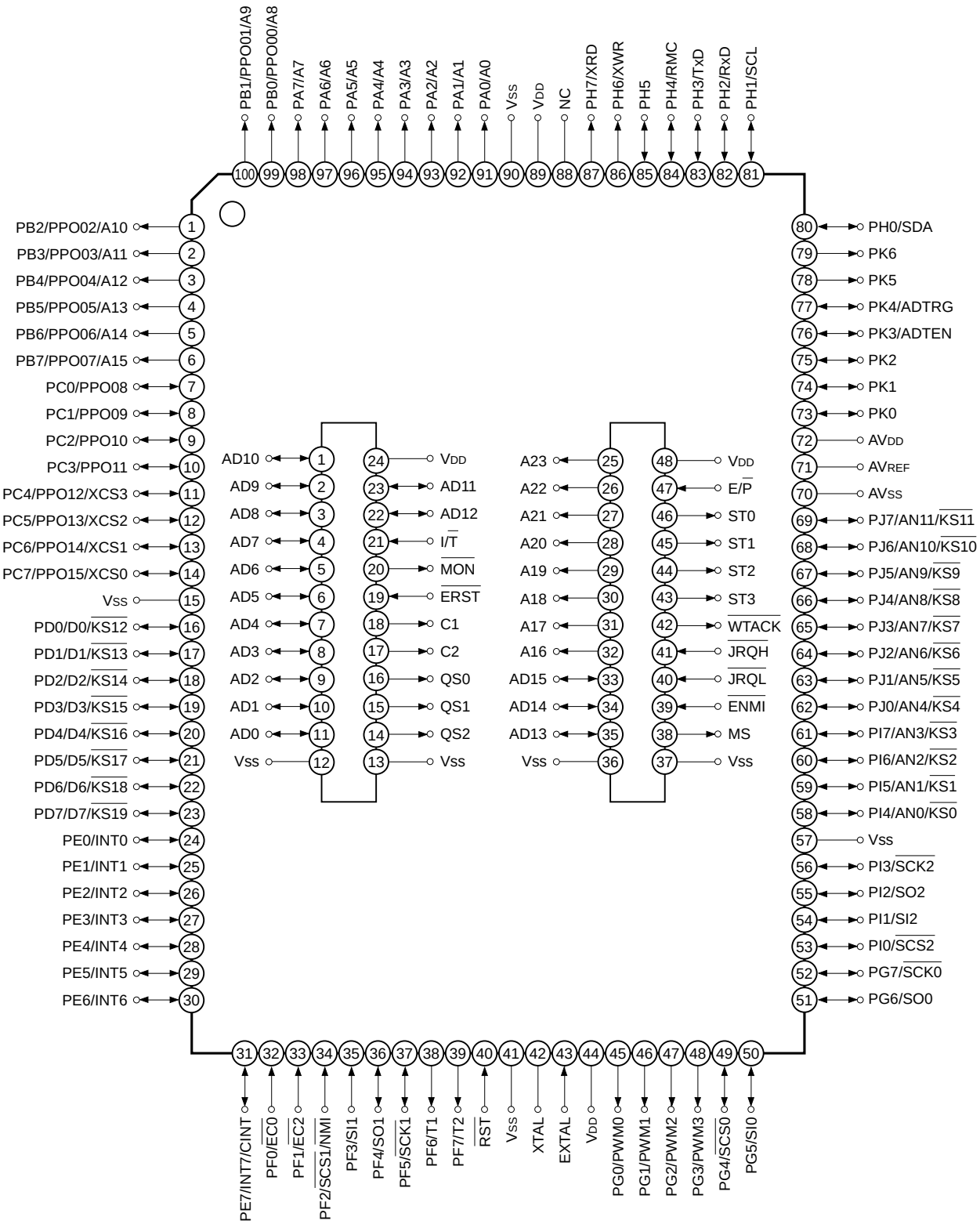


Note) 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.

2. Vss and AVss (Pins 15, 41, 57, 70 and 90) must be connected to GND.

3. V_{DD} and AV_{DD} (Pins 44, 72 and 89) must be connected to V_{DD}.

Pin Assignment in Evaluator Mode (Top View) 100-pin QFP package

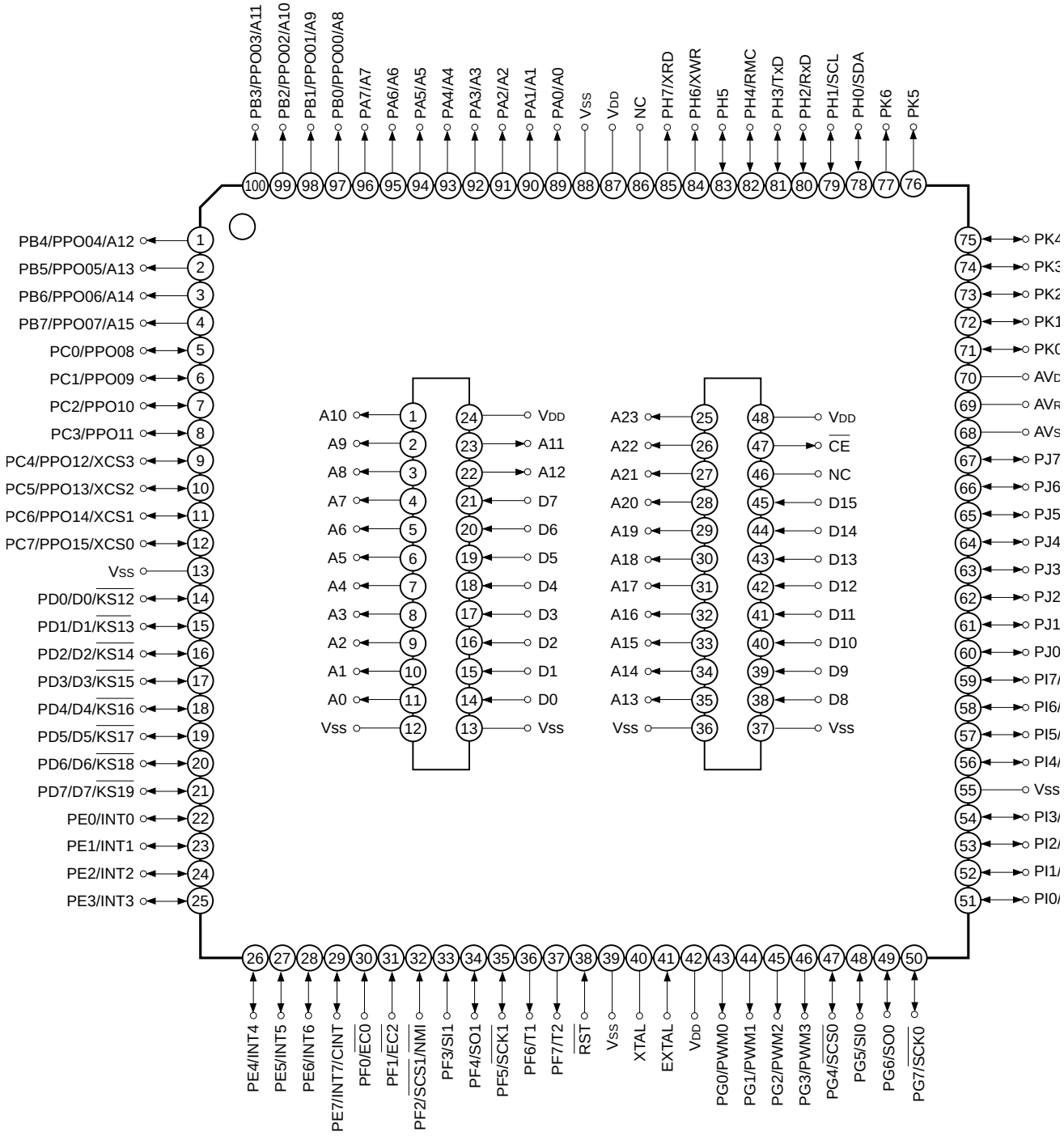


Note) 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.

2. Vss and AVss (Pins 15, 41, 57, 70 and 90) must be connected to GND.

3. V_{DD} and AV_{DD} (Pins 44, 72 and 89) must be connected to V_{DD}.

Pin Assignment in Piggyback Mode (Top View) 100-pin LQFP package

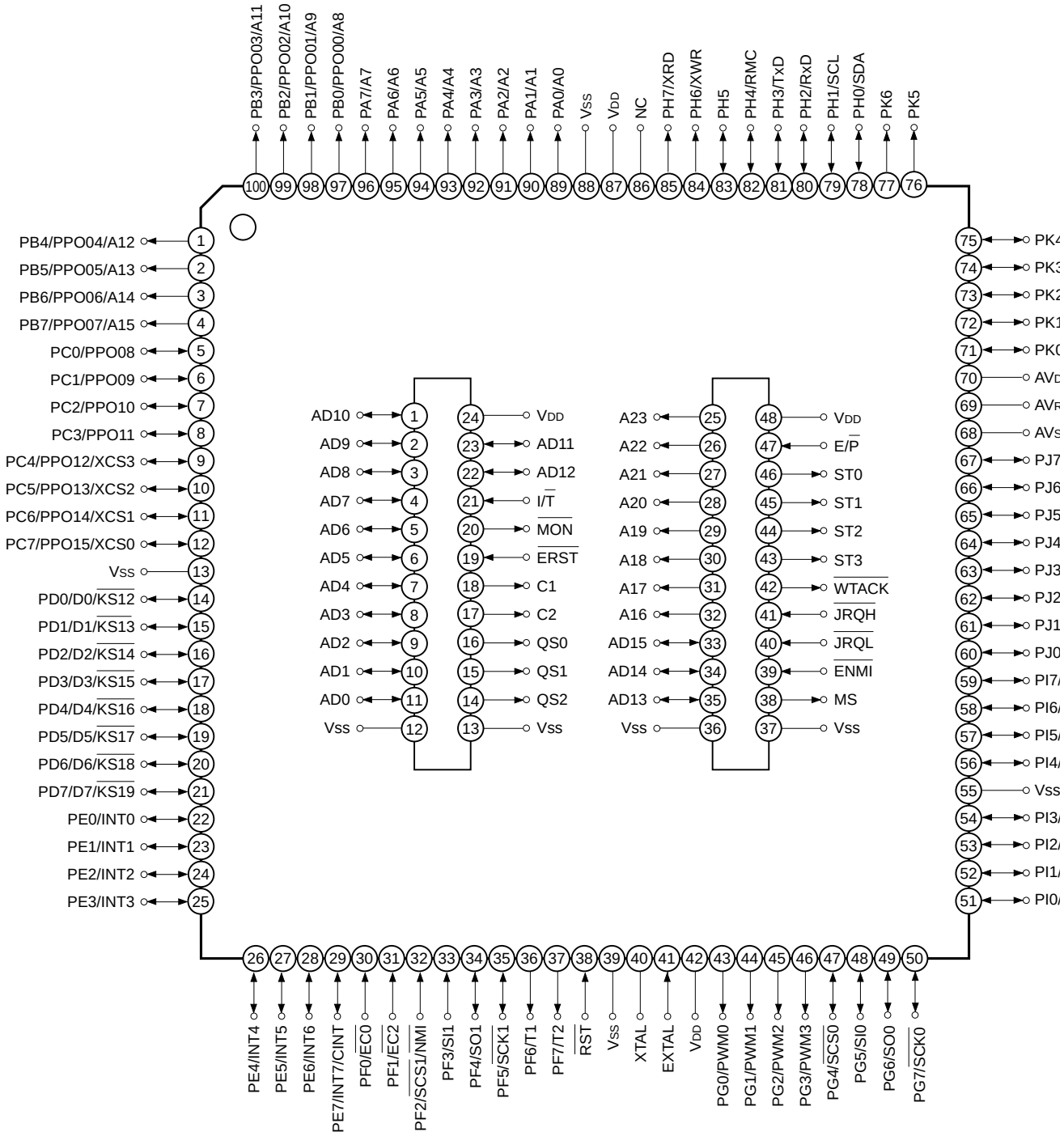


Note) 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.

2. Vss and AVss (Pins 13, 39, 55, 68 and 88) must be connected to GND.

3. V_{DD} and AV_{DD} (Pins 42, 70 and 87) must be connected to V_{DD}.

Pin Assignment in Evaluator Mode (Top View) 100-pin LQFP package



Note) 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.

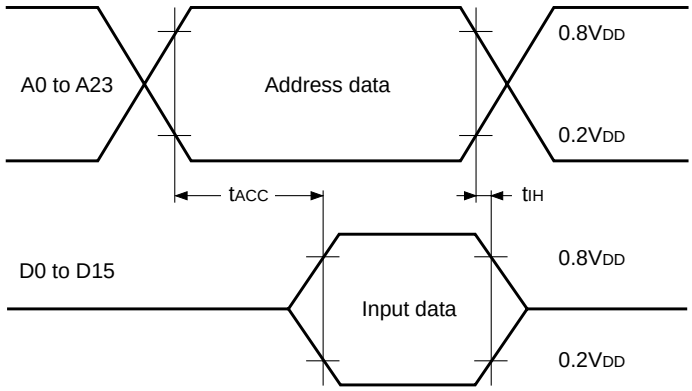
2. Vss and AVss (Pins 13, 39, 55, 68 and 88) must be connected to GND.

3. V_{DD} and AV_{DD} (Pins 42, 70 and 87) must be connected to V_{DD}.

EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V)

Item	Symbol	Pins	Min.	Max.	Unit
Address → data Input delay time	t_{ACC}	A0 to A23 D0 to D15		50	ns
Address → data hold time	t_{IH}	A0 to A23 D0 to D15	0		ns



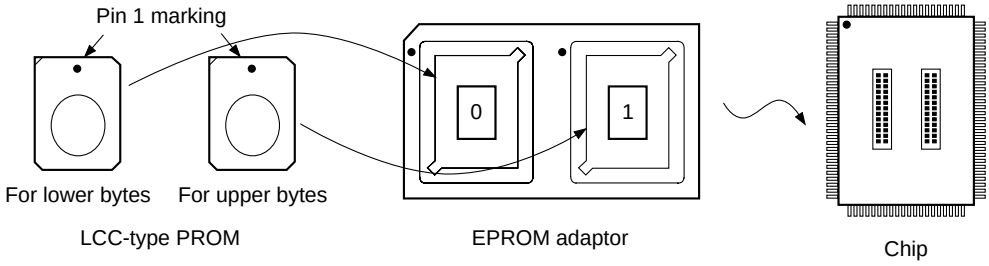
Product List

Type	Piggy/evaluation chip	
Product name	CXP971000-U01Q	CXP971000-U01R
Package	100-pin ceramic PQFP (QFP supported)	100-pin ceramic PQFP (LQFP supported)
ROM capacity	EPROM 512K bytes	
Reset pin pull-up resistor	Existent	

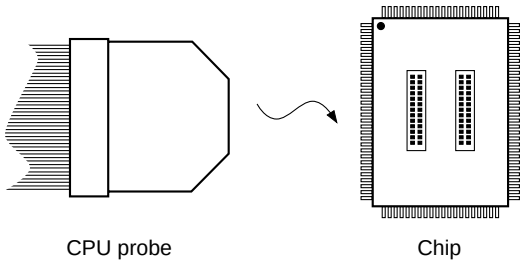
Switching of Piggyback Mode and Evaluator Mode

Piggyback mode can be used by setting two LCC-type EPROM (for upper bytes, for lower byte) and connecting to the connector of top of the chip.
Evaluator mode can be used by connecting in-circuit emulator CPU probe to the connector of top of the chip.

Piggyback mode



Evaluator mode

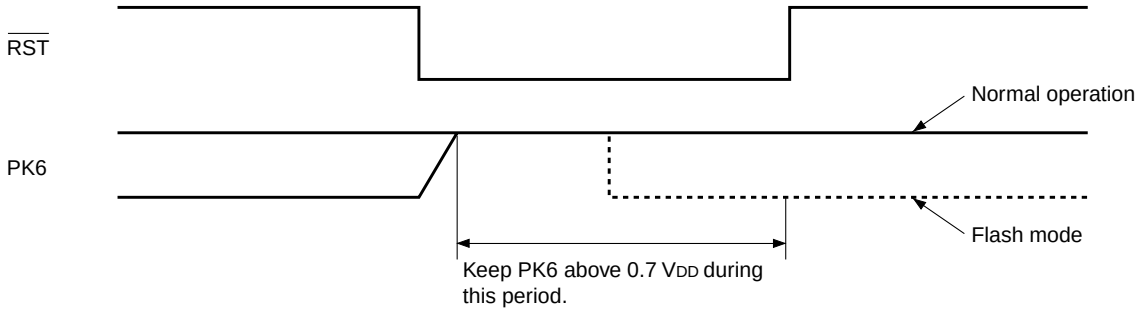


Notes on PK6 Usage

FLASH EEPROM incorporated PK6 is also used as flash mode setting function. Note the followings:

1. "H" is output to PK6 during a reset. That is driven at comparatively high impedance (approximately 150kΩ), and take care that V_{OH} should not fall under $0.7V_{DD}$ by the partial pressure with external circuit load impedance.

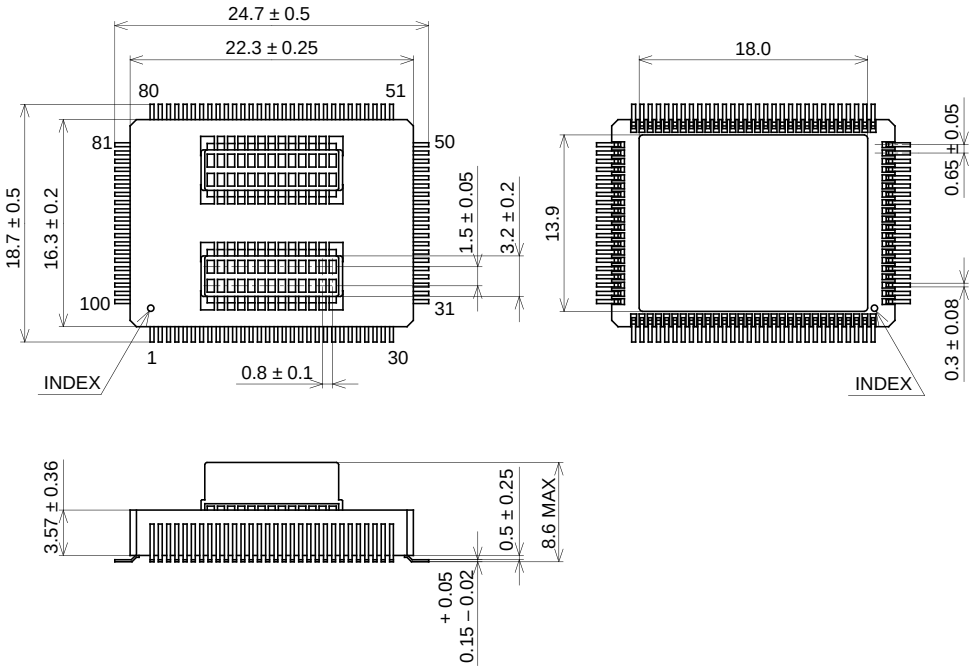
2. When using software reset functions, PK6 may not rise enough during a reset. Switching PK6 to "H" output prior to software reset execution or connecting pull-up resistor is recommended.



Mask ROM and piggy/evaluation chip do not have flash mode setting function. Considering that EEPROM incorporated type is used, above countermeasure should be performed.

Package Outline Unit: mm

100PIN PQFP(CERAMIC)

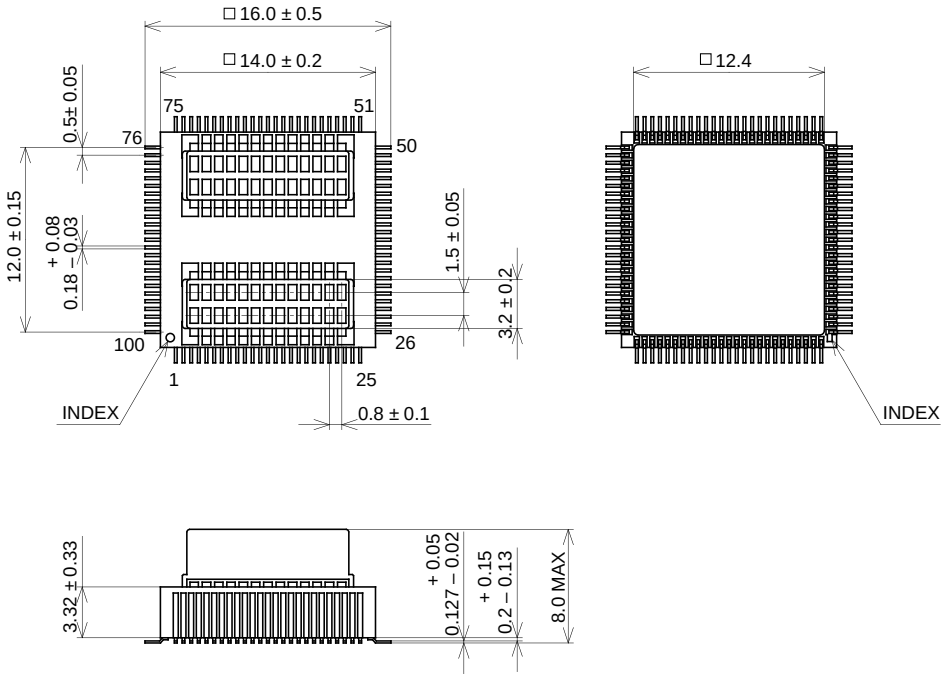


SONY CODE	PQFP-100C-L04
EIAJ CODE	AQFP100-C-0000
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	4.9g

100PIN PQFP(CERAMIC)



SONY CODE	PQFP-100C-L03
EIAJ CODE	AQFP100-C-0000
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.7g