

### FEATURES

- 8-Bit Triple Video Digital-to-Analog Converter
- 30 MWPS Operation (typ)
- Low Power: 135 mW
- Internal Voltage Reference
- 5 V Monolithic CMOS
- 48-Pin QFP Package (7 mm x 7 mm, 0.5 mm Pitch)

### APPLICATIONS

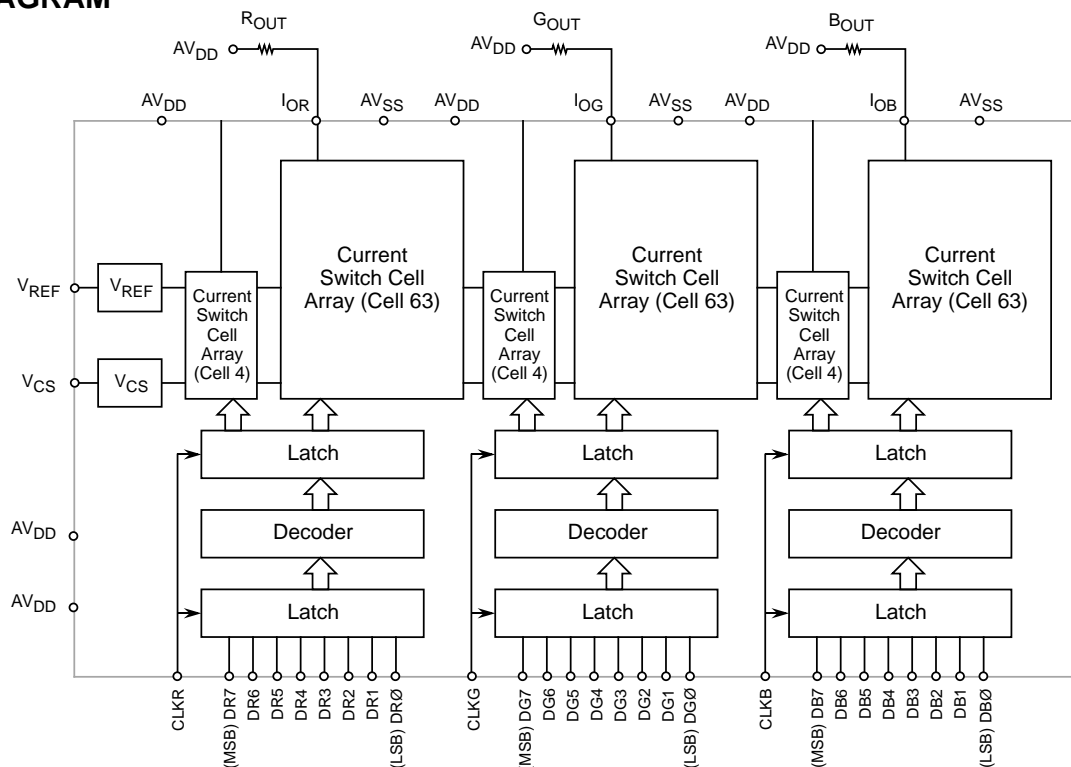
- Desktop Video Processing of S-Video and CCIR-601 Video Signals
- VGA Color Graphics Monitors
- Professional Video Equipment
- Digital Television

### GENERAL DESCRIPTION

The SPT5110 is an 8-bit, 30 MWPS triple video digital-to-analog converter specifically designed for high performance, high resolution color graphics monitor and video processing

applications. A single external resistor controls the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of  $\pm 0.5$  LSB over the full temperature range. The device is available in a 48-lead QFP package in the commercial temperature range.

### BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)<sup>1</sup>

### Supply Voltages

$AV_{DD}$  (measured to  $AV_{SS}$ ) ..... -0.3 to 7.0 V

### Output Current

$I_{OUT}$  ..... 0 to 7 mA

### Input Voltage

Clock and Data .....  $AV_{SS}$  to  $AV_{DD}$

### Temperature

Operating, ambient ..... 0 to +70 °C

Storage ..... -55 to +125 °C

**Note:** 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

## ELECTRICAL SPECIFICATIONS

$f_{CLK}$  = 27 MWPS,  $AV_{DD}$  = 5.0 V, Output Pull-Up Load = 240  $\Omega$ ,  $T_A$  = 25 °C,  $AV_{SS}$  = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
<b>DC ELECTRICAL CHARACTERISTICS</b>						
<b>DC Performance</b>						
Resolution				8.0		Bits
Differential Linearity	$T_A = T_{MIN}$ to $T_{MAX}$	I		$\pm 0.25$	$\pm 0.3$	LSB
Differential Linearity		I			$\pm 0.5$	LSB
Integral Linearity		I			$\pm 0.5$	$\pm 1.0$
<b>Analog Outputs</b>						
Output Voltage Range	$V_{CS} = +1.27$ V	I	3.6		5.0	V
Conversion Rate		I	27	30		MWPS
Output Offset Voltage		I		17	25	mV
Signal-to-Noise Ratio		I	41	47		dB
Differential Phase		V		1		Degrees
Differential Gain		V		2		%
Glitch Energy		V			100	pV-s
Settling Time		I		31	27	ns
Propagation Delay ( $t_{pd}$ )		V			10	ns
Crosstalk		I		-47		dB
FS Control Voltage ( $V_{CS}$ )		V		1.0		1.4
<b>Digital Inputs and Timing</b>						
Input Current, Logic High	$V_{IH} = 5$ V $V_{IL} = 0$ V	I			5	$\mu$ A
Input Current, Logic Low		I		-5		$\mu$ A
Set-Up Time, Data and Controls ( $t_S$ )		I	5			ns
Hold Time, Data and Controls ( $t_H$ )		I	10			ns
Clock Pulse Width (Low)		I	18.5			ns
Clock Pulse Width (High)		I	18.5			ns
<b>Power Supply Requirements</b>						
Supply Voltage		I	4.75		5.25	V
Supply Current		I			27	mA
Power Dissipation		I			135	mW

## TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

## TEST LEVEL

## TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at $T_A=25\text{ }^\circ\text{C}$ , and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at $T_A = 25\text{ }^\circ\text{C}$ . Parameter is guaranteed over specified temperature range.

## INTERFACE CONSIDERATIONS

Figure 1 shows a typical interface circuit of the SPT5110 in normal circuit operation.

## SUPPLY AND GROUND CONSIDERATIONS

SPT suggests that all power supply pins ( $AV_{DD}$ ) be tied together and decoupled using a  $0.1\text{ }\mu\text{F}$  ceramic capacitor in parallel with a  $10\text{ }\mu\text{F}$  tantalum capacitor.

## INTERNAL REFERENCE VOLTAGE ( $V_{REF}$ )

Voltage reference is internally generated. Connect a  $0.1\text{ }\mu\text{F}$  bypass capacitor as close to the pin as possible.

## FULL-SCALE ADJUST CONTROL ( $V_{CS}$ )

Connect a  $0.1\text{ }\mu\text{F}$  bypass capacitor with the shortest possible lead length between  $V_{CS}$  and  $AV_{SS}$ . A resistor connected between this pin and  $AV_{DD}$  controls the magnitude of the full-scale video signal.

The output voltage range of the SPT5110 can be kept constant and stable by keeping the value of  $V_{CS}$  to ground constant. The full-scale voltage changes according to  $V_{CS}$ . (See figure 2.)

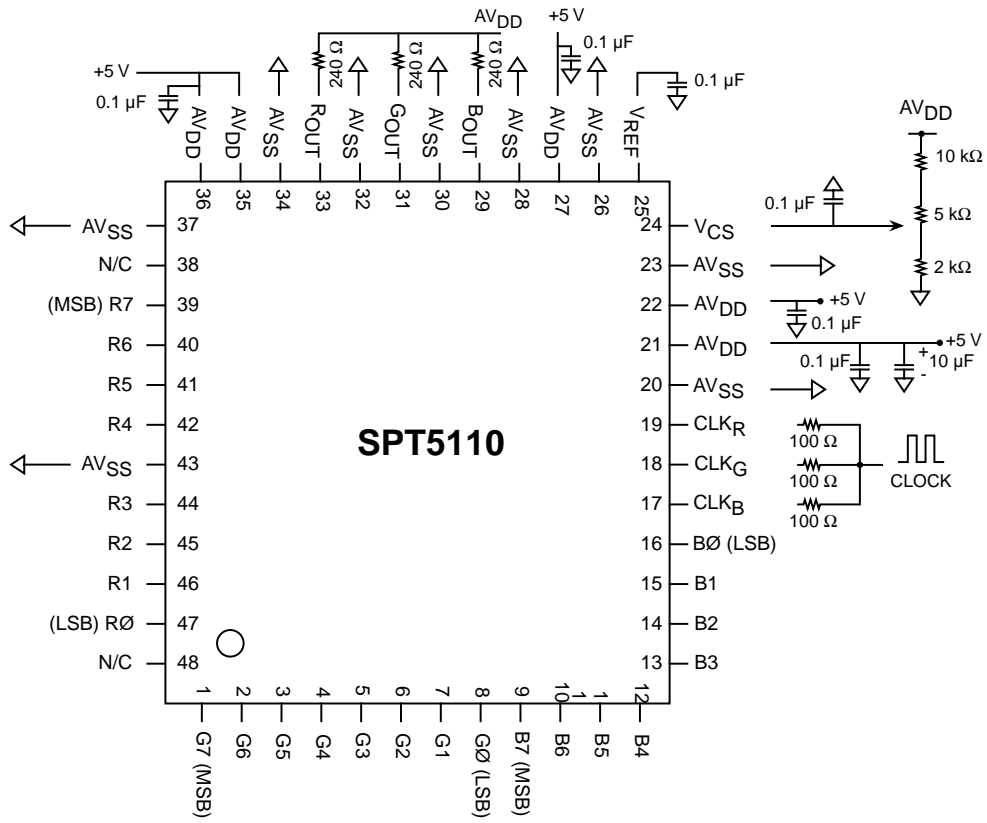
## CURRENT OUTPUTS

Each red, green and blue current output should have a load resistor connected to  $AV_{DD}$ . The resistors are typically  $240\text{ }\Omega$  and should be kept in the  $150\text{ }\Omega$  to  $250\text{ }\Omega$  range.

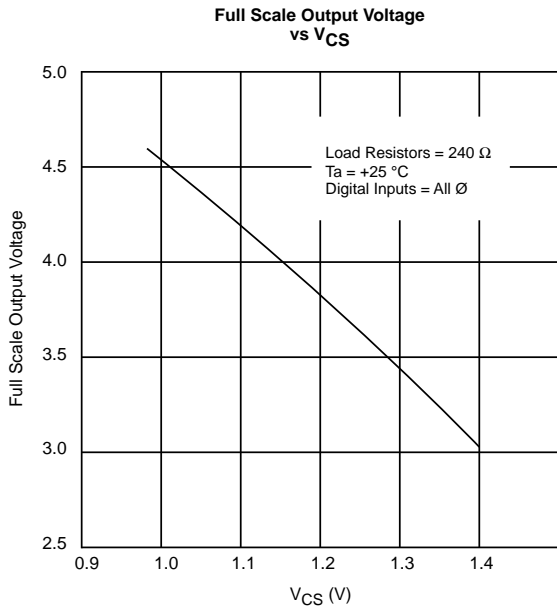
**Table I - Binary Codes**  
1 LSB = 5.49 mV,  $V_{CS} = 1.27\text{ V}$

Step	Digital Input								Analog Out (V)
	A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	
0	0	0	0	0	0	0	0	0	3.6000
1	0	0	0	0	0	0	0	1	3.6055
2	0	0	0	0	0	0	1	0	3.6110
3	0	0	0	0	0	0	1	1	3.6165
.				.					.
.				.					.
.				.					.
254	1	1	1	1	1	1	1	0	4.9890
255	1	1	1	1	1	1	1	1	4.9945

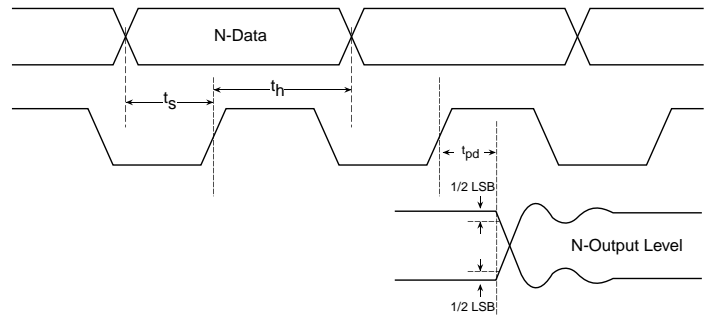
**Figure 1 - Typical Interface Circuit**



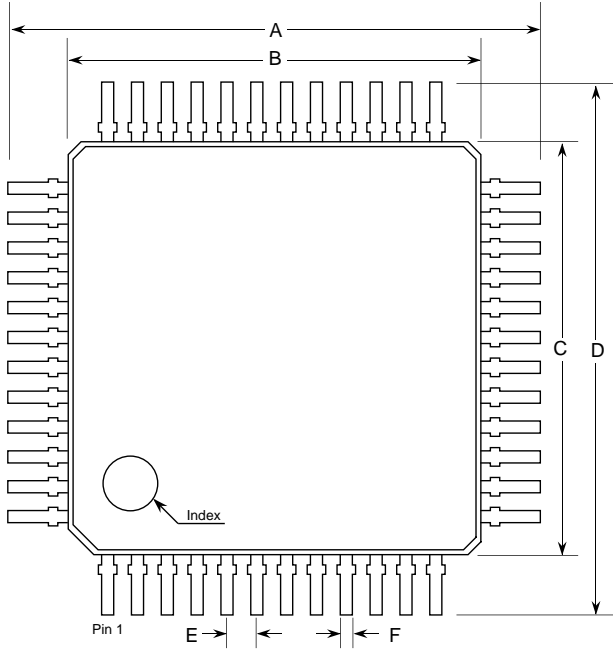
**Figure 2 - Typical Performance Characteristics**



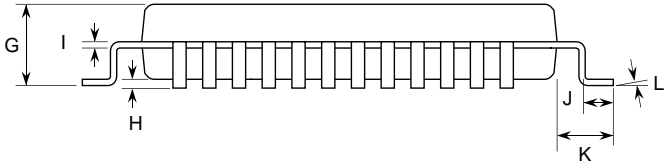
**Figure 3 - Timing Diagram**



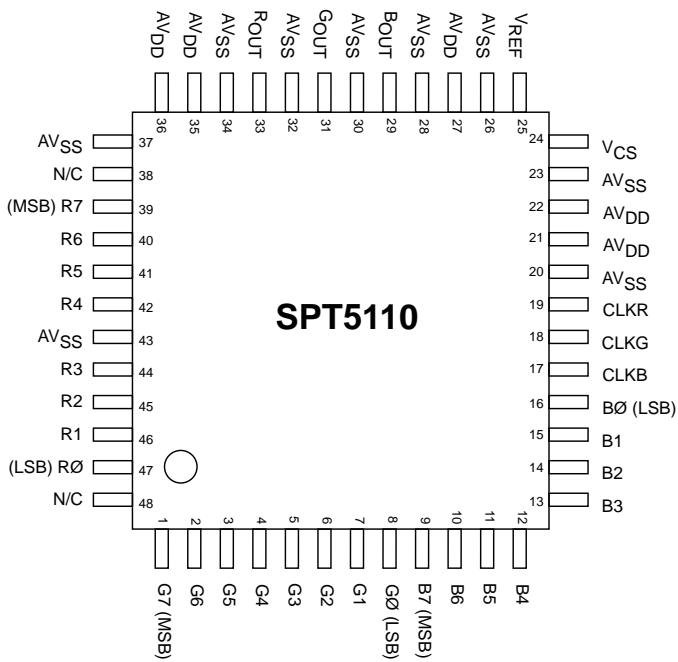
**PACKAGE OUTLINE**  
**48-Lead QFP**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.343	0.359	8.79	9.21
B	0.269	0.277	6.89	7.11
C	0.269	0.277	6.89	7.11
D	0.343	0.359	8.79	9.21
E	0.016	0.023	0.41	0.59
F	0.004	0.012	0.09	0.31
G	0.052	0.067	1.34	1.71
H	0.000	0.006		0.16
I	0.003	0.007	0.074	0.176
J	0.011	0.028	0.29	0.71
K	0.039 typ		1.0 typ	
L	0°	10°	0°	10°



## PIN ASSIGNMENTS



## PIN FUNCTIONS

Name	Function
ROUT	Red Analog Current Output
GOUT	Green Analog Current Output
BOUT	Blue Analog Current Output
R7 - R0	Red Data Inputs
G7 - G0	Green Data Inputs
B7 - B0	Blue Data Inputs
CLKR	Red Clock Input
CLKG	Green Clock Input
CLKB	Blue Clock Input
VREF	Voltage Reference (A 0.1 $\mu$ F ceramic capacitor should be used.)
VCS	Full-Scale Adjust Control Voltage 1 to 1.4 V.
AVSS	Ground
AVDD	Analog Power
N/C	No Connection

## ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5110SCT	0 to +70 °C	48L QFP

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**WARNING - LIFE SUPPORT APPLICATIONS POLICY** - SPT products should not be used within Life Support Systems without the specific written consent of SPT. A Life Support System is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in significant personal injury or death.

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.