SPT7725

8-BIT, 300 MSPS, FLASH A/D CONVERTER

TECHNICAL DATA

AUGUST 17, 2001

FEATURES

- Metastable errors reduced to 1 LSB
- Low input capacitance: 10 pF
- Wide input bandwidth: 210 MHz
- 300 MSPS conversion rate
- Typical power dissipation: 2.2 watts

APPLICATIONS

- Digital oscilloscopes
- Transient capture
- Radar, EW, ECM
- Direct RF down-conversion
- Medical electronics: ultrasound, CAT instrumentation

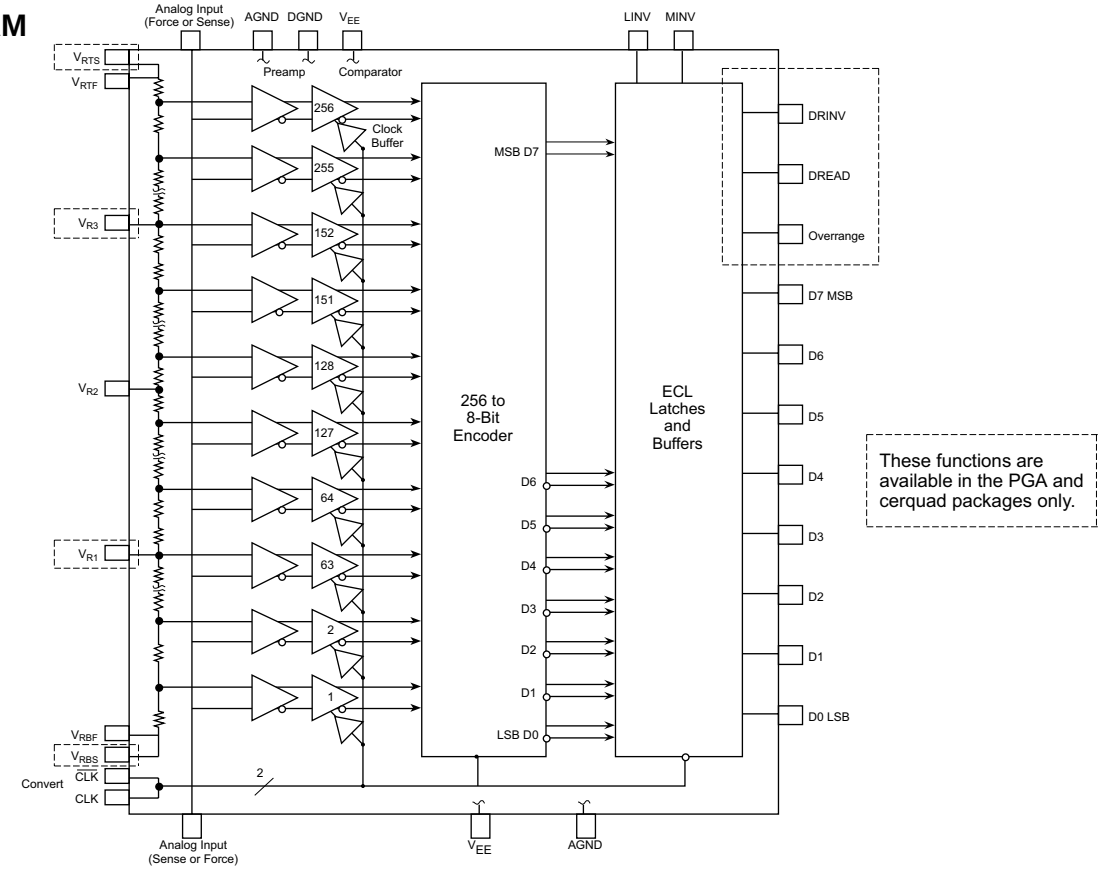
GENERAL DESCRIPTION

The SPT7725 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal into 8-bit digital words at a 300 MSPS (typ) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard –5.2 volt power supply is required for operation of the SPT7725, with nominal power dissipation of 2.2 W. A proprietary decoding scheme reduces metastable errors to the 1 LSB level.

The SPT7725 is available in 42-lead ceramic sidebrazed DIP, surface-mount 44-lead cerquad, and 46-lead PGA packages (all are pin-compatible with the SPT7710); the cerquad and PGA packages allow access to additional reference ladder taps, an overrange bit, and a data ready output. The SPT7725 is available in the industrial temperature range.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Negative Supply Voltage (V_{EE} TO GND) –7.0 to +0.5 V
Ground Voltage Differential ..... –0.5 to +0.5 V

Input Voltage

Analog Input Voltage ..... V_{EE} to +0.5 V
Reference Input Voltage ..... V_{EE} to +0.5 V
Digital Input Voltage ..... V_{EE} to +0.5 V
Reference Current V_{RTF} to V_{RBF} ..... 25 mA

Output

Digital Output Current ..... 0 to –30 mA

Temperature

Operating Temperature,ambient ..... –25 to +85 °C
junction ..... +150 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{EE}=–5.2 V, R_{Source}=50 Ω, V_{RBF}=–2.00 V, V_{R2}=–1.00 V, V_{RTF}=0.00 V, f_{CLK}=250 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7725A MIN	SPT7725A TYP	SPT7725A MAX	SPT7725B MIN	SPT7725B TYP	SPT7725B MAX	UNITS
DC Accuracy									
Integral Linearity Error	f_{CLK} = 100 kHz	VI	–0.75	±0.60	+0.75	–0.95	±0.80	+0.95	LSB
Differential Linearity Error	f_{CLK} = 100 kHz	VI	–0.75		+0.75	–0.95		+0.95	LSB
No missing codes			Guaranteed			Guaranteed			
Analog Input									
Offset Error V_{RT}		VI	–30		+30	–30		+30	mV
Offset Error V_{RB}		VI	–30		+30	–30		+30	mV
Input Voltage Range		VI	–2.0		0.0	–2.0		0.0	Volts
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		15			15		kΩ
Input Current		VI		250	500		250	500	µA
Input Slew Rate		V		1,000			1,000		V/µs
Large Signal Bandwidth	V_{IN}=F.S.	V		210			210		MHz
Small Signal Bandwidth	V_{IN}=500 mV_{P-P}	V		335			335		MHz
Clock Synchronous Input Currents		V		40			40		µA
Reference Input									
Ladder Resistance		VI	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
Timing Characteristics									
Maximum Sample Rate		IV	250	300		250	300		MSPS
Clock to Data Delay		V		2.4			2.4		ns
Output Delay Tempco		V		2			2		ps/°C
CLK-to-Data Ready Delay (t_D)		V		2.0			2.0		ns
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns
Dynamic Performance									
Signal-to-Noise Ratio	f_{IN} = 3.58 MHz	VI	45	47		44	46		dB
	f_{IN} = 50 MHz	VI	39	42		38	41		dB
Total Harmonic Distortion	f_{IN} = 3.58 MHz	VI		–52	–48		–50	–46	dB
	f_{IN} = 50 MHz	VI		–43	–40		–42	–39	dB
Signal-to-Noise and Distortion (SINAD)	f_{IN} = 3.58 MHz	VI	44	46		42	44		dB
	f_{IN} = 50 MHz	VI	37	39		35	37		dB

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{EE}=–5.2 V, R_{Source}=50 Ω, V_{RBF}=–2.00 V, V_{R2}=–1.00 V, V_{RTF}=0.00 V, f_{CLK}=250 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7725A MIN	SPT7725A TYP	SPT7725A MAX	SPT7725B MIN	SPT7725B TYP	SPT7725B MAX	UNITS
Digital Inputs									
Digital Input High Voltage (MINV, LINV)		VI	–1.1		–0.7	–1.1		–0.7	Volts
Digital Input Low Voltage (MINV, LINV)		VI	–2.0		–1.5	–2.0		–1.5	Volts
Clock Low Width, t_{PWL}		VI	2.2	2.0		2	1.8		ns
Clock High Width, t_{PWH}		VI	2.2	2.0		2	1.8		ns
Digital Outputs									
Digital Output High Voltage	50 Ω to –2 V	VI	–1.1			–1.1			Volts
Digital Output Low Voltage	50 Ω to –2 V	VI			–1.5			–1.5	Volts
Power Supply Requirements									
Supply Current	+25 °C	VI		425	550		425	550	mA
Power Dissipation	+25 °C	VI		2.2	2.9		2.2	2.9	W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

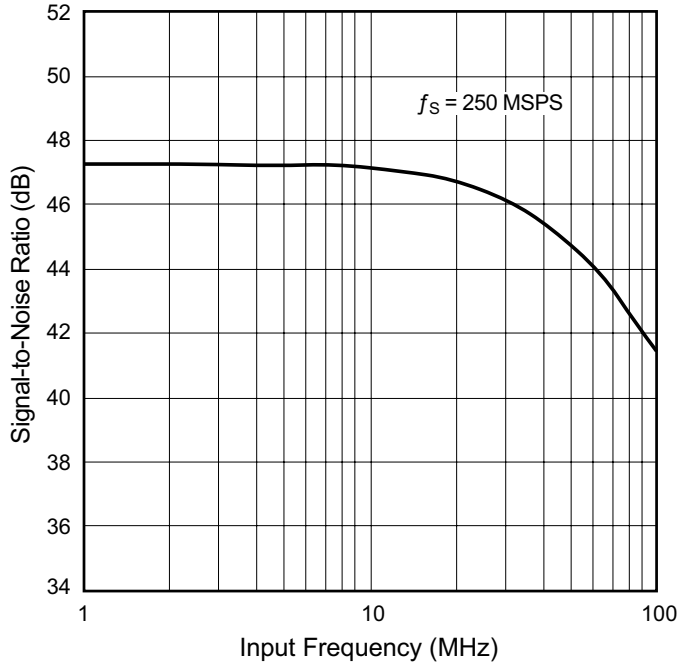
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all test are pulsed tests; therefore, $T_J = T_C = T_A$.

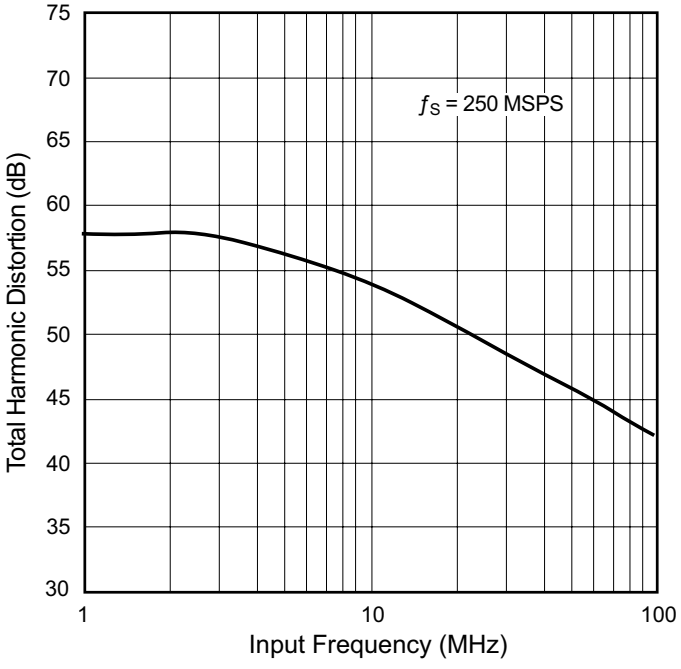
LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

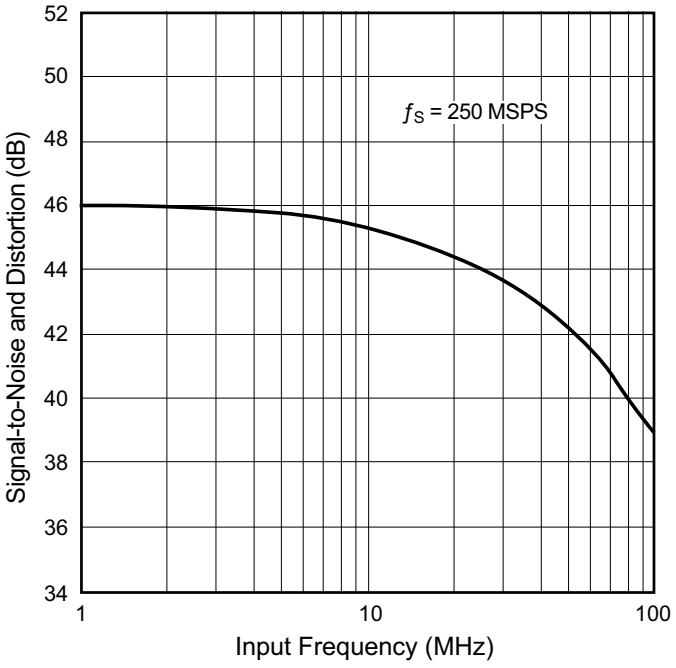
SNR vs Input Frequency



THD vs Input Frequency



SINAD vs Input Frequency



SNR, THD, SINAD vs Temperature

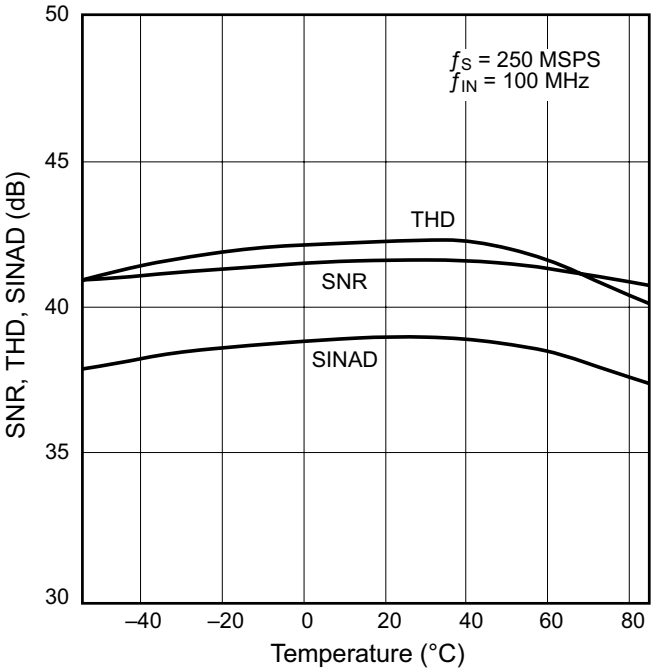
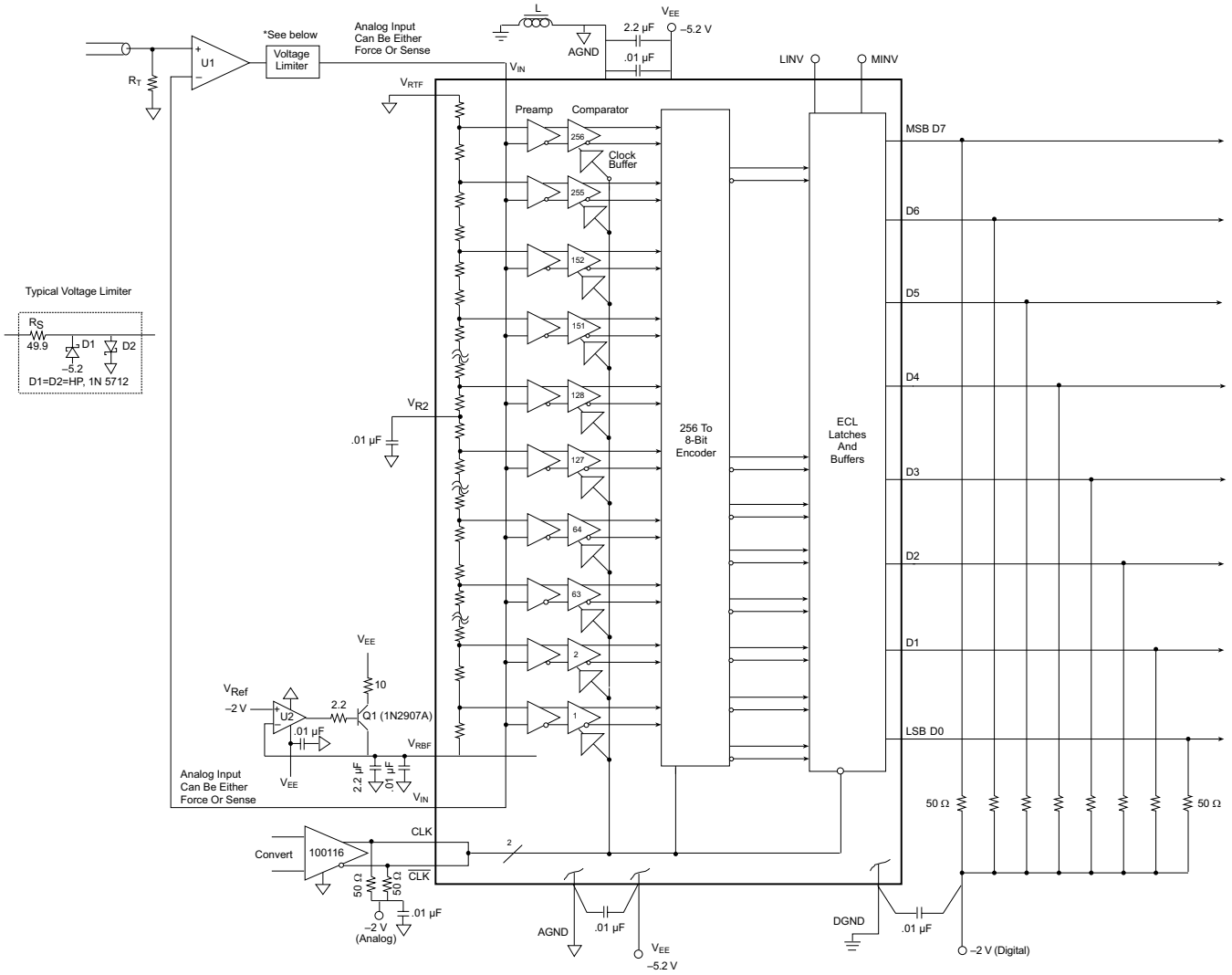


Figure 1 – Typical Interface Circuit 1



GENERAL DESCRIPTION

The SPT7725 is a fast monolithic 8-bit parallel flash A/D converter. The nominal conversion rate is 300 MSPS and the analog bandwidth is in excess of 200 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant for varying input voltages and frequencies and, therefore, makes the part easier to drive than previous flash converters. The SPT7725 incorporates a proprietary decoding scheme that reduces metastable errors (sparkle codes or *flyers*) to a maximum of 1 LSB.

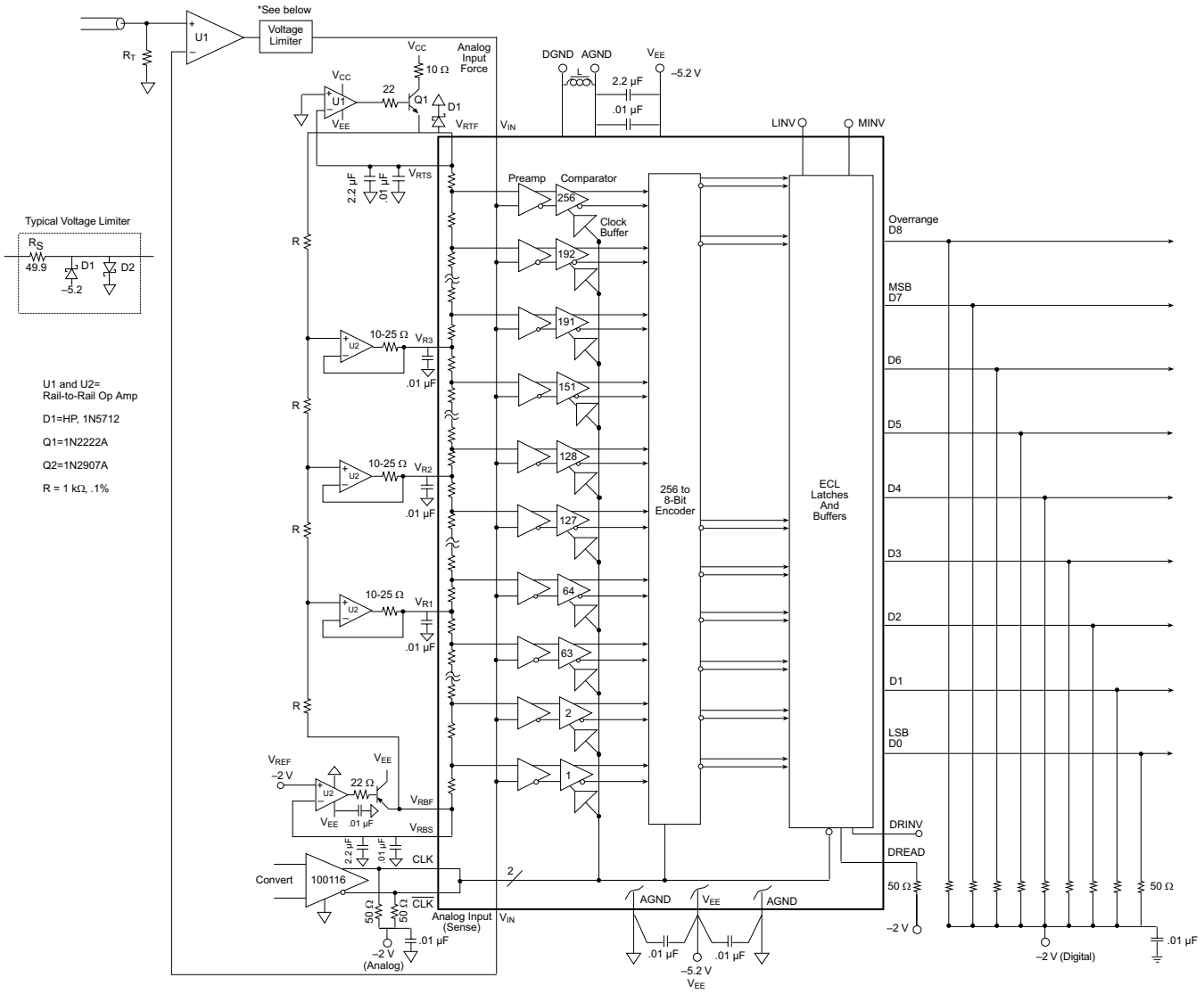
The SPT7725 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit is shown in figure 1. The SPT7725 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a

Figure 2 – Typical Interface Circuit 2 (PGA and Cerquad packages only)



double-sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in figure 2 (PGA and cerquad packages only) is intended to show the most elaborate method of achieving the least error by correcting for integral nonlinearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, an input buffer, and supply decoupling. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum should also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 1.

V_{IN} (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input *sense* and the other for input *force*. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by

Table I – Output Coding

		BINARY		TWOs COMPLEMENT	
		TRUE	INVERTED	TRUE	INVERTED
ANALOG INPUT VOLTAGE	D8	MINV=LINV=0 D7_____D0	MINV=LINV=1 D7_____D0	MINV=1; LINV=0 D7_____D0	MINV=0; LINV=1 D7_____D0
–2 V + 1/2 LSB	0	00000000 00000001	11111111 11111110	10000000 10000001	01111111 01111110
–1.0 V	0	01111111 10000000	10000000 01111111	11111111 00000000	00000000 11111111
0 V – 1/2 LSB	0	11111111 11111110	00000000 00000001	01111111 01111110	10000000 10000001
≥0 V	1	11111111	00000000	01111111	10000000

the same source. The SPT7725 is superior to similar devices, due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. An optional input buffer may be used.

CLK, $\overline{\text{CLK}}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{\text{CLK}}$ is internally biased to –1.3 V. (See clock input circuit.) $\overline{\text{CLK}}$ may be left open, but a .01 µF bypass capacitor from $\overline{\text{CLK}}$ to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. For more information, see table I. Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive ECL levels into 50 Ω when pulled down to –2 V. When pulled down to –5.2 V, the outputs can drive 150 Ω to 1 kΩ loads.

V_{RBF}, V_{R2}, V_{RTF} (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are –2 V (V_{RBF}), mid-tap (V_{R2}), and AGND (V_{RTF}). The reference pins can be driven as shown in figure 1. V_{R2} should be bypassed to AGND for further noise suppression.

V_{RBF}, V_{RBS}, V_{R1}, V_{R2}, V_{R3}, V_{RTF}, V_{RTS} REFERENCE INPUTS *(PGA AND CERQUAD PACKAGES ONLY)*

These are five external reference voltage taps from –2 V (V_{RBF}) to AGND (V_{RTF}) that can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in figure 2. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. V_{RB} and V_{RT} have force and sense pins for monitoring the top and bottom voltage references.

N/C

All *Not Connected* pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

DREAD – DATA READY; DRINV – DATA READY INVERSE *(PGA AND CERQUAD PACKAGES ONLY)*

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the SPT7725's decoders and latches. This function is useful for interfacing with high-speed memory. Using the data ready output to latch the output data ensures minimum set-up and hold times. DRINV is a data ready inverse control pin. (See the timing diagram.)

D8 – OVERRANGE *(PGA AND CERQUAD PACKAGES ONLY)*

This is an overrange function. When the SPT7725 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the SPT7725 into higher resolution systems.

OPERATION

The SPT7725 has 256 preamp/comparator pairs that are each supplied with the voltage from V_{RTF} to V_{RBF} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each comparator's individual clock buffer. When CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RTF} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low.

At the output of the decoders is a set of four 7-bit latches that are enabled (*track*) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns, and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions, which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 3 – Timing Diagram

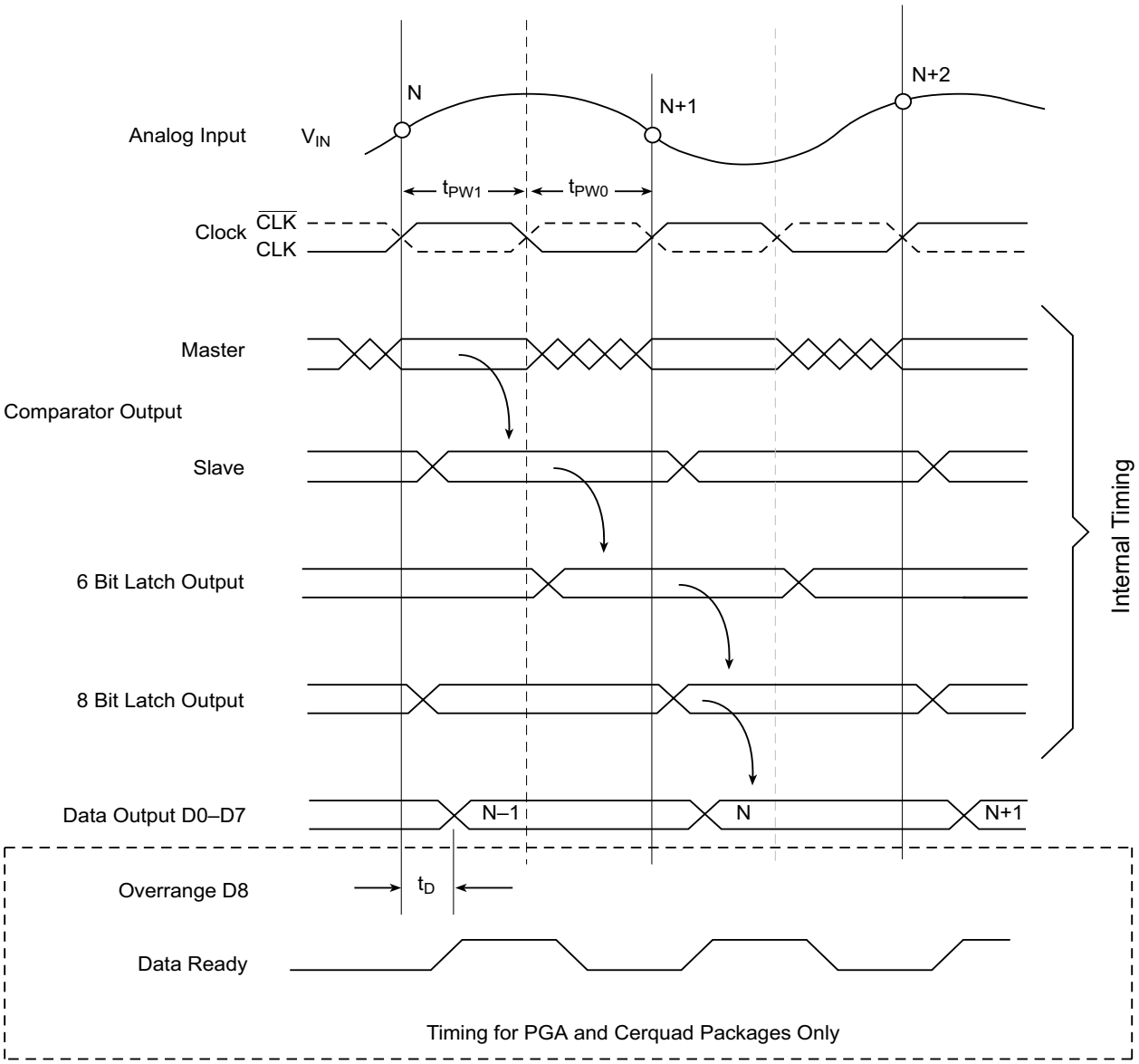


Figure 4 – Subcircuit Schematics

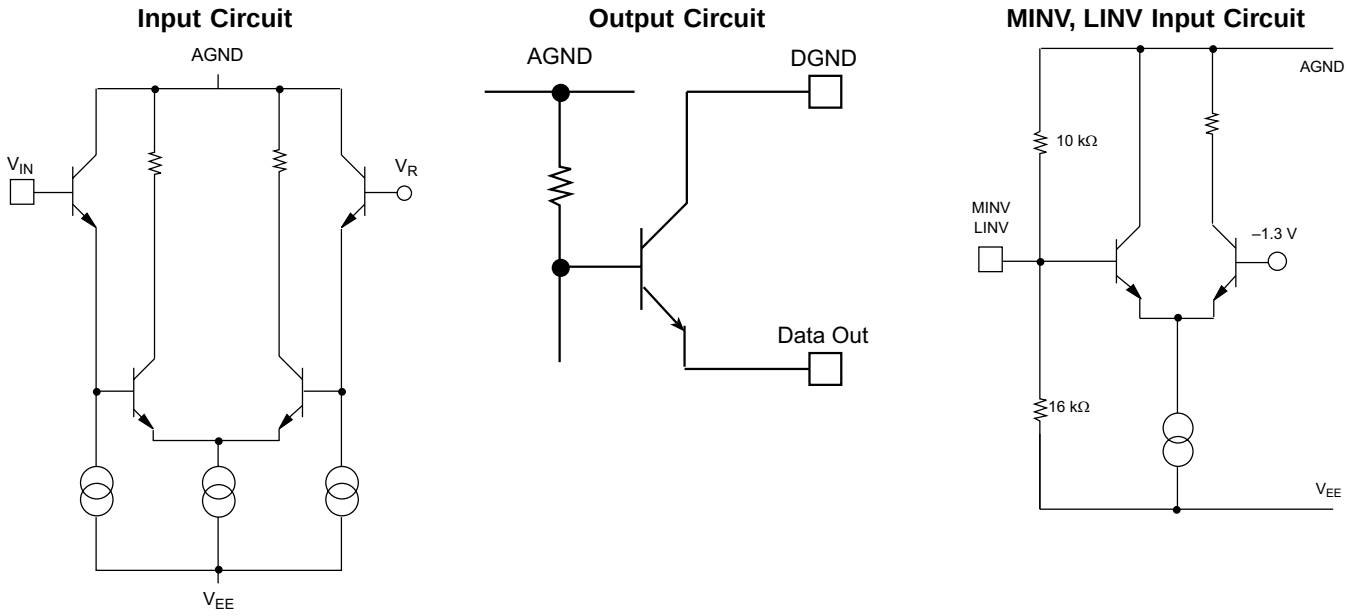


Figure 5 – Clock Input

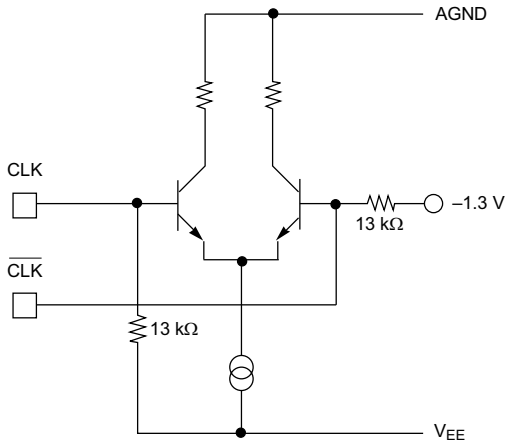
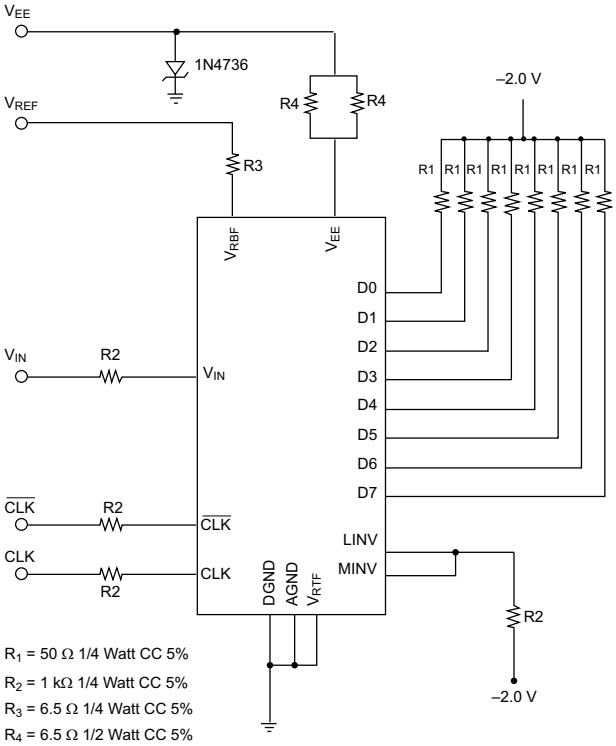


Figure 6 – Burn-In Circuit (42-lead DIP Package only)

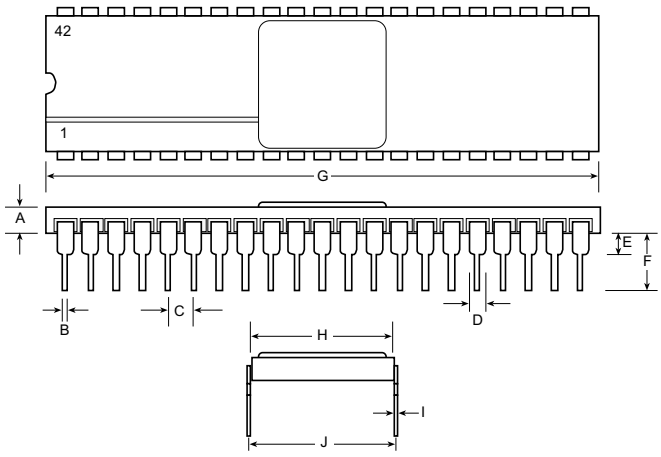


EVALUATION BOARDS

The EB7725 evaluation board is available to aid designers in demonstrating the full performance of the SPT7725. This board includes a voltage reference circuit, clock driver circuit, output data latches, and an on-board reconstruction of the digital data. An application note describing the operation of this board, as well as application tips, is also available. Contact the factory for price and delivery.

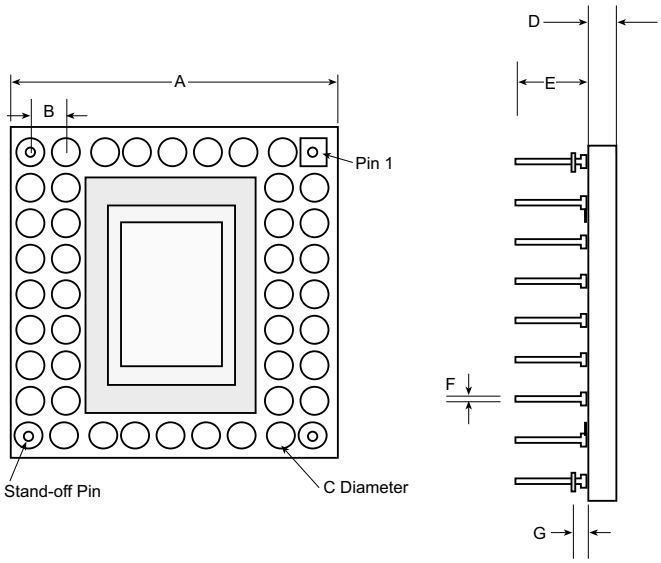
PACKAGE OUTLINES

42-Lead Sidebrazed DIP



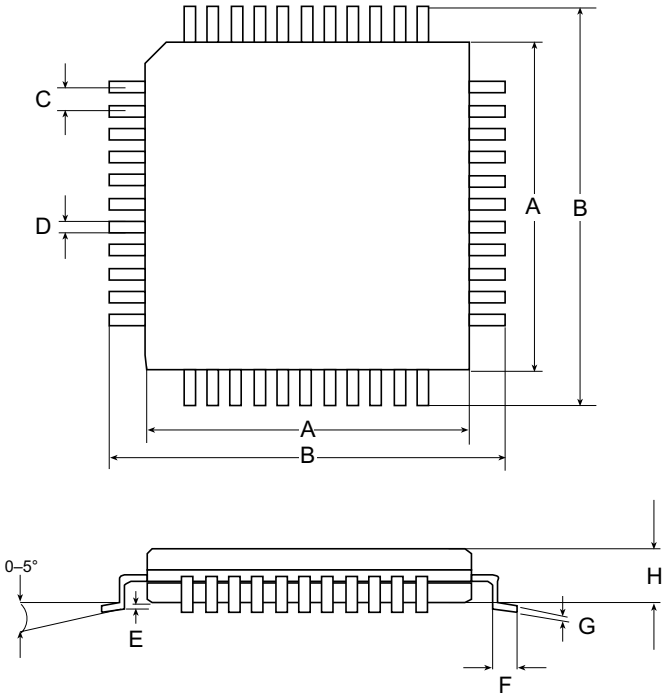
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D	.050 typ		1.27	
E	.050 typ		1.27	
F		0.275		6.99
G	2.080	2.120	52.83	53.85
H	0.585	0.605	14.86	15.37
I	0.008	0.015	0.20	0.38
J	0.600	0.620	15.24	15.75

46-Lead Pin Grid Array



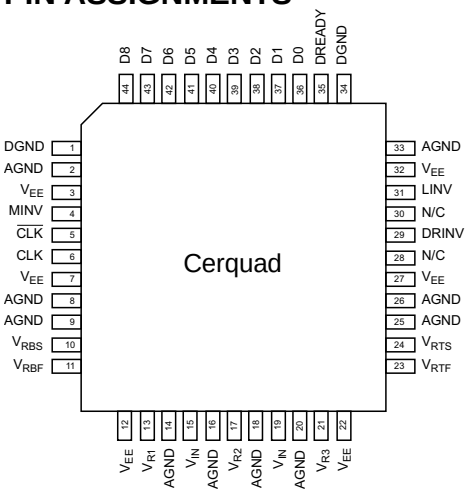
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.100 typ		2.54 typ	
C	.045 dia	.055 dia	1.14	1.40
D	0.084	0.096	2.13	2.44
E	0.169	0.193	4.29	4.90
F	.020 dia	.030 dia	0.51	0.76
G	.050 typ		1.27 typ	

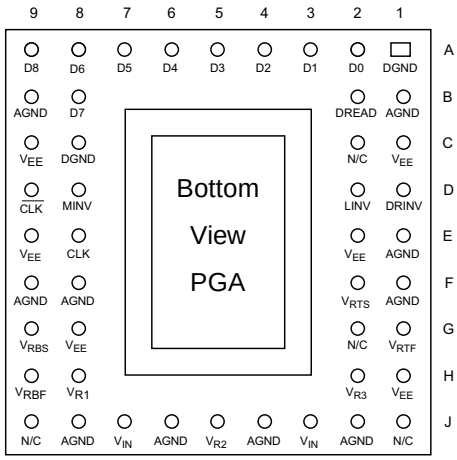
44-Lead Cerquad

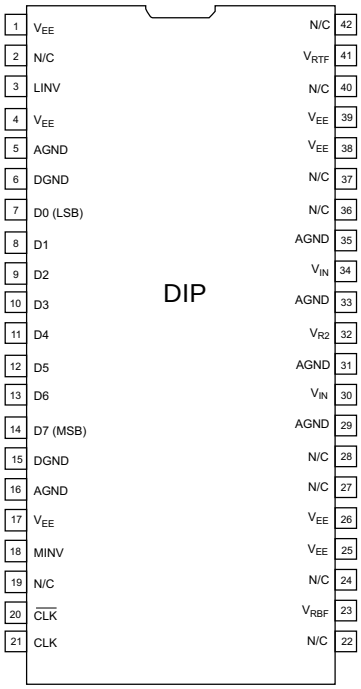


	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.550 typ		13.97 typ	
B	0.685	0.709	17.40	18.00
C	0.037	0.041	0.94	1.04
D	0.016 typ		0.41 typ	
E	0.008 typ		0.20 typ	
F	0.027	0.051	0.69	1.30
G	0.006 typ		0.15 typ	
H	0.080	0.089	2.03	2.26

PIN ASSIGNMENTS







PIN FUNCTIONS

Name	Function
LINV	D0 through D6 Output Inversion Control Pin
V_{EE}	Negative Analog Supply Nominally –5.2 V
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1–D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
AGND	Analog Ground
V_{IN}	Analog Input; Can be Connected to the Input Signal or Used as a Sense
V_{R2}	Reference Voltage Tap 2 (–1.0 V typ)
V_{RTF}	Reference Voltage Top
V_{RBF}	Reference Voltage Bottom

The following pins are on PGA and cerquad packages only.

DRINV	Data Ready Inverse
DREAD	Data Ready Output
Overrange	Overrange Output D8
V_{R1}	Reference Voltage Tap 1 (–1.5 V typ)
V_{R3}	Reference Voltage Tap 3 (–0.5 V typ)
V_{RTS}	Reference Voltage Top, Sense
V_{RBS}	Reference Voltage Bottom, Sense

ORDERING INFORMATION

PART NUMBER	LINEARITY	TEMPERATURE RANGE	PACKAGE TYPE
SPT7725AIJ	0.75 LSB	–25 to +85 °C	42L Ceramic S/B
SPT7725BIJ	0.95 LSB	–25 to +85 °C	42L Ceramic S/B
SPT7725AIG	0.75 LSB	–25 to +85 °C	46L PGA
SPT7725BIG	0.95 LSB	–25 to +85 °C	46L PGA
SPT7725AIQ	0.75 LSB	–25 to +85 °C	44L Cerquad
SPT7725BIQ	0.95 LSB	–25 to +85 °C	44L Cerquad
SPT7725BCU	0.95 LSB	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.

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Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.