

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ± 2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- 50 dB SNR @ 10.3 MHz Input
- Low Power (1.3 W Typical)
- 5 pF Input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

GENERAL DESCRIPTION

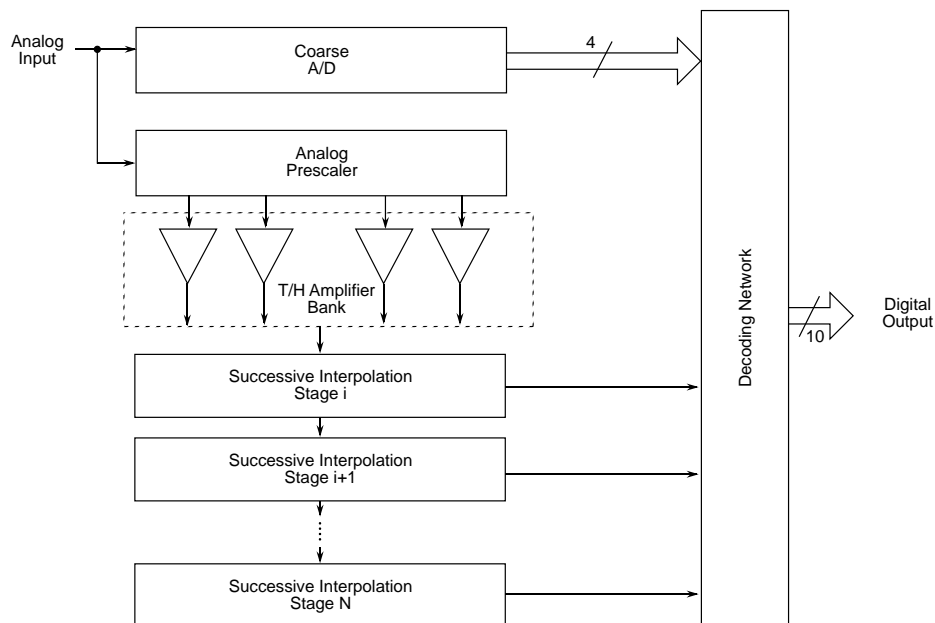
The SPT7814 A/D converter is a 10-bit monolithic converter capable of word rates of a minimum of 40 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions.

Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7814 also provides a wide input voltage swing of ± 2.0 volts.

The SPT7814 is available in a 28-lead ceramic sidebraced DIP, PDIP, and die form. Commercial and industrial temperature ranges are currently offered. Contact the factory for availability of military temperature ranges and /833 processed units.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25 °C

Supply Voltages

V_{CC} -0.3 to +6 V
 V_{EE} +0.3 to -6 V

Input Voltages

Analog Input $V_{FB} \leq V_{IN} \leq V_{FT}$
 V_{FT}, V_{FB} +3.0 V, -3.0 V
 Reference Ladder Current 12 mA

Output

Digital Outputs +30 to -30 mA

Temperature

Operating Temperature -25 to +85 °C
 Junction Temperature (1) +175 °C
 Lead Temperature, (soldering 10 seconds) +300 °C
 Storage Temperature -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{min} - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

| PARAMETERS | TEST CONDITIONS | TEST LEVEL | SPT7814A | | | SPT7814B | | | UNITS |
|-----------------------------|------------------------|------------|------------|-----|-----|------------|-----|-----|-------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Resolution | | | 10 | | | 10 | | | Bits |
| DC Accuracy (+25 °C) | ± Full Scale | | | | | | | | |
| Integral Nonlinearity | 250 kHz Sample Rate | V | ±1.0 | | | ±1.5 | | | LSB |
| Differential Nonlinearity | | V | ±0.5 | | | ±0.75 | | | LSB |
| No Missing Codes | | VI | Guaranteed | | | Guaranteed | | | |
| Analog Input | | | | | | | | | |
| Input Voltage Range | | VI | ±2.0 | | | ±2.0 | | | |
| Input Bias Current | V _{IN} =0 V | VI | 30 60 | | | 30 60 | | | µA |
| Input Resistance | | VI | 100 | 300 | | 100 | 300 | | kΩ |
| Input Capacitance | | V | 5 | | | 5 | | | pF |
| Input Bandwidth | 3 dB Small Signal | V | 120 | | | 120 | | | MHz |
| +FS Error | | V | ±2.0 | | | ±2.0 | | | LSB |
| -FS Error | | V | ±2.0 | | | ±2.0 | | | LSB |
| Reference Input | | | | | | | | | |
| Reference Ladder Resistance | | VI | 500 | 800 | | 500 | 800 | | Ω |
| Reference Ladder Tempco | | V | 0.8 | | | 0.8 | | | Ω/°C |
| Timing Characteristics | | | | | | | | | |
| Maximum Conversion Rate | | VI | 40 | | | 40 | | | MHz |
| Overvoltage Recovery Time | | V | 20 | | | 20 | | | ns |
| Pipeline Delay (Latency) | | IV | 1 | | | 1 | | | Clock Cycle |
| Output Delay | T _A =+25 °C | V | 5 | | | 5 | | | ns |
| Aperture Delay Time | T _A =+25 °C | V | 1 | | | 1 | | | ns |
| Aperture Jitter Time | T _A =+25 °C | V | 5 | | | 5 | | | ps-RMS |
| Dynamic Performance | | | | | | | | | |
| Effective Number of Bits | | | | | | | | | |
| f _{IN} =1 MHz | | | 8.7 | | | 8.2 | | | Bits |
| f _{IN} =3.58 MHz | | | 8.7 | | | 8.2 | | | Bits |
| f _{IN} =10.3 MHz | | | 7.3 | | | 6.9 | | | Bits |

Typical thermal impedances: 28L sidebraced DIP: θ_{ja} = 50 °C/W,
 28L plastic DIP: θ_{ja} = 50 °C/W.

ELECTRICAL SPECIFICATIONS

$T_A = T_{min} - T_{max}$, $V_{CC} = +5.0$ V, $V_{EE} = -5.2$ V, $V_{IN} = \pm 2.0$ V, $V_{SB} = -2.0$ V, $V_{ST} = +2.0$ V, $f_{clock} = 40$ MHz, 50% clock duty cycle, unless otherwise specified.

| PARAMETERS | TEST CONDITIONS | TEST LEVEL | SPT7814A | | | SPT7814B | | | UNITS |
|--|--|------------|----------|-----------|-------|----------|-----------|-------|---------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Dynamic Performance | | | | | | | | | |
| Signal-To-Noise Ratio (without Harmonics) | | | | | | | | | |
| $f_{IN} = 1$ MHz | +25 °C | I | 55 | 57 | | 52 | 54 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 53 | 55 | | 50 | 52 | | dB |
| $f_{IN} = 3.58$ MHz | +25 °C | I | 55 | 57 | | 52 | 54 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 53 | 55 | | 50 | 52 | | dB |
| $f_{IN} = 10.3$ MHz | +25 °C | I | 48 | 50 | | 46 | 48 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 45 | 47 | | 43 | 45 | | dB |
| Harmonic Distortion | | | | | | | | | |
| $f_{IN} = 1$ MHz | +25 °C | I | 54 | 56 | | 52 | 54 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 51 | 53 | | 49 | 51 | | dB |
| $f_{IN} = 3.58$ MHz | +25 °C | I | 54 | 56 | | 52 | 54 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 51 | 53 | | 49 | 51 | | dB |
| $f_{IN} = 10.3$ MHz | +25 °C | I | 46 | 48 | | 43 | 45 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 45 | 47 | | 41 | 43 | | dB |
| Signal-to-Noise and Distortion | | | | | | | | | |
| $f_{IN} = 1$ MHz | +25 °C | I | 52 | 54 | | 49 | 51 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 49 | | | 46 | | | dB |
| $f_{IN} = 3.58$ MHz | +25 °C | I | 52 | 54 | | 49 | 51 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 49 | | | 46 | | | dB |
| $f_{IN} = 10.3$ MHz | +25 °C | I | 44 | 46 | | 41 | 43 | | dB |
| | $T_A = T_{min} - T_{max}$ | IV | 43 | | | 40 | | | dB |
| Spurious Free Dynamic Range | +25 °C, $f_{IN} = 1$ MHz | V | | 67 | | | 67 | | dB |
| Differential Phase | +25 °C, $f_{IN} = 3.58$ & 4.35 MHz | V | | 0.2 | | | 0.2 | | Degree |
| Differential Gain | +25 °C, $f_{IN} = 3.58$ & 4.35 MHz | V | | 0.5 | | | 0.7 | | % |
| Digital Inputs | | | | | | | | | |
| Logic 1 Voltage | | VI | -1.1 | | | -1.1 | | | V |
| Logic 0 Voltage | | VI | | | -1.5 | | | -1.5 | V |
| Maximum Input Current Low | | VI | -500 | ± 200 | +750 | -500 | ± 200 | +750 | μ A |
| Maximum Input Current High | | VI | -500 | ± 300 | +750 | -500 | +300 | +750 | μ A |
| Pulse Width Low (CLK) | | IV | 10 | | | 10 | | | ns |
| Pulse Width High (CLK) | | IV | 10 | | 300 | 10 | | 300 | ns |
| Digital Outputs | | | | | | | | | |
| Logic 1 Voltage | 50 Ω to -2 V | VI | -1.1 | -0.8 | | -1.1 | -0.8 | | V |
| Logic 0 Voltage | 50 Ω to -2 V | VI | | -1.8 | -1.5 | | -1.8 | -1.5 | V |
| Power Supply Requirements | | | | | | | | | |
| Voltages V_{CC} | | IV | +4.75 | -5.0 | +5.25 | +4.75 | +5.0 | +5.25 | V |
| - V_{EE} | | IV | -4.95 | -5.2 | -5.45 | -4.95 | -5.2 | -5.45 | V |
| Currents I_{CC} | | VI | | 140 | 170 | | 140 | 190 | mA |
| - I_{EE} | | VI | | 115 | 140 | | 115 | 160 | mA |
| Power Dissipation | Outputs Open | VI | | 1.3 | 1.6 | | 1.3 | 1.8 | W |
| Power Supply Rejection Ratio | (5 V \pm 0.25 V, -5.2 V \pm 2.0 V) | V | | 1.0 | | | 1.0 | | LSB |

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL

TEST PROCEDURE

| | |
|-----|--|
| I | 100% production tested at the specified temperature. |
| II | 100% production tested at $T_A=25\text{ }^\circ\text{C}$, and sample tested at the specified temperatures. |
| III | QA sample tested only at the specified temperatures. |
| IV | Parameter is guaranteed (but not tested) by design and characterization data. |
| V | Parameter is a typical value for information purposes only. |
| VI | 100% production tested at $T_A = 25\text{ }^\circ\text{C}$. Parameter is guaranteed over specified temperature range. |

Figure 1A: Timing Diagram

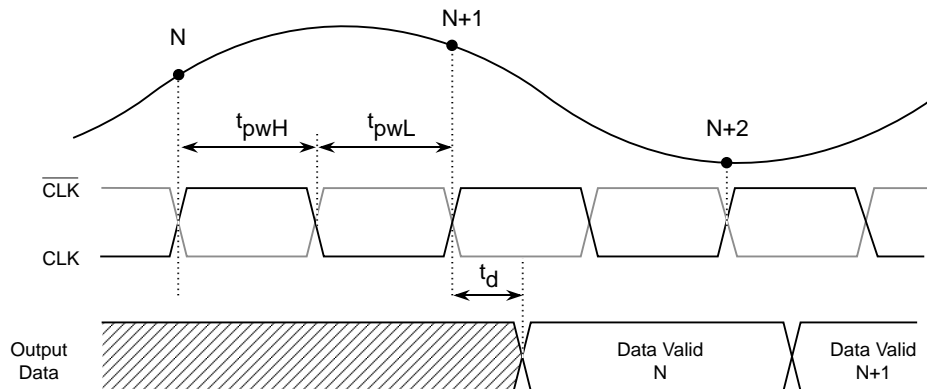


Figure 1B: Single Event Clock

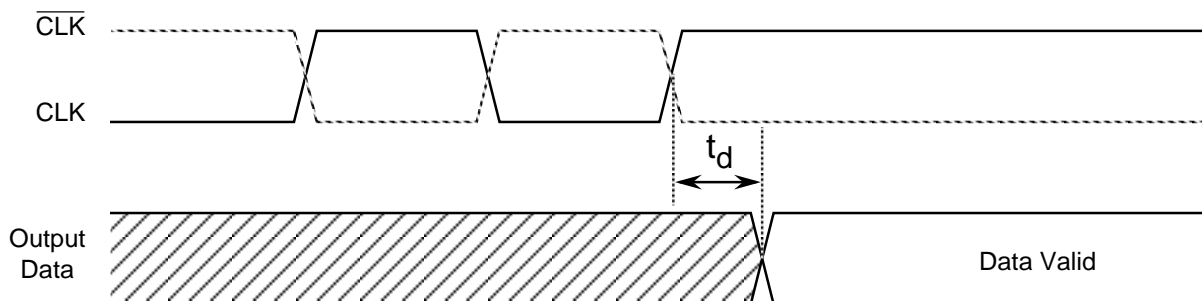


Table I - Timing Parameters

| PARAMETERS | DESCRIPTION | MIN | TYP | MAX | UNITS |
|------------|------------------------------|-----|-----|-----|-------|
| t_d | CLK to Data Valid Prop Delay | - | 5 | - | ns |
| t_{pwH} | CLK High Pulse Width | 10 | - | 300 | ns |
| t_{pwL} | CLK Low Pulse Width | 10 | - | - | ns |

SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

$SINAD = 6.02N + 1.76$, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

± FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

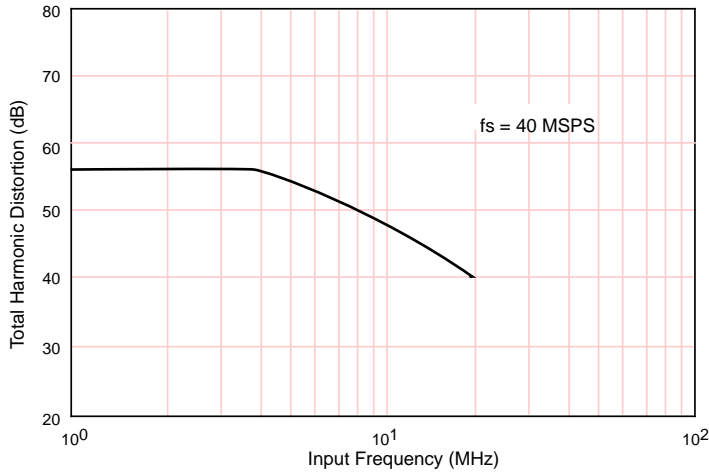
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

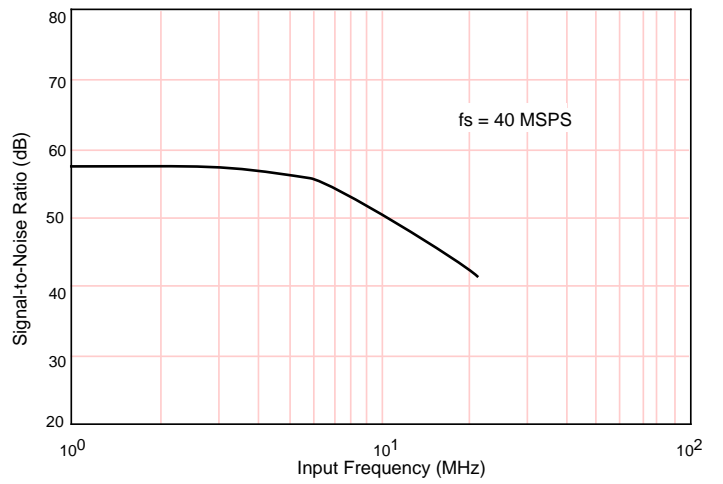
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

TYPICAL PERFORMANCE CHARACTERISTICS

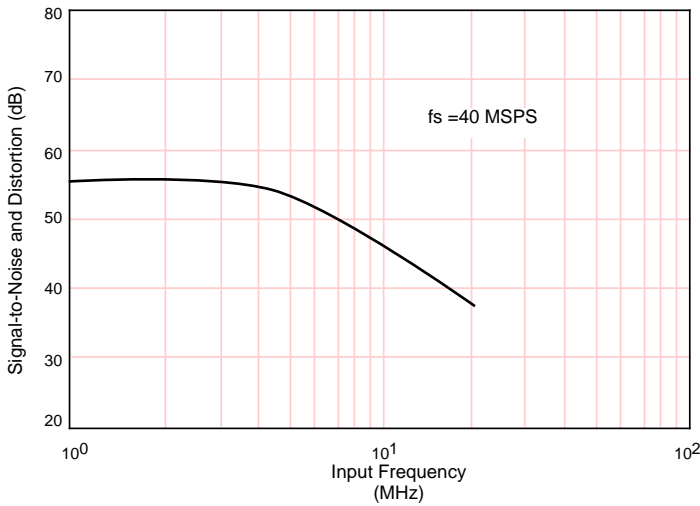
THD vs Input Frequency



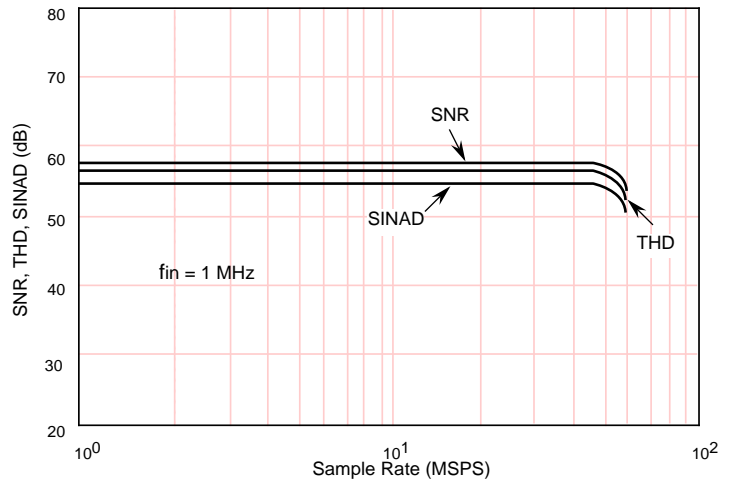
SNR vs Input Frequency



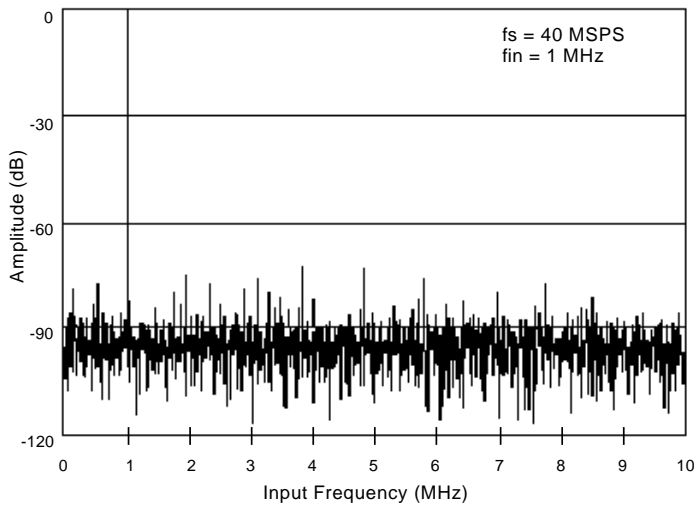
SINAD vs Input Frequency



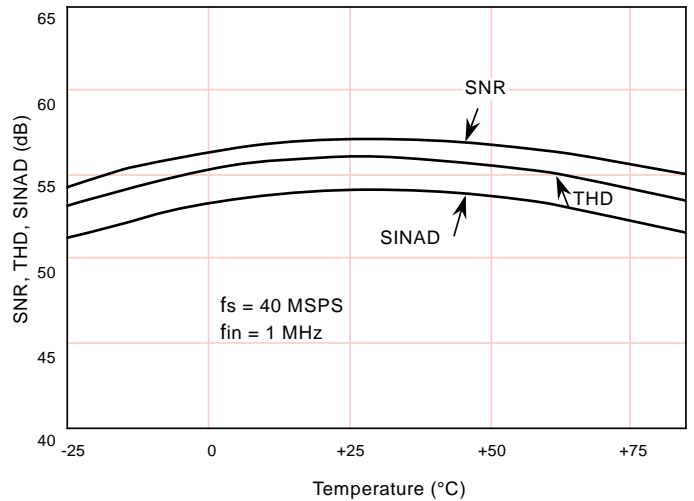
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7814 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7814 in normal circuit operation.

The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7814 requires the use of two supply voltages, V_{EE} and V_{CC} . Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 μF and 10 μF capacitors as shown in figure 2.

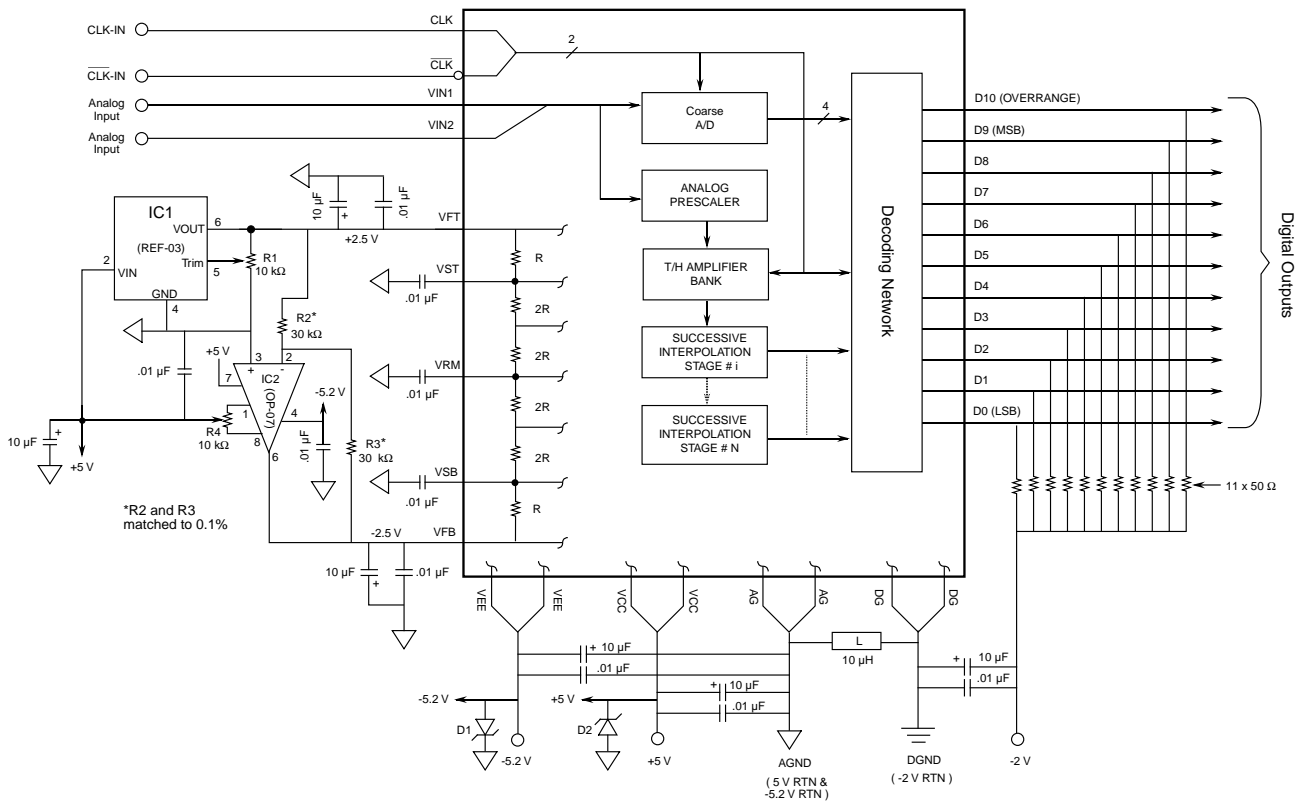
The two grounds available on the SPT7814 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pull-down voltage. These grounds

are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7814. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7814 requires the use of two voltage references: V_{FT} and V_{FB} . V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST} , V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



NOTE: D1=D2=1N5817 or equivalent. (Used to prevent damage caused by power sequencing.)

An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or ± 0.015 V. The potentiometer R1 is 10 k Ω and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB} . If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is $\pm 20\%$ of the recommended reference voltages of V_{FT} and V_{FB} . However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a $\pm 2\%$ range.

The following errors are defined:

$$+FS \text{ error} = \text{top of ladder offset voltage} = \Delta(+FS - V_{ST} + 1 \text{ LSB})$$

$$-FS \text{ error} = \text{bottom of ladder offset voltage} = \Delta(-FS - V_{SB} - 1 \text{ LSB})$$

where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

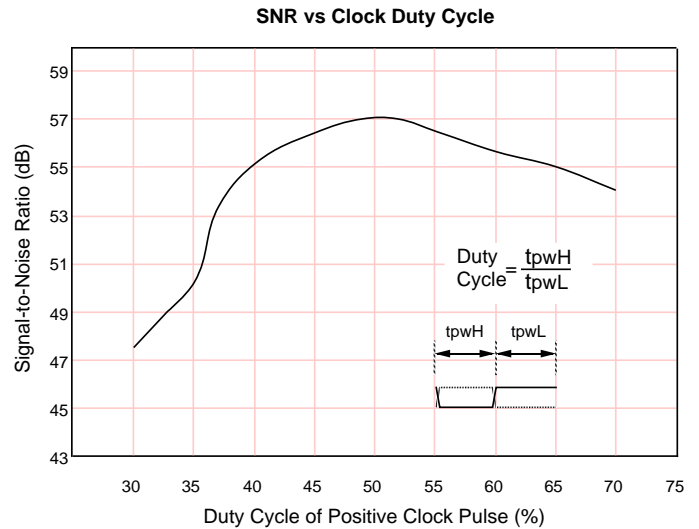
V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input sense and the other for an input force. The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ± 2 volts with $V_{FB} = -2.5$ V and $V_{FT} = +2.5$ V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7814's extremely low input capacitance of only 5 pF and very high input resistance of 300 k Ω . For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μ A.

CLOCK INPUT

The clock inputs (CLK, \overline{CLK}) are designed to be driven differentially with ECL levels. The clock may be driven single ended since \overline{CLK} is internally biased to -1.3 V. \overline{CLK} may be left open, but a .01 μ F bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7814 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See graph.) The analog input signal is latched on the rising edge of the CLK.



DIGITAL OUTPUTS

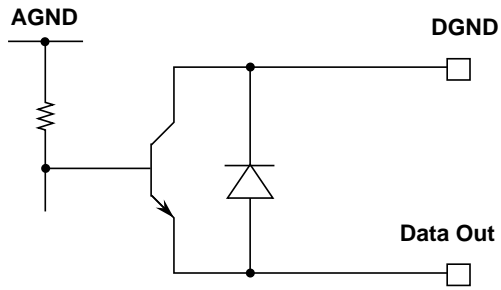
The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Table II - Output Data Information

| ANALOG INPUT | OVERRANGE D10 | OUTPUT CODE D9-D0 |
|-------------------|---------------|--|
| >+2.0 V + 1/2 LSB | 1 | 11 1111 1111 |
| +2.0 V -1 LSB | 0 | 11 1111 111 \emptyset |
| 0.0 V | 0 | $\emptyset\emptyset \emptyset\emptyset\emptyset\emptyset \emptyset\emptyset\emptyset\emptyset$ |
| -2.0 V +1 LSB | 0 | 00 0000 000 \emptyset |
| <-2.0 V | 0 | 00 0000 0000 |

(\emptyset indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



EVALUATION BOARD

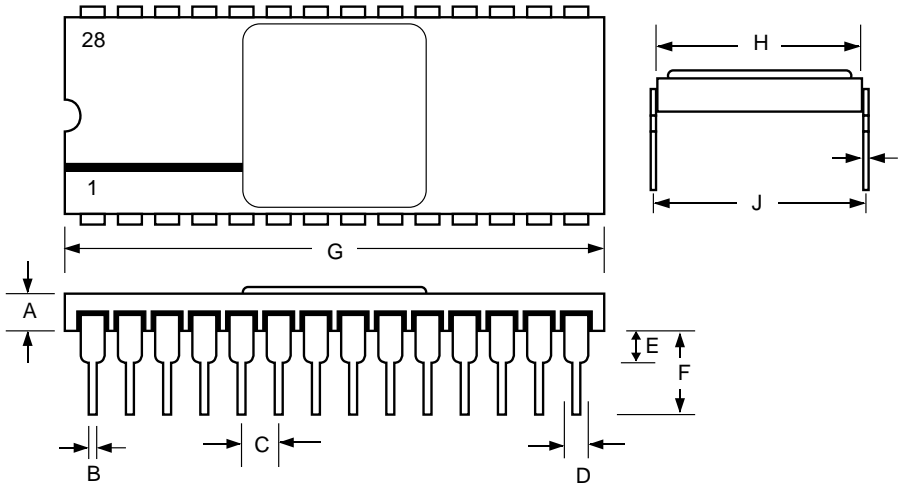
The EB7814 evaluation board is available to aid designers in demonstrating the full performance of the SPT7814. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7814 is also available. Contact the factory for price and availability.

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7814 into higher resolution systems.

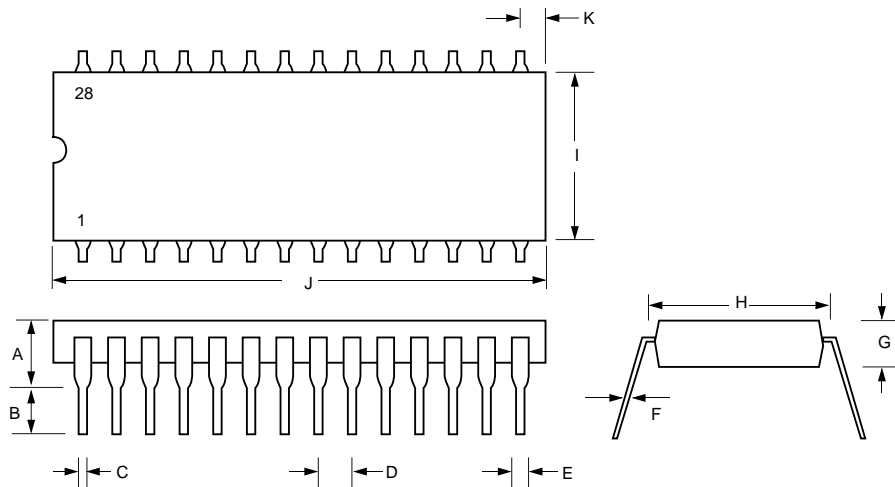
PACKAGE OUTLINES

28-Lead Sidebraced



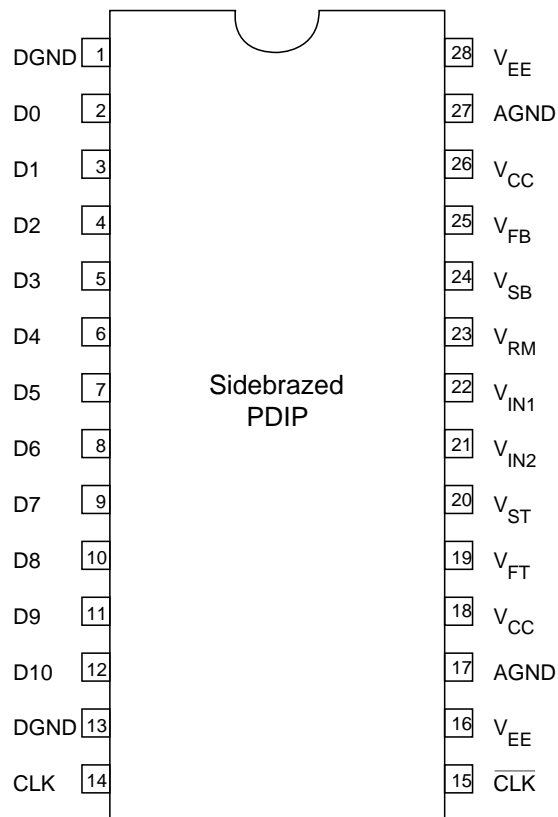
| SYMBOL | INCHES | | MILLIMETERS | |
|--------|--------|----------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.077 | 0.093 | 1.96 | 2.36 |
| B | 0.016 | 0.020 | 0.41 | 0.51 |
| C | 0.095 | 0.105 | 2.41 | 2.67 |
| D | | .050 typ | 0.00 | 1.27 |
| E | 0.040 | 0.060 | 1.02 | 1.52 |
| F | 0.215 | 0.235 | 5.46 | 5.97 |
| G | 1.388 | 1.412 | 35.26 | 35.86 |
| H | 0.585 | 0.605 | 14.86 | 15.37 |
| I | 0.009 | 0.012 | 0.23 | 0.30 |
| J | 0.600 | 0.620 | 15.24 | 15.75 |

28-Lead Plastic DIP



| SYMBOL | INCHES | | MILLIMETERS | |
|--------|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | | 0.200 | | 5.08 |
| B | 0.120 | 0.135 | 3.05 | 3.43 |
| C | | 0.020 | | 0.51 |
| D | | 0.100 | | 2.54 |
| E | | 0.067 | | 1.70 |
| F | | 0.013 | | 0.33 |
| G | 0.170 | 0.180 | 4.32 | 4.57 |
| H | | 0.622 | | 15.80 |
| I | | 0.555 | | 14.10 |
| J | | 1.460 | | 37.08 |
| K | | 0.085 | | 2.16 |

PIN ASSIGNMENTS



PIN FUNCTIONS

| Name | Function |
|-------------------------------------|--------------------------------------|
| DGND | Digital Ground |
| D0-D9 | ECL Outputs (D0=LSB) |
| D10 | ECL Output Overage |
| CLK | Clock Input |
| $\overline{\text{CLK}}$ | Inverted Clock Input |
| V _{EE} | -5.2 V Supply |
| AGND | Analog Ground |
| V _{CC} | +5.0 V supply |
| V _{IN1} , V _{IN2} | Inputs (tied together at the die) |
| V _{FT} | Force for Top of Reference Ladder |
| V _{ST} | Sense for Top of Reference Ladder |
| V _{FB} | Force for Bottom of Reference Ladder |
| V _{SB} | Sense for Bottom of Reference Ladder |
| V _{RM} | Middle of Reference Ladder |

ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE TYPE |
|-------------|-------------------|--------------------|
| SPT7814AIJ | -25 to +85 °C | 28L Sidebraced DIP |
| SPT7814BIJ | -25 to +85 °C | 28L Sidebraced DIP |
| SPT7814ACN | 0 to 70 °C | 28L Plastic DIP |
| SPT7814BCN | 0 to 70 °C | 28L Plastic DIP |
| SPT7814BCU | +25 °C | Die* |

*Please see the die specification for guaranteed electrical performance.

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WARNING - LIFE SUPPORT APPLICATIONS POLICY - SPT products should not be used within Life Support Systems without the specific written consent of SPT. A Life Support System is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in significant personal injury or death.

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.