

#### FEATURES

- 40 MSPS maximum sample rate
- 9.5 effective number of bits at  $f_{IN} = 10$  MHz and  $f_S = 40$  MSPS
- 2 V<sub>P-P</sub> full-scale input range
- Differential input 2.5 V common mode
- Internal or external voltage reference
- Common-mode voltage reference output
- +3.3 V / +5 V digital output logic compatibility
- +5 V analog power supply

#### APPLICATIONS

- High-speed applications where low power dissipation is required
- Video imaging
- Medical imaging
- Radar receivers
- IR imaging
- Digital communications

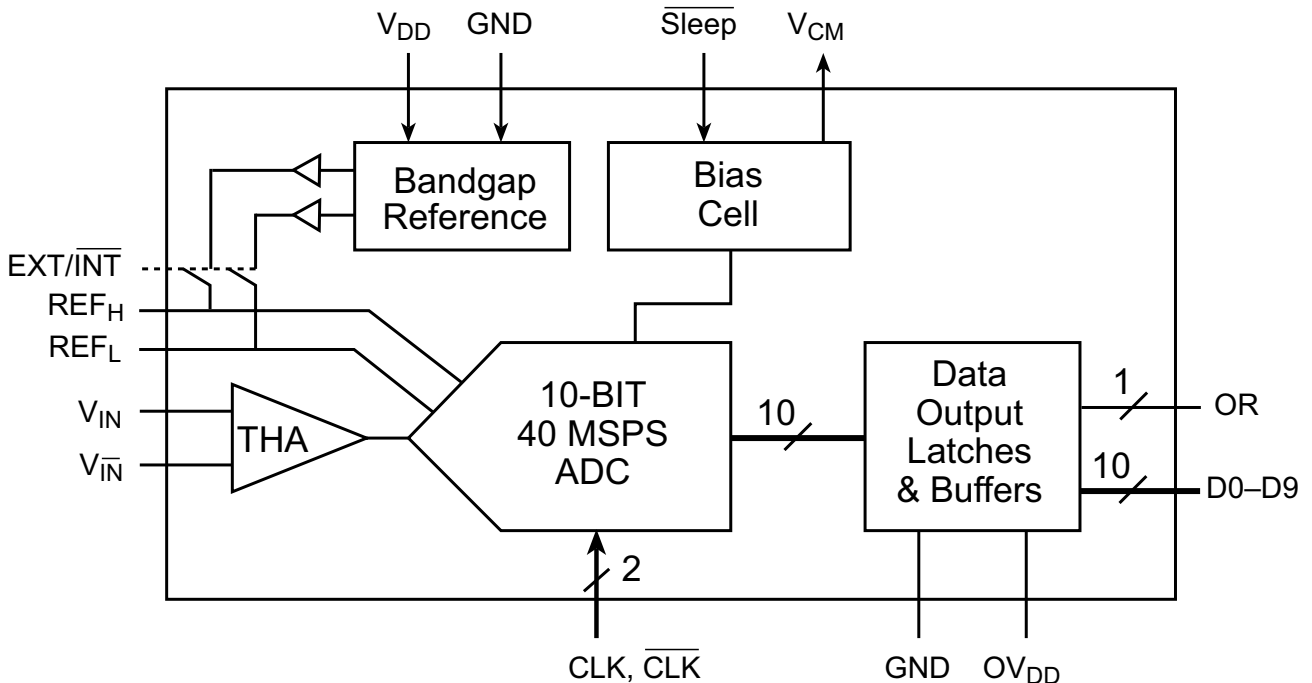
#### GENERAL DESCRIPTION

The SPT7864 is a 10-bit, 40 MSPS analog-to-digital converter with low power dissipation at only 395 mW typical at 40 MSPS with a power supply of +5.0 V. The digital outputs are +3 V or +5 V, and are user selectable. The SPT7864 has incorporated proprietary circuit design and CMOS

processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7864 is available in a 28-lead SSOP package over the industrial temperature range.

#### BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)<sup>1</sup> 25 °C

### Supply Voltages

V <sub>DD</sub> .....	TBD
OV <sub>DD</sub> .....	TBD

### Output

Digital Outputs .....	TBD
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### Input Voltages

Analog Input .....	TBD
CLK Input .....	TBD

### Temperature

Operating Temperature .....	-40 to +85 °C
Storage Temperature .....	-65 to +150 °C

**Note:** 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

## ELECTRICAL SPECIFICATIONS

T<sub>A</sub>=T<sub>MIN</sub> to T<sub>MAX</sub>, V<sub>DD</sub>=+5.0 V, f<sub>S</sub>=40 MSPS, V<sub>RHS</sub>=3.0 V, V<sub>RLS</sub>=2.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	SPT7864 TYP	MAX	UNITS
<b>Resolution</b>			10			Bits
<b>DC Accuracy</b>						
Differential Linearity Error (DLE)	@ +25 °C full temperature	V		±0.4 ±0.75		LSB LSB
Integral Linearity Error (ILE)	@ +25 °C full temperature	V		±0.5 ±1.0		LSB LSB
No Missing Codes		VI		Guaranteed		
<b>Analog Input</b>						
Input Voltage Range (Differential)		V		±1		V
Input Common Mode		V		2.5		V
Input Capacitance		V		2		pF
Common Mode Rejection Ratio (CMRR)				TBD		
<b>Timing Characteristics</b>						
Conversion Rate		VI	40			MSPS
Pipeline Delay (Latency)		IV		7		clocks
Output Delay (t <sub>D</sub> )		IV	TBD	TBD	TBD	ns
Aperture Delay Time		V		TBD		ns
Aperture Jitter Time		V		TBD		ps (rms)
<b>Dynamic Performance</b>						
Effective Number of Bits (ENOB)						Bits
<i>f</i> <sub>IN</sub> = 10 MHz, <i>f</i> <sub>CLK</sub> = 40 MSPS	25 °C	I	9.3	9.5		Bits
	-40 °C to +85 °C	IV	9.0	9.2		Bits
Signal-to-Noise Ratio (SNR)						dB
<i>f</i> <sub>IN</sub> = 10 MHz, <i>f</i> <sub>CLK</sub> = 40 MSPS	25 °C	I	58	59		dB
	-40 °C to +85 °C	IV	57	58		dB
Total Harmonic Distortion (THD)						dB
<i>f</i> <sub>IN</sub> = 10 MHz, <i>f</i> <sub>CLK</sub> = 40 MSPS	25 °C	I		-71	-68	dB
	-40 °C to +85 °C	IV		-70	-67	dB
Signal-to-Noise and Distortion (SINAD)						dB
<i>f</i> <sub>IN</sub> = 10 MHz, <i>f</i> <sub>CLK</sub> = 40 MSPS	25 °C	I	58	59		dB
	-40 °C to +85 °C	IV	56	57		dB
Spurious Free Dynamic Range (SFDR)						dB
<i>f</i> <sub>IN</sub> = 10 MHz, <i>f</i> <sub>CLK</sub> = 40 MSPS	25 °C	I	70	73		dB
	-40 °C to +85 °C	IV	68	71		dB

## ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = +5.0$  V,  $f_S = 40$  MSPS,  $V_{RHS} = 3.0$  V,  $V_{RLS} = 2.0$  V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7864			UNITS
			MIN	TYP	MAX	
<b>Power Supply Requirements</b>						
$V_{DD}$ Voltage (Analog Supply)		IV	4.75	5.0	5.25	V
$OV_{DD}$ Voltage (Output Supply)		IV	2.7	3.3/5.0	5.25	V
$V_{DD}$ Current		VI		74		mA
$OV_{DD}$ Current		VI		8		mA
Power Dissipation						
External Voltage Reference		VI		387	417	mW
Internal Voltage Reference		VI		395	425	mW
Sleep Mode Power Dissipation						
External Voltage Reference		VI		TBD	TBD	mW
Internal Voltage Reference		VI		TBD	TBD	mW
Power Supply Rejection Ratio (PSRR)		V		TBD		mV/V
<b>Internal References</b>						
Common Mode Voltage Reference ( $V_{CM}$ )	$IO = -1 \mu A$	VI	TBD	2.5	TBD	V
Common Mode Voltage Tempco		V		100		ppm/°C
Output Impedance		V		TBD		k $\Omega$
Current Capability		VI		TBD		$\mu A$
Reference Low Output Voltage ( $V_{REFL}$ )	$(EXT/\overline{INT}) = 0$	VI	1.95	2.0	2.05	V
Reference High Output Voltage ( $V_{REFH}$ )	$(EXT/INT) = 0$	VI	2.95	3.0	3.05	V
<b>External References</b>						
Reference Low Input Voltage Range	$(EXT/\overline{INT}) = 1$	IV	1.7	2.0	2.3	V
Reference High Input Voltage Range	$(EXT/INT) = 1$	IV	2.7	3.0	3.3	V
<b>Digital Outputs</b>						
Output Voltage High	$IO = -2$ mA	VI	85% $OV_{DD}$	90% $OV_{DD}$	$OV_{DD}$	V
Output Voltage Low	$IO = 2$ mA	VI		0.2	0.4	V
<b>Digital Inputs</b>						
Input High Voltage		VI	80% $V_{DD}$			V
Input Low Voltage		VI			20% $V_{DD}$	V
Input High Current		VI			$\pm 10$	$\mu A$
Input Low Current		VI			$\pm 10$	$\mu A$
<b>Clock Inputs</b>						
Clock Inputs High Voltage		VI	2		5	V
Clock Inputs Low Voltage		VI			0.4	V

### TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

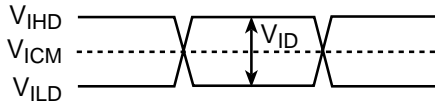
### TEST LEVEL

I  
II  
III  
IV  
V  
VI

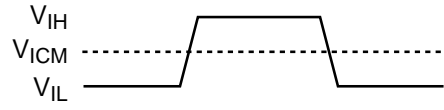
### TEST PROCEDURE

100% production tested at the specified temperature.  
100% production tested at  $T_A = +25$  °C, and sample tested at the specified temperatures.  
QA sample tested only at the specified temperatures.  
Parameter is guaranteed (but not tested) by design and characterization data.  
Parameter is a typical value for information purposes only.  
100% production tested at  $T_A = +25$  °C. Parameter is guaranteed over specified temperature range.

**Figure 1 – Driving Differential Inputs with a Differential Configuration**

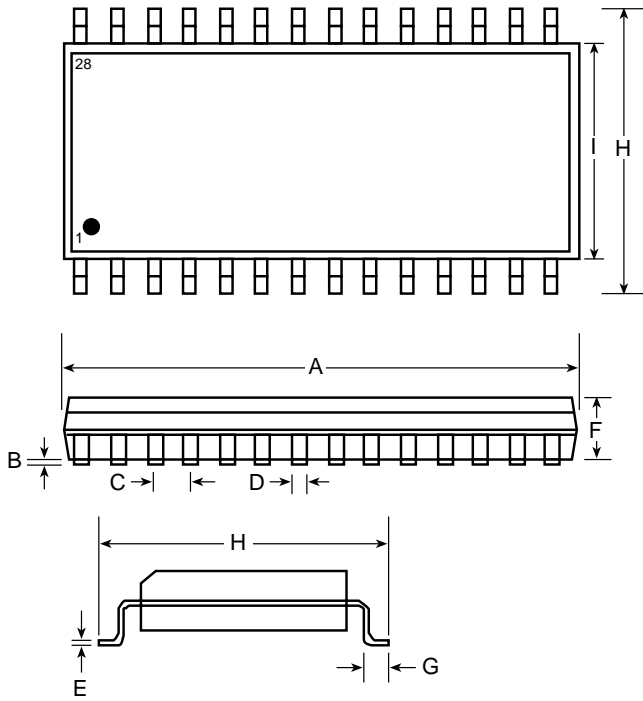


**Figure 2 – Driving Differential Inputs with a Single-Ended Configuration**



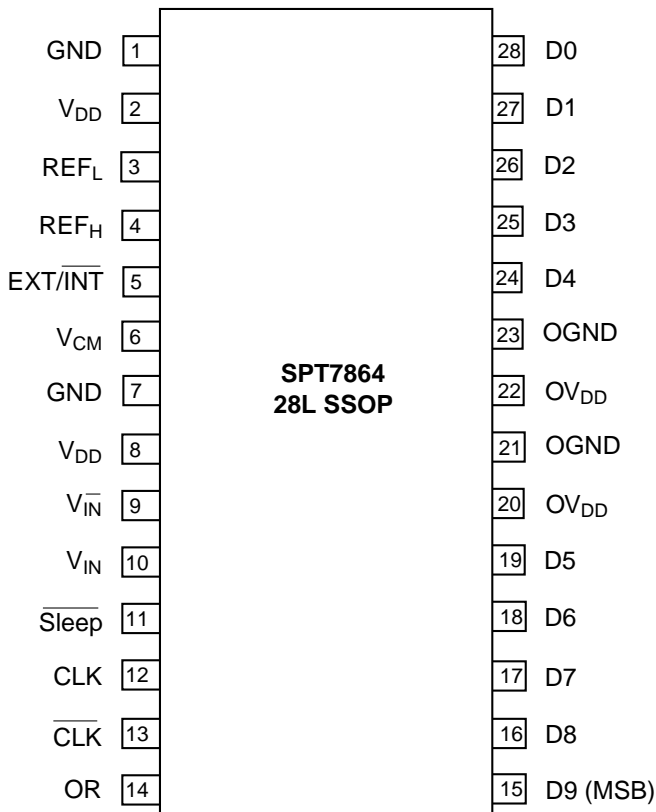
**PACKAGE OUTLINE**

**28-Lead SSOP**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.397	0.407	10.07	10.33
B	0.002	0.008	0.05	0.21
C		0.0256 typ		0.65 typ
D	0.010	0.015	0.25	0.38
E	0.004	0.008	0.09	0.20
F	0.066	0.070	1.68	1.78
G	0.025	0.037	0.63	0.95
H	0.301	0.311	7.65	7.90
I	0.205	0.212	5.20	5.38

## PIN ASSIGNMENTS



## PIN FUNCTIONS

Name	Function
GND	Analog ground
V <sub>DD</sub>	Analog +5 V
OGND	Output ground
OV <sub>DD</sub>	Supply voltage for digital outputs +5 V or +3.3 V
REF <sub>L</sub>	Reference pin low, input for external reference, bypass with capacitor (100 nF) when internal reference is selected.
REF <sub>H</sub>	Reference pin high, input for external reference, bypass with capacitor (100 nF) when internal voltage is selected.
V <sub>CM</sub>	2.5 V common mode voltage reference output
V <sub>IN</sub>	Non-inverted analog input
V <sub>IN</sub>	Inverted analog input
CLK	Clock input pin
CLK	Complement of clock input pin, internally biased to 1.5 V; if single-ended clock is used, bypass to GND with 100 nF
D0–D9	Digital outputs; D0 = LSB; 3.3 V/5 V compatible
OR	Overrange bit; 3.3 V/5 V compatible
EXT/INT	EXT/INT = 1, external reference used; internal reference powered down EXT/INT = 0, internal reference used; internally pulled down
Sleep	Sleep = 1, normal operation; internally pulled up Sleep = 0, powered-down mode

## ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7864SIR	–40 to +85 °C	28L SSOP

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Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.