HCMP96850

SINGLE ULTRAFAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay of 2.4 ns (typ)
- Propagation Delay Skew <300 ps
- Low Offset ±3 mV
- Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

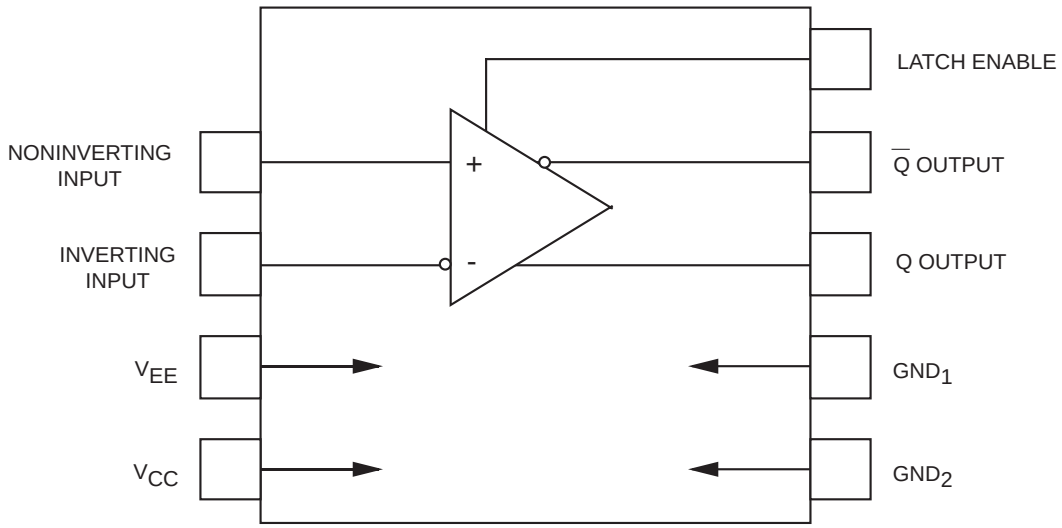
GENERAL DESCRIPTION

The HCMP96850 is a single, very high speed monolithic comparator. It is pin-compatible with and has improved performance over the AD9685 and the AM6685. The HCMP96850 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96850 is available in a 16-lead ceramic DIP package over the industrial temperature range. It is also available in die form.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Positive Supply Voltage (V_{CC} to GND) .... -0.5 to +6.0 V
- Negative Supply Voltage (V_{EE} to GND) ... -6.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltages
- Input Voltage ..... -4.0 to +4.0 V
- Differential Input Voltage ..... -5.0 to +5.0 V
- Input Voltage, Latch Controls ..... V_{EE} to 0.5 V

Output
- Output Current ..... 30 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 60 seconds) ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.2 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms[1]	IV	-3		+3	mV
Input Offset Voltage (V_{os})	R_S = 0 Ohms,[1] $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
(V_{os}) Tempco		V		4		µV/°C
Input Bias Current		I		4	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7		µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		3.3	5	mA
Negative Supply Current		I		13.5	18	mA
Positive Supply Voltage, V_{CC}		IV	+4.75	+5.0	+5.25	V
Negative Supply Voltage, V_{EE}		IV	-4.95	-5.2	-5.45	V
Input Common Mode Range		I	-2.5		+2.5	V
Latch Enable Common Mode Range		IV	-2		0	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	V		70		dB
Common Mode Rejection Ratio		V		80		dB
Power Dissipation	I_{OUTPUT} = 0 mA	IV		90	120	mW

ELECTRICAL SPECIFICATIONS

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[2]						
Propagation Delay	10 mV O.D.	III		2.4	3.0	ns
Latch Set-up Time		IV		0.6	1	ns
Latch to Output Delay	50 mV O.D.	IV			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		IV			0.5	ns
Rise Time	20% to 80%	V		1.76		ns
Fall Time	20% to 80%	V		1.76		ns

[1] R_S = source impedance.
[2] 100 mV input step.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

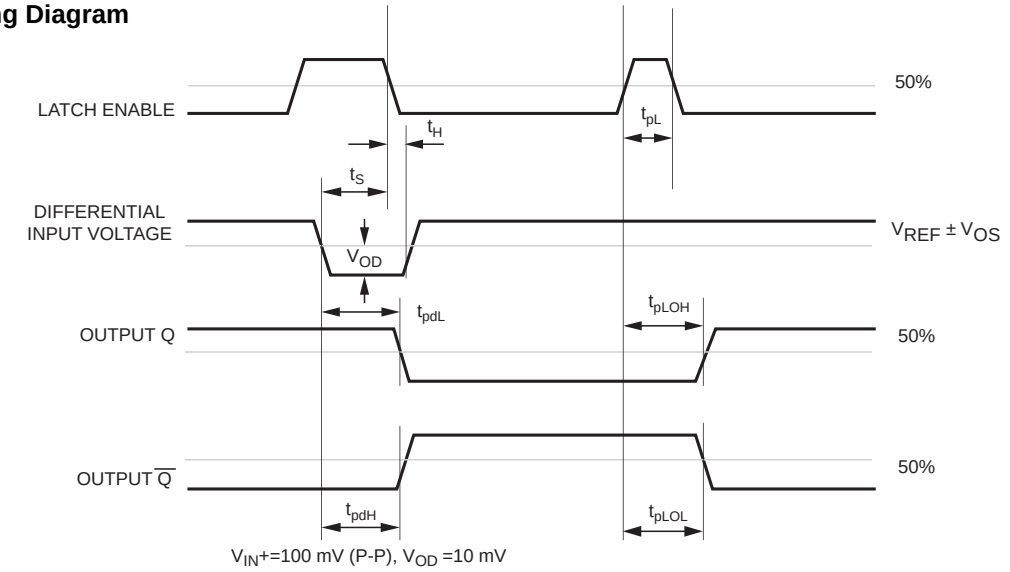
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

TIMING INFORMATION

The timing diagram for the comparator is shown in figure 1. The latch enable (LE) pulse is shown at the top. If LE is high in the HCMP96850, the comparator tracks the input difference voltage. When LE is driven low, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of a 10 mV overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the latch enable falling edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may or may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the input reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

V_{OD} VOLTAGE OVERDRIVE - The difference between the differential input and reference input voltages.

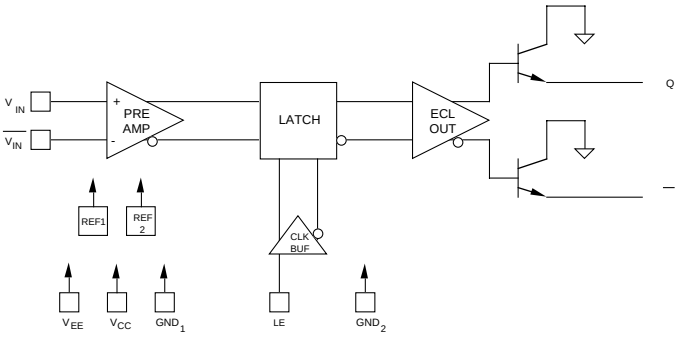
t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

Figure 2 - Internal Function Diagram



GENERAL INFORMATION

The HCMP96850 is an ultrahigh speed single voltage comparator. It offers tight absolute characteristics which guarantee matching from package to package. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

The HCMP96850 has one latch enable control and should be driven by standard ECL logic levels. It also has two separate ground pins, one for the output to accommodate large ground currents without affecting the rest of the circuit, while the other is for the small signal intermediate stages. The input stage is referenced to V_{CC} and V_{EE}.

TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96850 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. All voltage supply pins should be decoupled with high-frequency capacitors as close to the device as possible. All ground pins and no connects should be connected to a common ground plane to further improve noise immunity.

On the HCMP96850, all outputs, whether used or unused, should have identical terminations to minimize ground current switching.

Figure 3 - Typical Interface Circuit

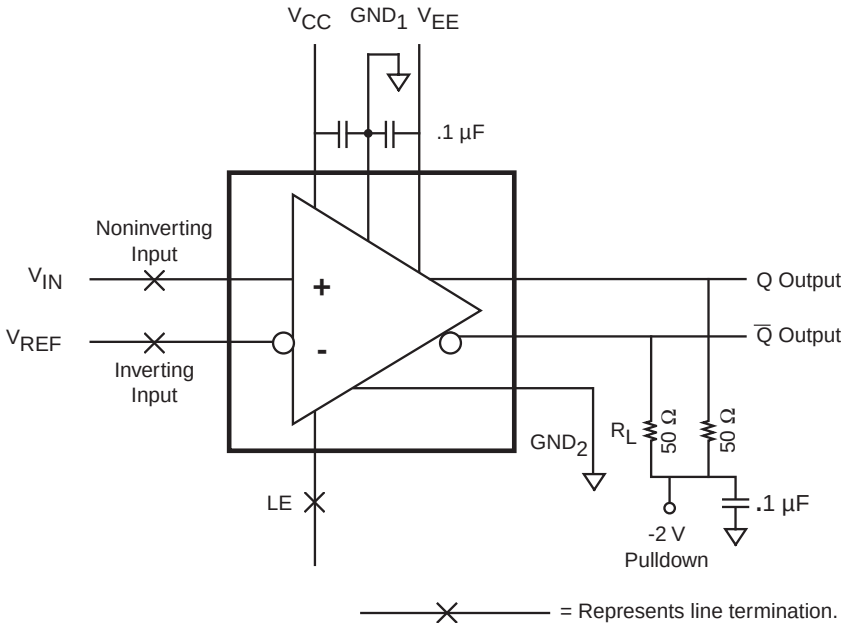


Figure 4 - Equivalent Input Circuit

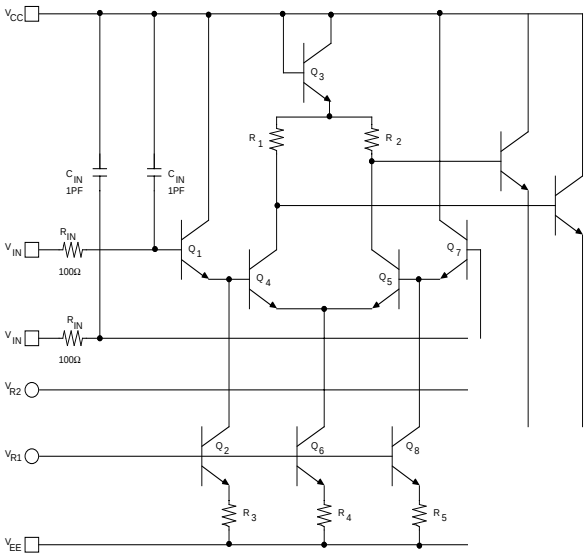


Figure 5 - Output Circuit

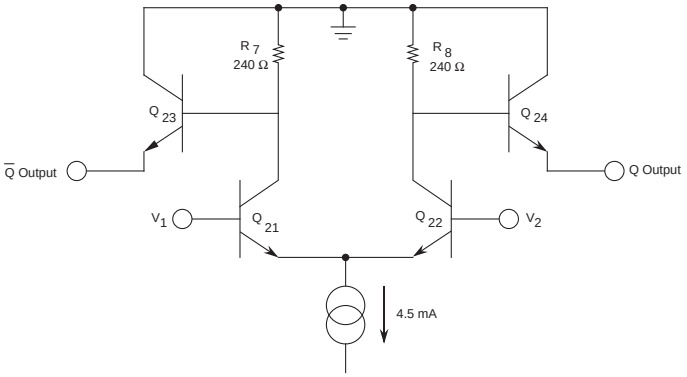


Figure 6 - Test Load

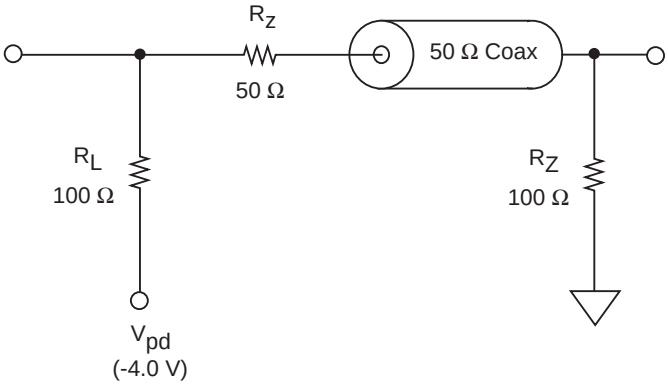
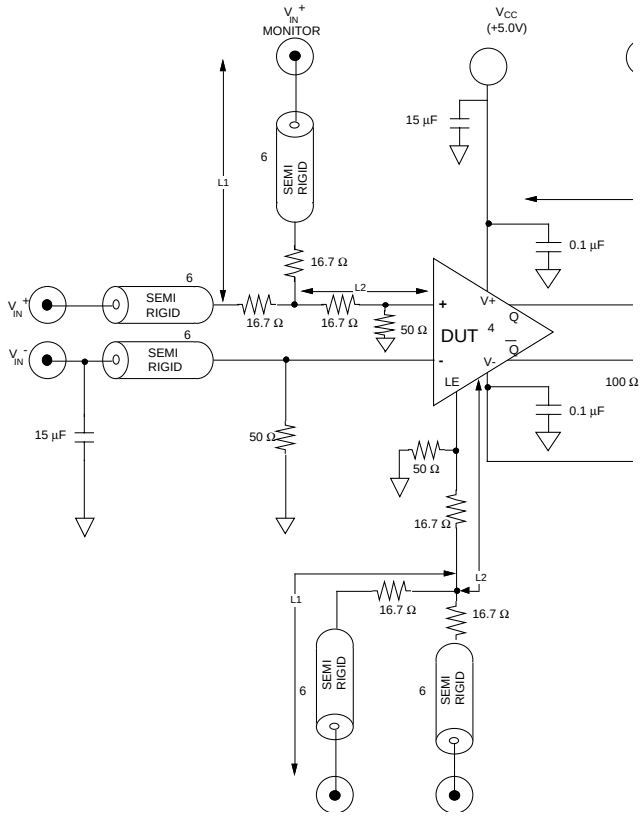


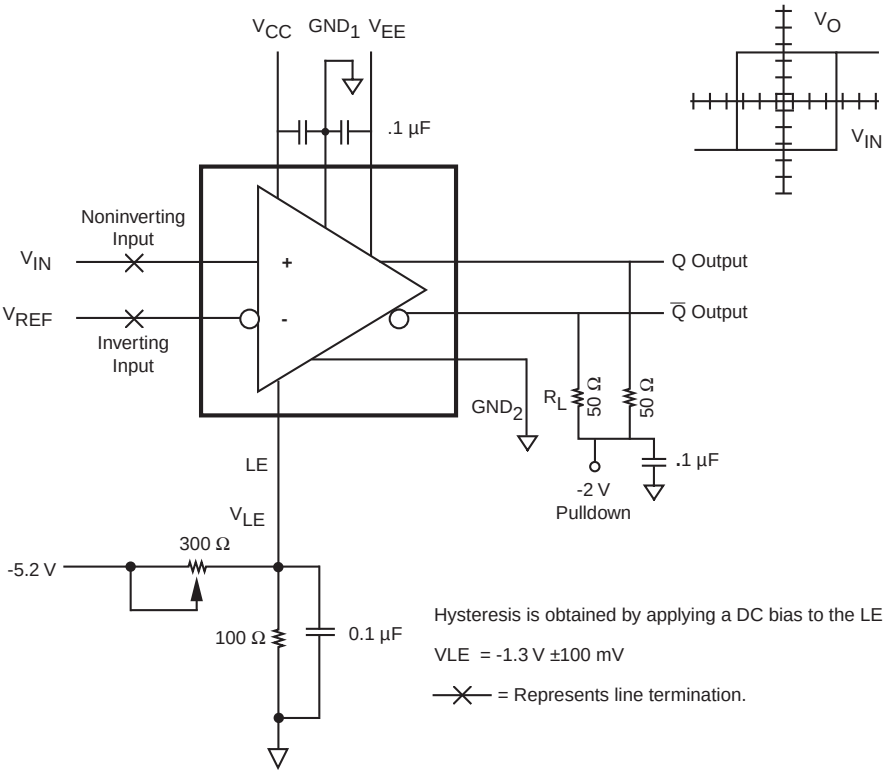
Figure 7 - AC Test Fixture



L3

NOTES:
1. ALL BNC & SEMIRIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (10 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMIRIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

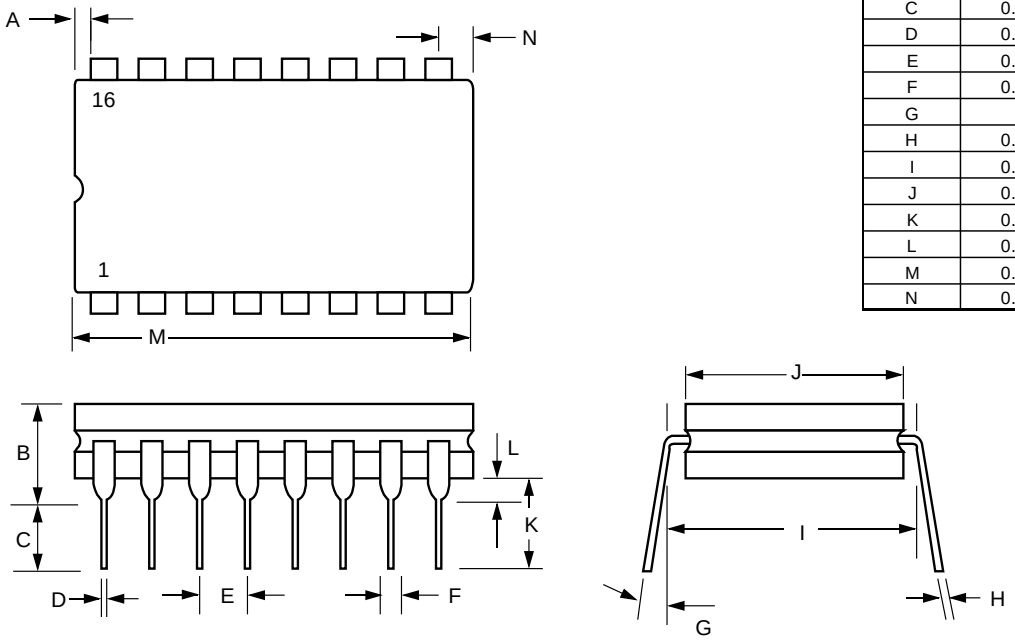
Figure 8 - HCMP96850 with Hysteresis



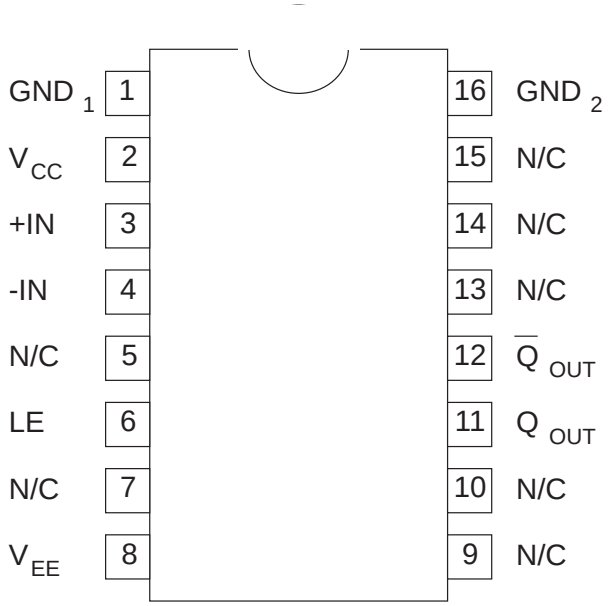
PACKAGE OUTLINE

16-Lead Cerdip

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B		0.200		5.08
C	0.125	0.150	3.18	3.81
D	0.015	0.023	0.38	0.58
E	0.090	0.110	2.29	2.79
F	0.030	0.065	0.76	1.65
G	0°	15°	0°	15°
H	0.008	0.015	0.20	0.38
I	0.290	0.320	7.37	8.13
J	0.250	0.310	6.35	7.87
K	0.140	0.200	3.56	5.08
L	0.015	0.050	0.38	1.27
M	0.745	0.785	18.92	19.94
N	0.015	0.050	0.38	1.27



PIN ASSIGNMENTS



16 LEAD DIP

PIN FUNCTIONS

Name	Function
GND_1	Circuit Ground
V_{CC}	Positive Supply Voltage
+IN	Noninverting Input
-IN	Inverting Input
N/C	No Connection
LE	Latch Enable
V_{EE}	Negative Supply Voltage
Q_{OUT}	Output
$\overline{Q}_{OUT}$	Inverted Output
GND_2	Output Ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
HCMP96850SID	-25 to +85 °C	16-Lead Cerdip
HCMP96850SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.