SPT9687

DUAL ULTRAFAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay <2.3 ns
- Propagation Delay Skew <300 ps
- Low Power: 185 mW
- Low Offset ±3 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- High-Speed Instrumentation, ATE
- High-Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

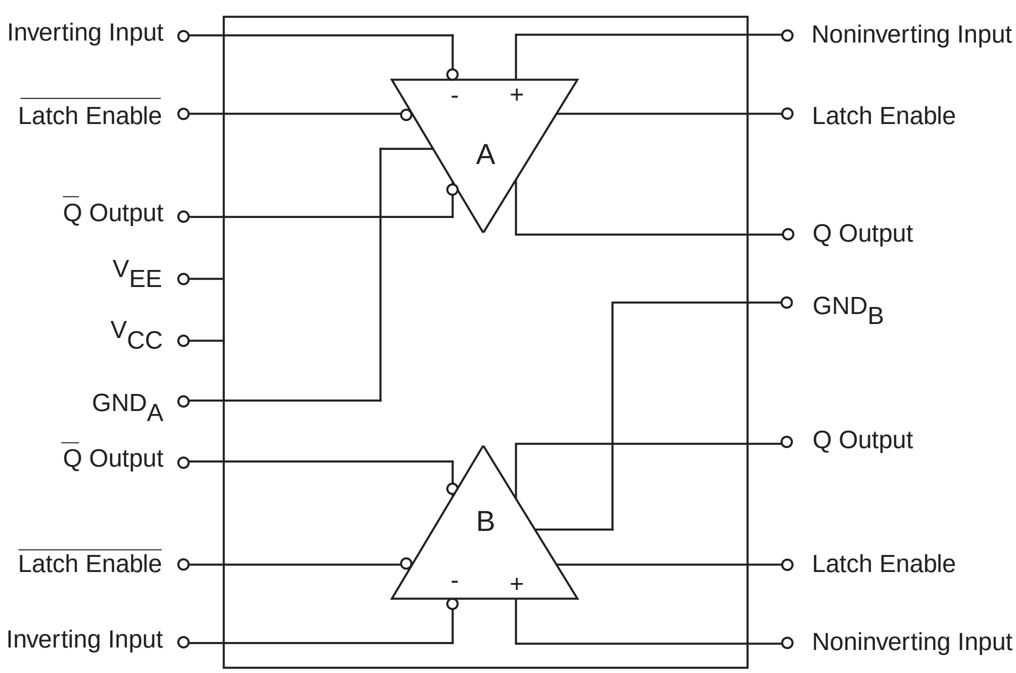
GENERAL DESCRIPTION

The SPT9687 is a dual, very high-speed monolithic comparator. It is pin compatible with, and has improved performance over Analog Device's AD9687. The SPT9687 is designed for use in Automatic Test Equipment (ATE), high-speed instrumentation, and other high-speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The SPT9687 is available in 16-lead SOIC, 16-lead plastic DIP, 20-lead PLCC and 20-contact LCC packages over the industrial temperature range. It is also available in die form.

BLOCK DIAGRAM



Signal Processing Technologies, Inc.
4755 Forge Road, Colorado Springs, Colorado 80907, USA
Phone: (719) 528-2300 FAX: (719) 528-2370 Website: http://www.spt.com E-Mail: sales@spt.com

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply (V_{CC} to GND) .... -0.5 to +6.0 V
Negative Supply (V_{EE} to GND) .... -6.0 to +0.5 V
Ground Voltage Differential .... -0.5 to +0.5 V

Input Voltages

Input Voltage .... -4.0 to +4.0 V
Differential Input Voltage .... -5.0 to +5.0 V
Input Voltage, Latch Controls .... V_{EE} to 0.5 V

Output

Output Current .... 30 mA

Temperature

Operating Temperature, ambient .... -25 to +85 °C
junction .... +150 °C
Lead Temperature, (soldering 60 seconds) ...... +300 °C
Storage Temperature .... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9687 MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms[1]	III	-3	±.5	+3	mV
Input Offset Voltage	R_S = 0 Ohms[1] T_{MIN} <T_A<T_{MAX}	IV	-3.5		+3.5	mV
Offset Voltage Tempco		V		4		µV/°C
Input Bias Current		I		6	±20	µA
Input Bias Current	T_{MIN} <T_A<T_{MAX}	IV		7	±38	µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	T_{MIN} <T_A<T_{MAX}	IV	-1.5		+1.5	µA
Input Common Mode Range		I	-2.5		+2.5	V
Latch Enable Common Mode Range		IV	-2.0		0	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	IV	50	100		dB
Common Mode Rejection Ratio		IV	50	85		dB
Positive Supply Current		I		7	11	mA
Negative Supply Current		I		27	37	mA
Positive Supply Voltage		IV	4.75	5.0	5.25	V
Negative Supply Voltage		IV	-4.95	-5.2	-5.45	V
Power Dissipation	I_{OUTPUT} = 0 mA	I		185	250	mW
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[2]						
Propagation Delay	10 mV OD	III		2.0	2.3	ns
Latch Set-up Time		IV		0.6	1	ns

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9687 MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[2]						
Latch to Output Delay	50 mV OD	IV			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		IV			0.5	ns
Rise Time	20% to 80%	V		1.2		ns
Fall Time	20% to 80%	V		1.2		ns

[1]R_S = Source impedance.
[2]100 mV input step.

TEST LEVEL CODES

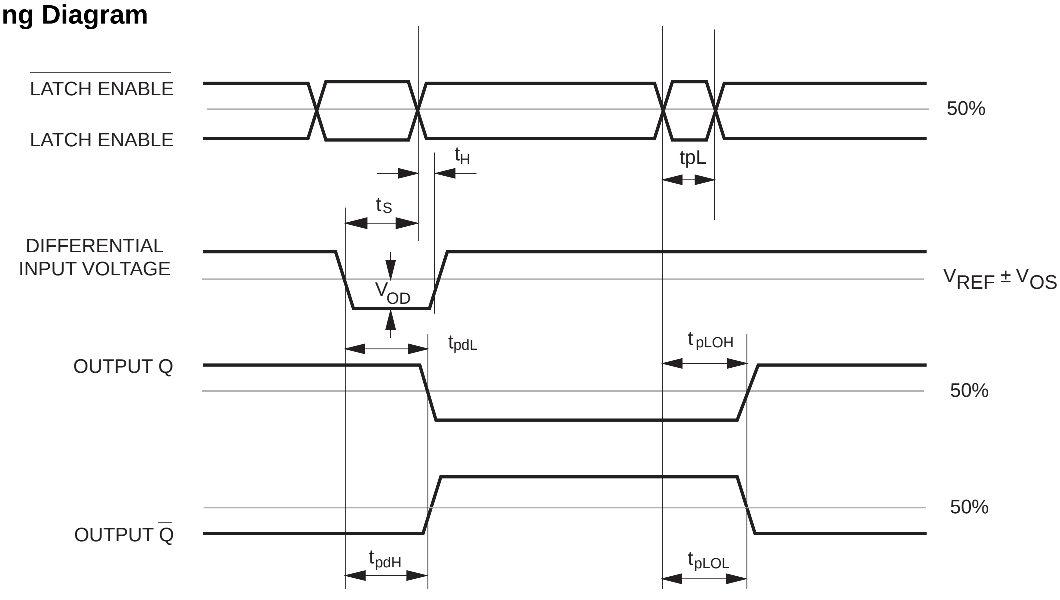
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



V_{IN}+ = 100 mV (p-p), V_{OD} = 50 mV

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

V_{OD} VOLTAGE OVERDRIVE - The difference between the differential input and the reference voltages.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

TIMING INFORMATION

The timing diagram for the comparator is shown in figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the SPT9687, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of a 50 mV overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

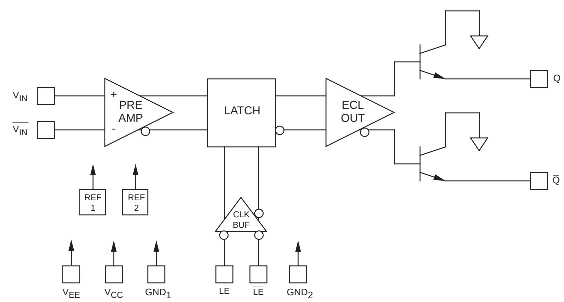
GENERAL INFORMATION

The SPT9687 is an ultrahigh-speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9687 has a complementary latch enable control for each comparator. Both should be driven by standard ECL logic levels.

The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

Figure 2 - Internal Functional Diagram



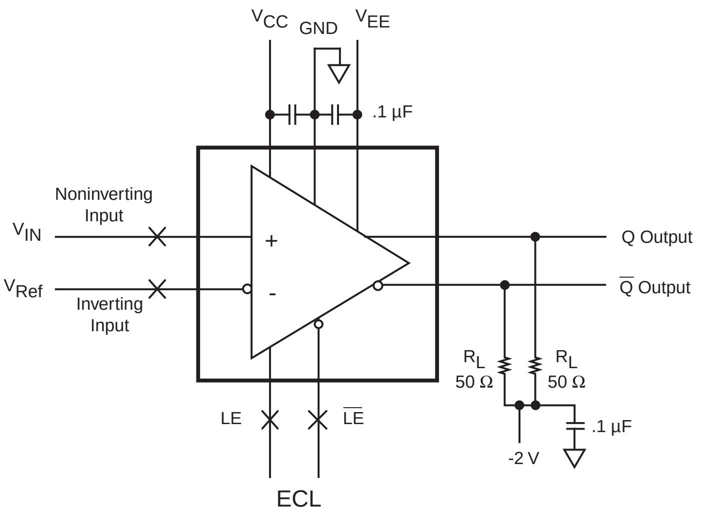
TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be met to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9687 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, and the input impedance to the part should be kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. All supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible. All ground and N/C pins should be connected to the same ground plane to further improve noise immunity and shielding. If using the SPT9687 as a single comparator, the outputs of the inactive comparator can be grounded, left open or terminated with 50 Ohms to -2 V. All outputs on the active comparator, whether used or unused, should have identical terminations to minimize ground current switching transients.

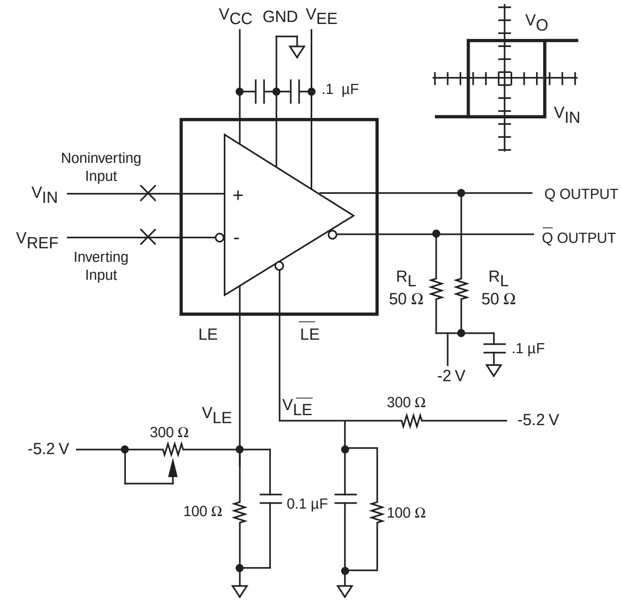
Note: To ensure proper power up of the device, the input should be kept below +1.5 V during power up.

Figure 3 - Typical Interface Circuit



= Represents line termination.

Figure 4 - Typical Interface With Hysteresis



Hysteresis is obtained by applying a DC bias to the LE pin.

V_{LE} = -1.3 V ±100 mV, $V_{\overline{LE}}$ = -1.3 V.

Represents line termination.

Figure 5 - Equivalent Input Circuit

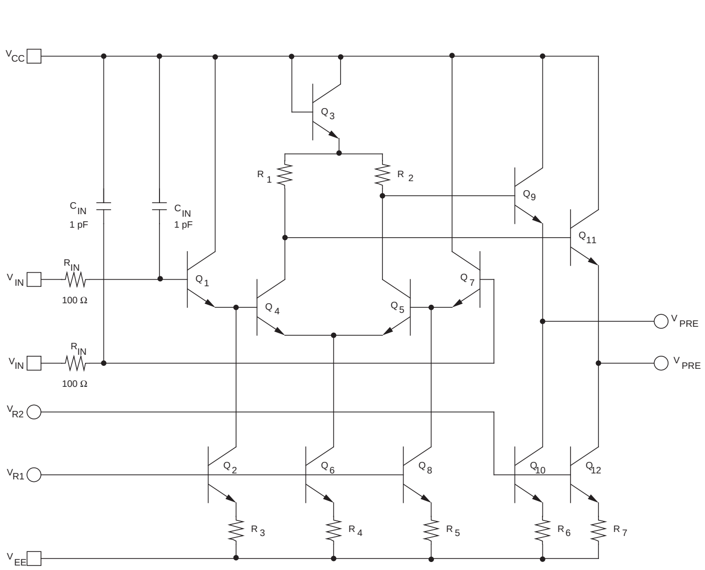


Figure 6 - AC Test Fixture

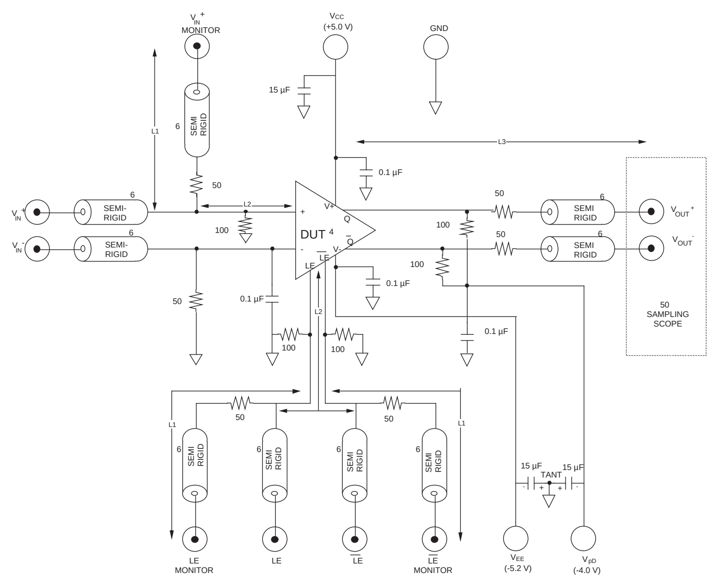


Figure 7 - Output Circuit

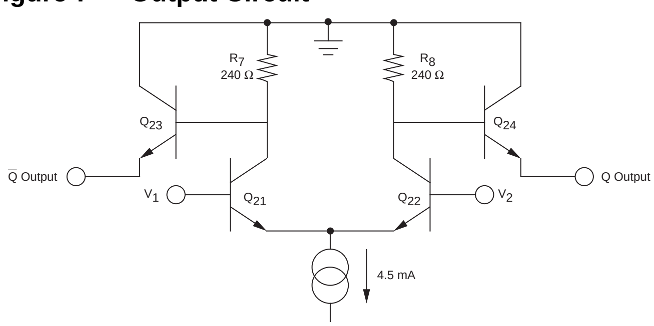
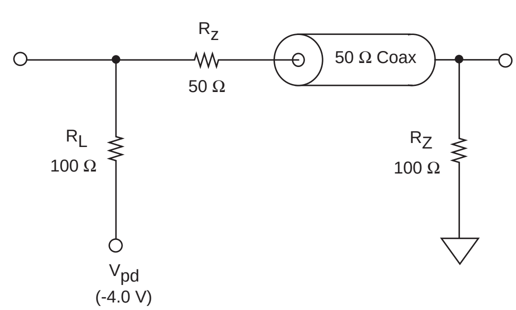


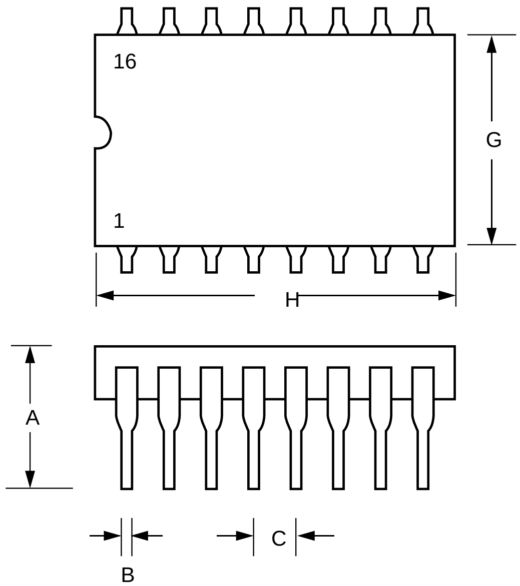
Figure 8 - Test Load

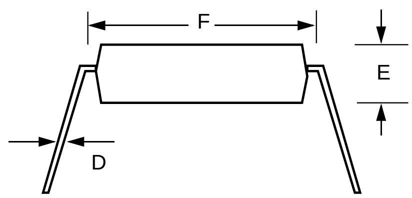


PACKAGE OUTLINES

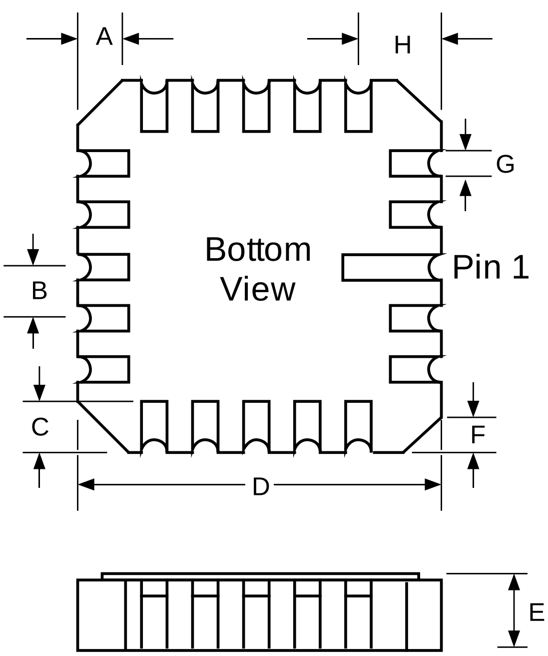
16-Lead Plastic DIP

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.300		7.62
B	0.014	0.026	0.36	0.66
C		.100 typ		2.54
D		.010 typ		0.25
E	1.150	1.950	29.21	49.53
F	0.290	0.330	7.37	8.38
G	0.246	0.254	6.25	6.45
H	0.740	0.760	18.80	19.30





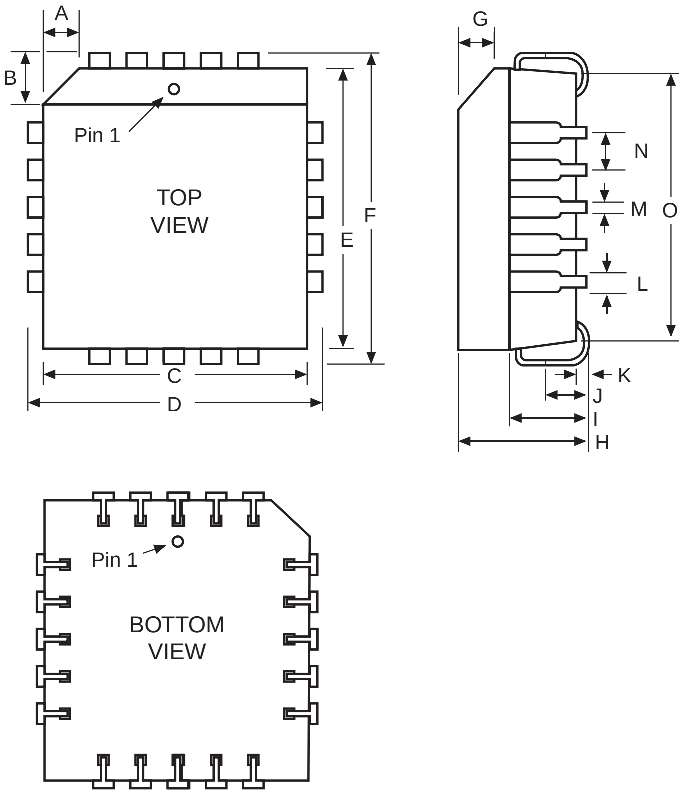
20-Contact Leadless Chip Carrier (LCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 typ		1.02
B		.050 typ		1.27
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F		.020 typ		0.51
G	0.022	0.028	0.56	0.71
H		0.075		1.91

PACKAGE OUTLINES

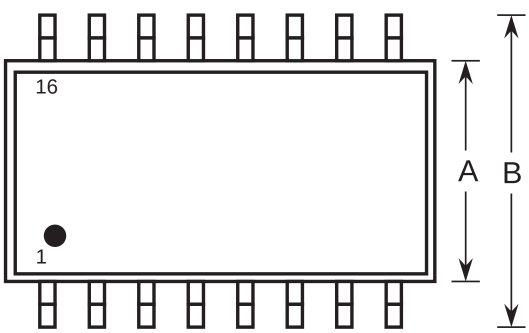
20-Lead Plastic Leaded Chip Carrier (PLCC)

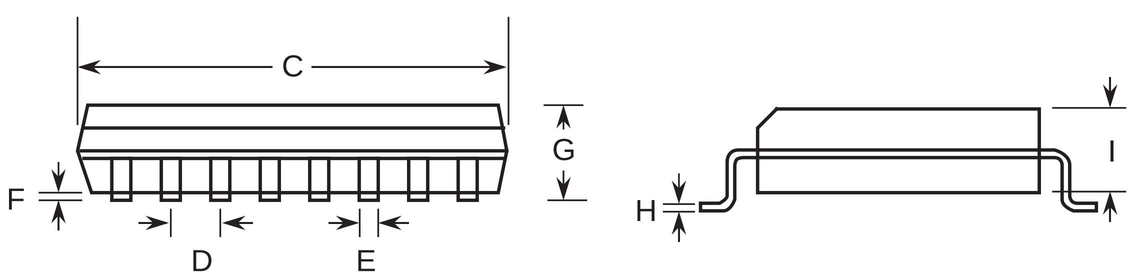


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.045 typ		1.14
B				
C	0.350	0.356	8.89	9.04
D	0.385	0.395	9.78	10.03
E	0.350	0.356	8.89	9.04
F	0.385	0.395	9.78	10.03
G	0.042	0.056	1.07	1.42
H	0.165	0.180	4.19	4.57
I	0.085	0.110	2.16	2.79
J	0.025	0.040	0.64	1.02
K	0.015	0.025	0.38	0.64
L	0.026	0.032	0.66	0.81
M	0.013	0.021	0.33	0.53
N		0.050		1.27
O	0.290	0.330	7.37	8.38

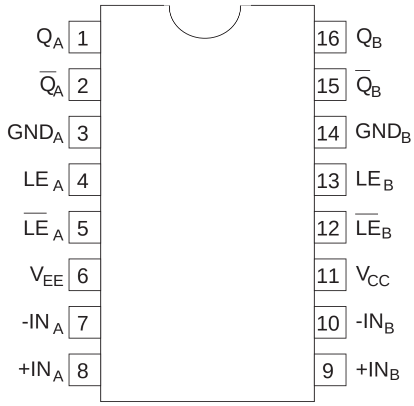
16-Lead Small Outline Integrated Circuit (SOIC)

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.150	0.157	3.81	3.99
B	0.230	0.244	5.84	6.20
C	0.386	0.393	9.80	9.98
D	.050 Typ		1.27 Typ	
E	0.0138	0.0192	0.35	0.49
F	0.004	0.0098	0.127	0.25
G	0.061	0.068	1.55	1.73
H	0.0075	0.0098	0.19	0.25
I	0.055	0.061	1.40	1.55

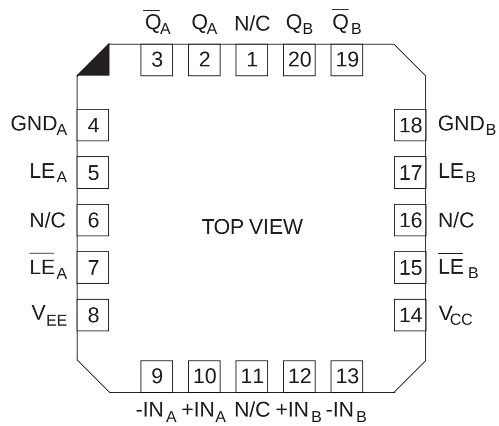




PIN ASSIGNMENTS



PDIP/SOIC



LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Latch Enabled B
$\overline{LE}_B$	Inverted Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

ORDERING INFORMATION

PART NUMBER	Temperature Range	PACKAGE TYPE
SPT9687SIN	-25 to +85 °C	16L PDIP
SPT9687SIP	-25 to +85 °C	20L PLCC
SPT9687SIC	-25 to +85 °C	20C LCC
SPT9687SIS	-25 to +85 °C	16L SOIC
SPT9687SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.

WARNING - LIFE SUPPORT APPLICATIONS POLICY - SPT products should not be used within Life Support Systems without the specific written consent of SPT. A Life Support System is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in significant personal injury or death.

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.