Solid State
Micro Technology
for Music

SSM 2300

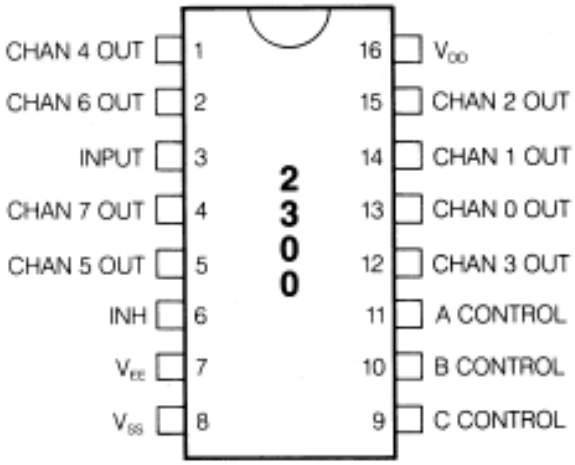
8 CHANNEL MULTIPLEXED SAMPLE AND HOLD®*

DESCRIPTION

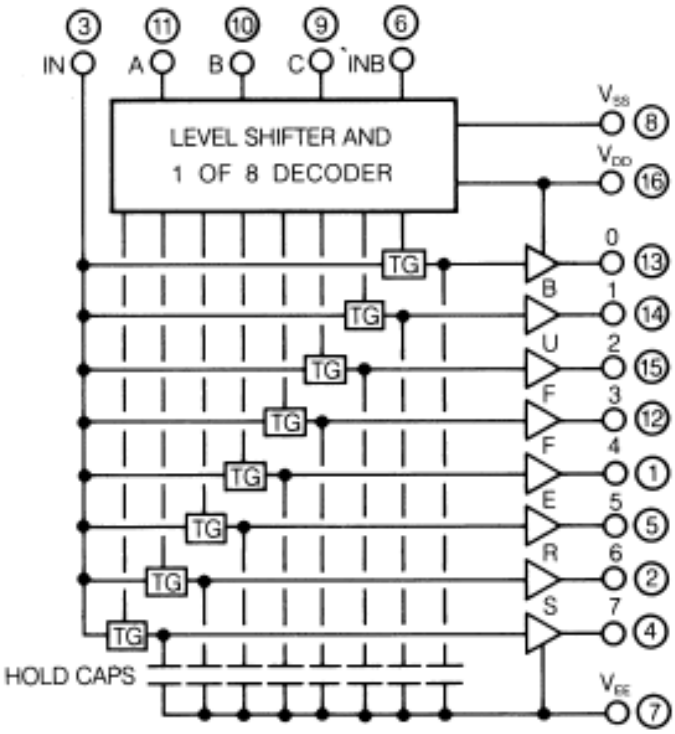
The SSM 2300 is an eight channel CMOS multiplexed sample and hold I.C. designed for data distribution in μP controlled systems. The device can be easily retrofitted into an existing 4051 socket used for this application replacing it and its external discretes with the advantage that the high impedance hold points are internal to the I.C., eliminating manufacturing and reliability problems. With a 15 volt supply, a channel can acquire an 8 bit input signal to ½ LSB in less than two microseconds allowing over 8 full band audio signals to be simultaneously demultiplexed from a single DAC. Near D.C., almost any number of 2300s can be paralleled for process control applications. The output swing includes the negative supply and the chip can operate off single or dual supplies from 5 to 18 volts total. The control inputs are both TTL and CMOS compatible over most of the full supply range.

FEATURES

- High Accuracy (8 Bits Absolute, 12 Bits Linearity)
- Low Droop Rate (≤ 50 mV/Second)
- Retrofits 4051 Used as Demultiplexer
- 5 to 18 Volts Total Supply Operation
- Internal High Z Hold Points
- Output Swing Includes Negative Supply
- TTL and CMOS Compatible Logic Inputs
- Low Cost
- Fast Acquisition Time
- Output Buffers Stable for C_L ≤500pF



PIN OUT (TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM

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*PATENTS PENDING

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OPERATING TEMPERATURE
−25°C to +75°C

STORAGE TEMPERATURE
−55°C to +125°C

The following specifications apply for V_{DD} = +15V, V_{EE} = V_{SS} = GND, and T_A = 25°C unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Current I_{DD}	2	4	8	mA	
Total Supply Range ($V_{DD} - V_{EE}$)	5		18	V	
Positive Supply V_{DD}	5		18	V	
Negative Supply V_{EE}	−10		0	V	
Logic Supply V_{SS}	−10		0	V	
Logic High (A, B, C, INH)	6			V	Also see
Logic Low (A, B, C, INH)			0.8	V	Table 1
Channel Select Time		300		nS	
Channel Deselect Time		300		nS	
Inhibit Recovery Time		150		nS	
Buffer Offset V_{OS}	−30	±8	+30	mV	0 ≤ Vin ≤ +13V
Hold Step V_{HS}		4	8	mV	0 ≤ Vin ≤ +13V
Acquisition Time		2		µS	0 ≤ Vin ≤ +13V
Droop Rate		50	150	mV/sec	
Output Source Current	1.2			mA	0 ≤ Vout ≤ +13V
Output Sink Current	0.5			mA	$V_{OUT} = V_{EE}$
Input/Output Voltage Range	0		13	V	R_{OL} = 10K to GND
Maximum Output Capacitive Load		500		pF	

*Final specifications may be subject to change

GENERAL

Handling

By design consideration, the SSM 2300 gate inputs have a resistor/diode gate protection network. Inherent p-n junction diodes provide diode protection for all gate inputs and outputs. At input and output interfaces, the diode networks of the SSM 2300 are protected from gate-oxide failure (70 to 100 volt limit) for static discharge or signal voltages up to 1 to 2 kilovolts under most transient or low current conditions.

In spite of design considerations leading to protection against electrostatic effects, special care should be exercised as follows:

1. All persons handling the SSM 2300 should wear grounded wrist straps.
2. Table and floor surfaces in areas which the SSM 2300 is handled should be covered with conductive mats.
3. Conductive plastic tubes, bags, and trays should be used for storage and conveyance.
4. Soldering iron tips and test equipment should be grounded.

Operating

Unused Inputs

Connect all unused input leads to either V_{SS} or V_{DD} depending on the appropriate logic circuit. For Printed Circuit [redacted] mounted inputs which may temporarily become unterminated, a pull-up resistor to V_{SS} or V_{DD} should be used, with a value range from 0.2 to 1 megaohm.

Input Signals

Do not apply signals to the SSM 2300 with power off, unless the input current's steady state value is limited to less than 10mA.

SUPPLIES (Pins 7, 8, and 16)

The supply voltages V_{DD} and V_{EE} establish the input and output voltage range which is:

$$V_{EE} \leq \text{Input, outputs} \leq V_{DD} - 2V$$

V_{DD} and V_{SS} (V_{SS} is usually ground) determine the control input logic levels and switch points (see Table 1 below).

V_{DD}	V_{SS}	V_{EE}	V_{IH}	V_{IL}
5	0	−5	2.4	.8
5	0	−10	2.4	.8
3	0	−12	2	.8
7.5	0	−7.5	3	.8
15	0	0	6	.8
12	0	0	5	.8

TABLE 1 — CONTROL INPUT SWITCH POINTS

The total supply range is 7 to 15 volts nominal and 5 to 18 volts absolute maximum, however, several specifications including acquisition time, offset, and output voltage compliance will degrade for a total supply less than 7 volts.

The supply current, I_{DD}, is typically 4mA with the outputs unloaded.

SIGNAL INPUT (pin 3)

The signal input should be driven by a low impedance voltage source such as the output of an operational amplifier. The op amp should have a high slew rate and fast settling time if one needs to make use of the 2300's fast acquisition characteristics. As with all CMOS devices, all input excursions should be confined to the supply rails, i.e., $V_{EE} \leq$ inputs $\leq V_{DD}$, to avoid latch up (note, for latch up considerations, V_{SS} counts as an input).

To achieve this, split supplies such as ±7.5 volts can be used for the 2300 and the op amp. If single supply operation is desired, an op amp such as the LM324, 3403, or a CMOS op amp operating from V_{DD} that is designed for single supplies and whose input and output voltage compliances include ground, can be used to drive pin 3.

However, since the output of a DAC current to voltage convertor is positive going from ground, it is possible to use the circuit of Figure 1 to drive pin 3 and to power the op amp from split supplies with the 2300 and the op amp using the same positive supply. The clamp diode and the output resistor limit voltage and current during any negative turn-on transient. A small capacitor in feedback is required in order to prevent a large false hold step due to the op amp's high frequency output impedance.

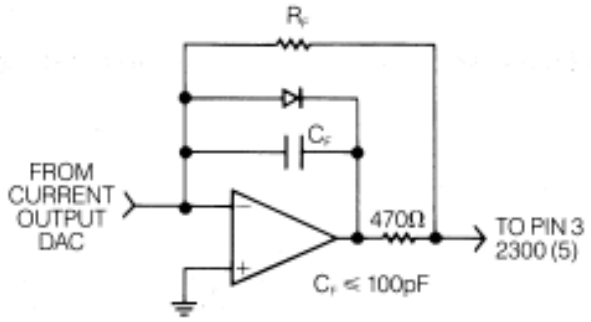


FIGURE 1 — DAC INTERFACE CIRCUIT (2300 SINGLE SUPPLY, OP AMP DRIVER SPLIT SUPPLY)

LOGIC INPUTS (Pins 6, 9, 10, and 11)

The threshold levels of the 2300 logic inputs have been intentionally shifted toward V_{SS} so that they can be driven by TTL as well as CMOS logic over most of the supply range (see Table 1). However, for $7.5V < V_{DD} < +12V$, pull up resistors to the 5 volt supply should be used on the TTL outputs. TTL drivers should not be used if V_{DD} is greater than 12 volts.

Table 2 shows the channel decoding for the SSM 2300 which is identical to that of the 4051. When there is an address change, it is possible for two or more channels to be connected to the input at the same time. In order to avoid crosstalk problems resulting from this, either the input signal should be kept at its previous level for 500nS after the address change (Figure 2A) or preferably 'INH' (pin 6) should be exercised as in Figure 2B.

Pin	9	10	11	6		
	C	B	A	INH	CH	Pin
	0	0	0	0	0	13
	0	0	1	0	1	14
	0	1	0	0	2	15
	0	1	1	0	3	12
	1	0	0	0	4	1
	1	0	1	0	5	5
	1	1	0	0	6	2
	1	1	1	0	7	4
	X	X	X	1	NONE	—

TABLE 2 — CHANNEL DECODING

OUTPUT BUFFERS (Pins 1, 2, 4, 5, 12, 13, 14, and 15)

The preliminary buffer offset specification is ±30mV. This is less than 1 LSB of an 8 bit DAC with the DAC and the 2300 operating with a 10V output compliance. The change in offset over the output range is typically 3mV. The hold step, the voltage shift when a channel is deselected, is about 4mV typical with very little variability. The droop rate of a held channel is ±50mV/second typical and ±150mV/second worst case (input and output(s) at opposite extremes of the voltage compliance range).

The buffers were designed primarily to drive loads connected to ground. The outputs can source more than 1.2mA each over the full output voltage range but have limited sink capability near V_{EE}. This is not a problem for split supply operation because the input and output voltage compliances can be restricted to 2V from either supply to give a symmetrical output swing. The output impedance with the output sourcing current is about 0.1 ohm. With the output sinking current, the impedance is about 1 ohm.

The outputs are stable with any capacitive load less than 500pF. Many FET input op amps used in sample and hold applications like the TL082 or LM353 become unstable with an output capacitive load as small as 30pF. This is particularly true when connected as unity gain buffers. Printed circuit board traces of moderate length can cause stability problems for these parts.

The buffer outputs are not short circuit protected. Care should be taken to avoid shorting any of the outputs to the supplies or ground.

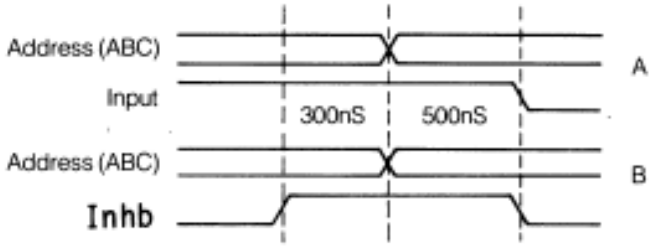
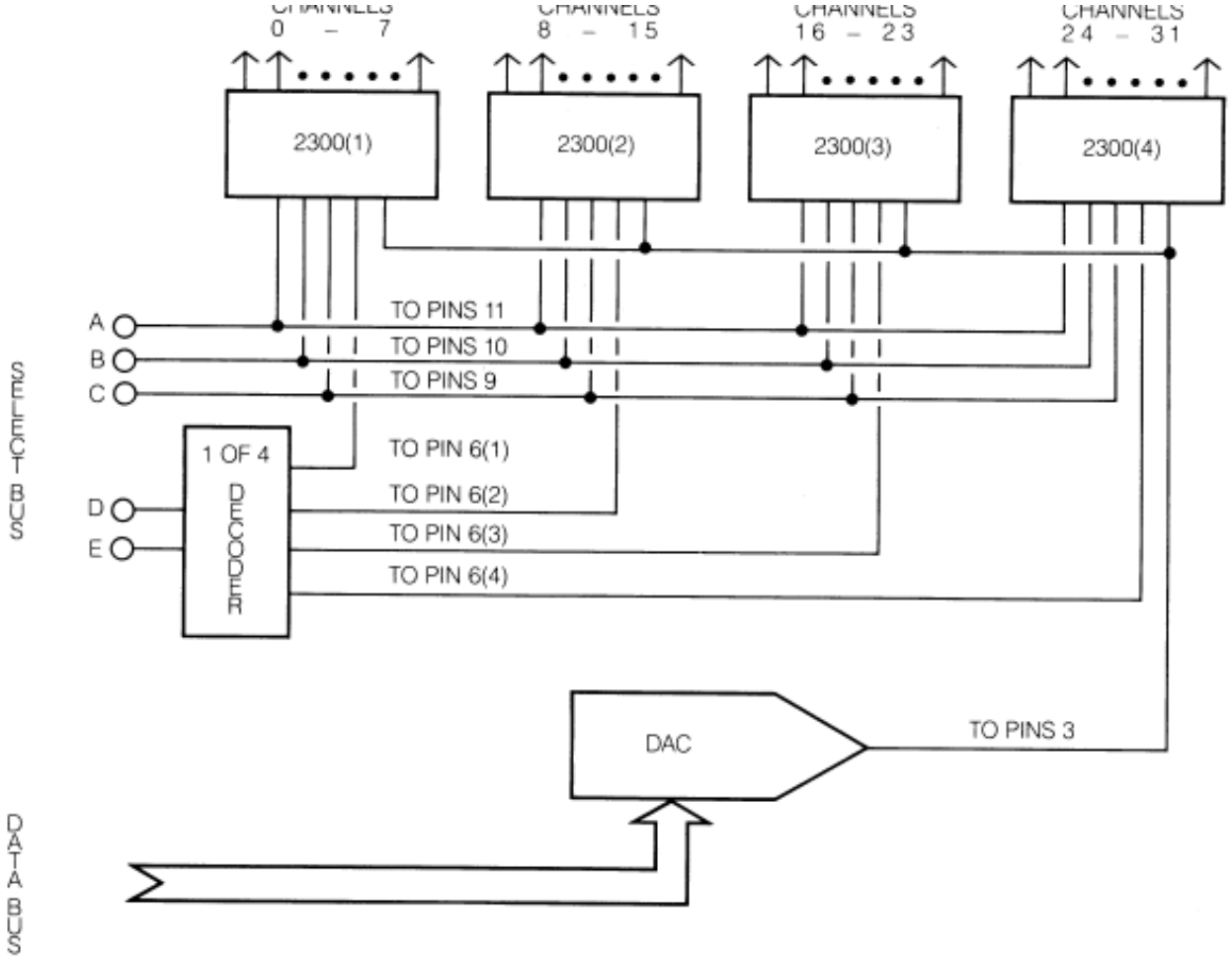


FIGURE 2 — DECODE TIMING



TYPICAL APPLICATION (1 TO 32 ANALOG DEMULTIPLEXER)

APPLICATIONS

Near D.C., almost any number of 2300's can be connected in parallel for process control applications allowing a single DAC to service many control channels simultaneously (see Typical Application Schematic). The 2μS acquisition time, the number of channels, and the address timing determines the maximum update rate. Eight channels of full band audio can be demultiplexed with a DAC and the 2300.