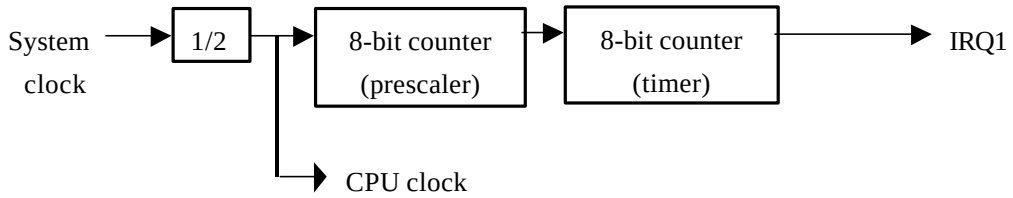
STK55C1042 Specification

1. CHIP FEATURES :

* Operating voltage : 2.5V-6.5V
* Operating current : under 5mA at 5V.
* Dual frequency
  - 32.768 KHz for LCD & 0.5 second timer interrupt.
  - Crystal or RC oscillator for system clock.
  - CPU clock is half of system clock.
* Built-in 2K bytes RAM, (1st 144 bytes for LCD, the rest 1904 bytes for program & stack).
* Built-in 32K bytes ROM with 16K per bank.
* Two chip enable signals for external memory. Each one can be expanded to 512K bytes with 16K bytes per bank.
* One 0.5 second pre-divider timer interrupt with start/stop control.
* 2 output ports for key matrices
  - 14 pins for port 1, also used as address pins.
  - 4 input pins with wake-up interrupt for port 2.
  - Built-in pull-up resistors for port 2.
* 8-bit timer with 8-bit prescale counter, both are auto-reloadable.



* 65 segments and 16 commons output pins for LCD driver.
  - 1/5 bias, 1/16 duty and 64 Hz frame frequency.
* Selectable 64 Hz Interrupt by NMI.
* Timers and port 2 enable IRQ Interrupt.
* Timer range is programmable.
* 8-bit sound generator with 8-bit prescaler, both are auto-reloadable.
* One output for the speaker.
  - 2 KHz or 4 KHz signal with two different envelopes are selectable for sound output.
* One UART serial port with even parity check bit added after MSB for error detecting.
* The internal ROM can be disabled and the corresponding memory area are mapped to the highest banks of external ROM.

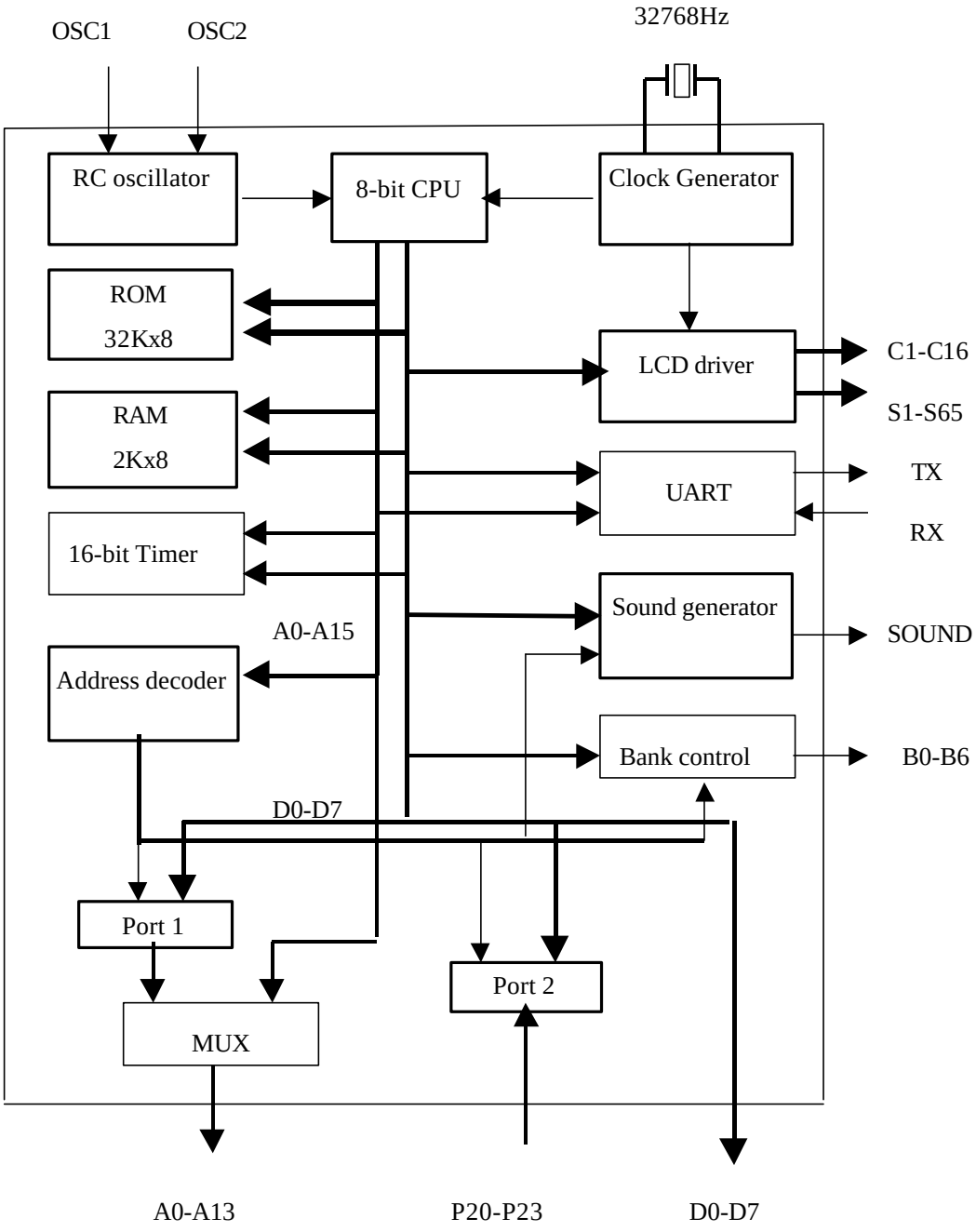
* Sleep mode : LCD off , crystal & system oscillator stop, Vdd=3V, Idd < 1 uA.

Stand-by mode : LCD on and system oscillator stop, Vdd=3V, Idd < 80 uA. LCD off and system oscillator stop, Vdd=3V, Idd < 8 uA.

2. APPLICATION:

- Data Bank
- Translator
- Organizer
- Hand-held game

3. BLOCK DIAGRAM:



4. PIN DESCRIPTION : (Total 131 pads)

Pin name	I/O	Description
COM1-COM16	O	Output pins for driving the commons of LCD panel
SEG1-SEG65	O	Output pins for driving the segments of LCD panel
SOUND	O	Output pin for speaker
A0-A13	O	Address bus outputs share with port 1 output
L0-L3	IU	4 input pins for key matrix with wake-up interrupt
D0-D7	I/O	Data pins
OSC1	I	RC/Crystal Oscillator input pin for system clock
OSC2	O	RC/Crystal Oscillator output pin for system clock (Note: CPU clock = system clock/2)
OSC3	I/O	RC Oscillator bi-directional pin for system clock
/RES	IU	Chip reset
VDD	I	Power input
VSS	I	Signal ground
LOSC1	I	Crystal oscillator input pin
LOSC2	O	Crystal oscillator output pin
BANK0-BANK4	O	To select external memory banks. The data on $1209 will be output in these pins except during /CE2 read/write cycle. At that time these pins will output the data on $120A
/CE1	O	External chip Enable 1. This pin will be forced to high during sleep mode.
/CE2	O	External chip enable 2. This pin will be forced to high during sleep mode.
/TEST	IU	Test pin. Keep floating or connect to VDD
RWB	O	Read/Write signal output
VLCD	I	Power supply for LCD driver
VR	I	Contrast control for LCD
CLKOUT	O	512 Hz output clock for voltage doubler. This clock will be stopped if 32.768K Hz crystal is stopped
/DIROM	IU	Internal ROM control pin. =0 Disable internal ROM =1 Enable internal ROM
TX	O	Transmit data pin
RX	IU	Receive data pin

Note : IU -- Input pin with pull-up resistor.

5. ADDRESS ARRANGEMENT :

1) RAM

0000-008F : for LCD output data storage.

	SEG1-SEG8	SEG9-SEG16	• • •	SEG57-SEG64	SEG65
COM1	0000	0010	• • •	0070	0080
COM2	0001	0011	• • •	0071	0081
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
COM16	000F	001F	• • •	007F	008F

* The LSB of low byte - SEG1

The LSB of high byte - SEG65

Middle bits are in order.

0090-00FF : for zero page area

0100-01FF : for stack area

0200-07FF : for data area.

4000-7FFF : for external chip enable 1. While this area is accessed, /CE1 will be low and the data in $1209 will be output on BANK0-BANK4. If bit 0 of $121A is set to one, then this area can not be accessed.

2) ROM

8000-BFFF : for external chip 2 or internal ROM banks.

/DIROM	$121A Bit 1	$121A Bit 0	Function description
X	0	0	This area is external memory. /CE2 will be low and the data in $120A will output to BANK0-BANK4.
X	0	1	This condition is prohibited.
0	1	0	This area is external memory. /CE2 will be low and the value of $1209 will be sent to BANK0-4.
0	1	1	This condition is prohibited.
1	1	X	This area is internal ROM. /CE2 will keep high. $1209 defines the bank number of internal ROM. The internal ROM are located at bank 1EH-1FH. Bank 00H is used to define the volume of sound output.

C000-FFFF : for program memory

/DIROM	Bit 0 of $121A	Function description
0	0	This area is external memory. /CE2 will be low and BANK4-BANK0=1FH.
0	1	This condition is prohibited.
1	X	The internal ROM bank 1FH is selected. /CE2 will be high.

FFFF,FFFE - IRQ vector

FFFD,FFFC - RES vector

FFFB,FFFA - NMI vector

3) Others

1200 To enter stand-by mode; write only.

* In standby mode, the system oscillator will be stopped. But 32768Hz crystal will still work.
* The CPU, UART and timer will be stopped.
* LCD state is depended on bit 1 of $120D.
* NMI and IRQ3 are still functionally.
* When in stand-by mode, NMI, IRQ2 or IRQ3 will wake up the CPU.

1201 To enter sleep mode; write only.

Bit 1 : = 0 Disable sleep mode

= 1 Enable sleep mode

In sleep mode, whole chip will be stopped. That is, the system and 32768 Hz crystal oscillator will be stopped. The bit 1 of $120D will be reset. Only reset and IRQ2 will wake up this chip.

1202 Sound output control

Bit 0 : = 0 For 1 KHz base frequency

= 1 For 2 KHz base frequency

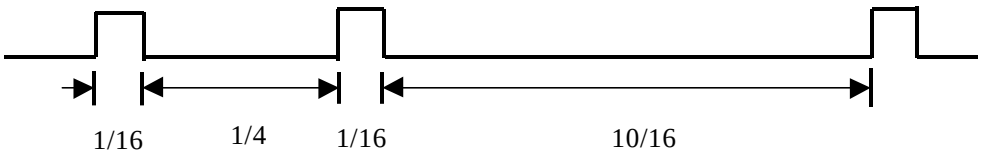
2-1 : = 0x Sound off

= 10 For alarm envelope

= 11 Sound always on

* The default value for each bit is zero.

Alarm envelope waveform: (unit = second)



1203 IRQ flag register; read & write.

* Read : Bit 0 : if 1, timer interrupt, IRQ1.

Bit 1 : if 1, port 2 interrupt, IRQ2.

Bit 2 : if 1, 0.5 sec. timer interrupt, IRQ3.

Bit 3 : if 1, transmit data complete interrupt, IRQ4.

Bit 4 : if 1, receiver data ready interrupt, IRQ5.

* Write : Bit 0 : if 0, clear the flag of IRQ1.

Bit 1 : if 0, clear the flag of IRQ2.

Bit 2 : if 0, clear the flag of IRQ3.

Bit 3 : if 0, clear the flag of IRQ4.

Bit 4 : if 0, clear the flag of IRQ5.

* When the system is in IRQ mode, the IRQ flag register must be cleared before having another interrupt request; otherwise, the system will always be in IRQ mode.

1204 Low byte data for port 1; write only.

The output data pins are shared with A0-A7.

1205 High byte data for port 1; write only.

Bit 5-0 : Output data. The output data pins are shared with A8-A13.

1206 Write: load prescaler value and timer value from buffer to counter

Read : read current counter value

* After $1206 been written, timer will begin to count down. And IRQ1 happens when timer counts to zero.

elapsed time = $120B*($120C+1)/(system clock/2).

1207 Port 2 data; read only

Bit 3-0 : Input data. One wait state will be added while reading this port.

1208 Set port 2 bit interrupt function; write only.

* An '0' in this register will set the interrupt function of the corresponding pin of port 2 to be enabled.
* The port 2 interrupt is enabled only during sleep or standby mode.
* The default value for each bit is one.

1209 For selecting the memory bank of external chip 1 or internal ROM; write only

Bit 4-0 : set bank number of external chip 1.

120A For selecting the memory bank of external chip 2; write only

Bit 4-0 : set bank number of external chip 2.

120B Write initial timer prescaler value to buffer; write only

120C Write initial timer value to buffer; write only

120D Control register; write only

Bit 0 : = 0 Disable 64 Hz NMI
= 1 Enable 64 Hz NMI (NMI frequency = 64Hz)
1 : = 0 LCD off
= 1 LCD on
2 : = 0 Disable timer
= 1 Enable timer
3 : = 0 Disable IRQ1
= 1 Enable IRQ1

The default value is zero.

120E 0.5 sec timer interrupt; write only

Bit 0 : = 0 Stop 0.5 second timer and reset it

= 1 Start 0.5 second timer

When 0.5 second is elapsed, IRQ3 will occur.

120F Select oscillator warm-up time.

Bit 0 : = 0 warm-up time is 4 system clocks, for RC oscillator

= 1 warm-up time is 31.25ms, for crystal oscillator

1214 Load baud rate counter value to buffer; write only.

Baud rate = (system clock)/16/([$1214]+1)

Example: For system clock = 2MHz

Baud rate	Counter Value (Dec)	Actual Baud rate	Error (%)
1200	103	1201.92	0.16
2400	51	2403.85	0.16
3600	34	3571.43	-0.79
4800	25	4807.69	0.16
7200	16	7352.94	2.12
9600	12	9615.38	0.16

1215 Load baud rate counter value from buffer to counter to generate desired baud rate; write only.

1216 Read : read the received data from buffer

Write: load data to buffer for transmission

1217 UART status register; read only.

Bit 0 : = 0 Received data no error

= 1 Received data parity error

1 : = 0 Transmit buffer not ready

= 1 Transmit buffer empty

1218 Write initial prescaler value to sound generator; write only

1219 Write initial value to sound generator; write only

* Output frequency = system clock/[($1219)+1]/[($1218)+1]/4

121A Control register. Write only.

Bit 0 : = 0 Enable external memory expansion. $8000-$BFFF are external memory. A0-A13 are shared with port 1. D0-D7 are data bus.

= 1 Disable external memory expansion. $8000-$BFFF are internal ROM. A0-A13 are output port 1 and D0-D7 are data bus.

1 : = 0 $8000-$BFFF are external memory bank.

= 1 $8000-$BFFF are internal ROM bank.

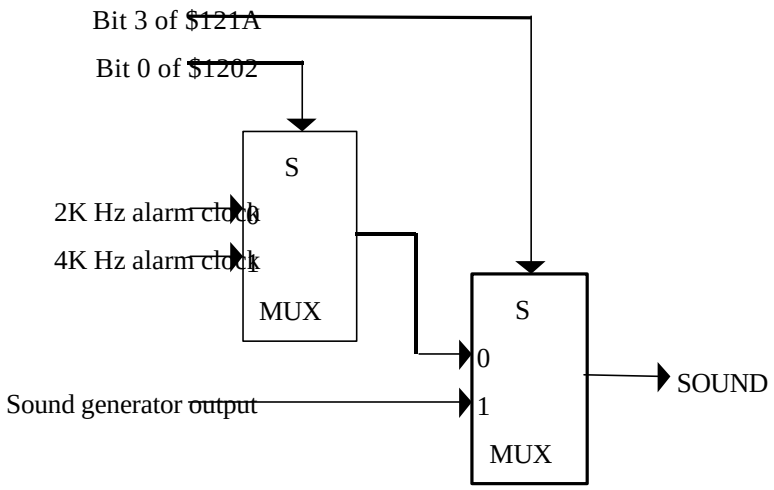
3 : = 0 Select alarm clock output.

= 1 Select sound generator output.

4 : = 0 Disable sound generator.

= 1 Enable sound generator.

The default value is zero.



4) The reset status of CPU

If the /RES is keep low more than two system clocks, then the CPU will be reset. After reset, the interrupt mask flag is set, the decimal mode is cleared and the program counter will be loaded with the reset vector from address $FFFC and $FFFD. So, **after initial procedure the firmware should do a 'CLI' instruction**. Otherwise, the CPU will not acknowledge any interrupt.

5) Interrupts

* There are six interrupt sources :

NMI - 64 Hz interrupt

IRQ1 - Timer interrupt

IRQ2 - Sleep and Stand-by interrupts by port 2

IRQ3 - 0.5 second timer interrupt

IRQ4 - Transmit buffer ready interrupt

IRQ5 - Receiver data ready interrupt

* Only IRQ2 will wake up CPU from sleep mode.
* Only IRQ2, IRQ3 and NMI can wake up CPU from stand-by mode.
* An oscillator warm-up time (4 cycles or 31.25ms) will be added before CPU been waken up from standby or sleep mode.
* After CPU wake up from sleep mode, programmer should turn on LCD again.
* 0.5 sec. timer interrupt, with start/stop control, is operated by writing $120E.
* In the IRQ routine, the program decides from port $1203 to check which Interrupt has happened.
* When port 2 interrupt is enabled, a low signal from any pin will generate IRQ2.
* Before starting timer, load new prescale value (by writing $120B) or new timer value (by writing $120C) to buffer for having different IRQ time ranges. Otherwise, write $1206 to have the same IRQ time range as the previous one's.
* When the CPU acknowledge the interrupt, following things will be done:
  a) The interrupt mask flag will be set by CPU
  b) The return address and status register will be pushed to stack.
* When the CPU return from interrupt routine by RTI instruction following things will be done:
  a) The return address and status register will be pulled from stack.
  b) The interrupt mask flag will be cleared.
* I**t is not necessary to add SEI and CLI instructions in interrupt routine**. If a CLI instruction is added in the interrupt routine, then another interrupt may be inserted during current interrupt routine and may cause stack overflow.

6) Serial port

* Load baud rate counter value (by writing $1214) to buffer then load it from buffer to counter(by writing $1215) to generate desired baud rate.
* Write $1216 to transmit data, one byte at a time. When one data byte has been transmitted, hardware generates IRQ4 interrupt (transmit buffer ready).
* When one data byte is received, hardware generates IRQ5 interrupt (receiver data ready). Read $1216 to fetch data from buffer.
* Read $1217 bit 0 to check if data received is correct and read bit 1 to check when next data byte can be transmitted.
* When system is in stand-by mode, serial port is disabled.

7) Internal ROM.

The internal 32K bytes ROM are split to 2 banks. The bank number is defined by $1209 and the internal ROM are located at bank 1EH to 1FH. CPU address 0C000H-0F000H is accessed the bank 1FH. The others should be accessed by set $1209 to the bank number and set bit 1 of $121A to one, then read from 8000H-0BFFFH.

8) Sound volume.

To change the volume, please follow the procedures listed below :

a) Write zero to $1209.

b) Set bit 1 of $121A to one.

c) Set 0 to bit 0 of $8001 to enable the melody output.

d) Write the volume value to $8000 (bit 0 is do not care).

The default value of volume is $FF.

9) Speech output.

To enable the speech function, please follow the procedures listed below :

a) Write zero to $1209.

b) Set bit 1 of $121A to one.

c) Set 1 to bit 0 of $8001 to disable the melody output and have the DAC always on.

d) Change the volume data in $8000 according to the speech data (bit 0 is do not care).

e) Repeat a), b) and d) to change the speech data.

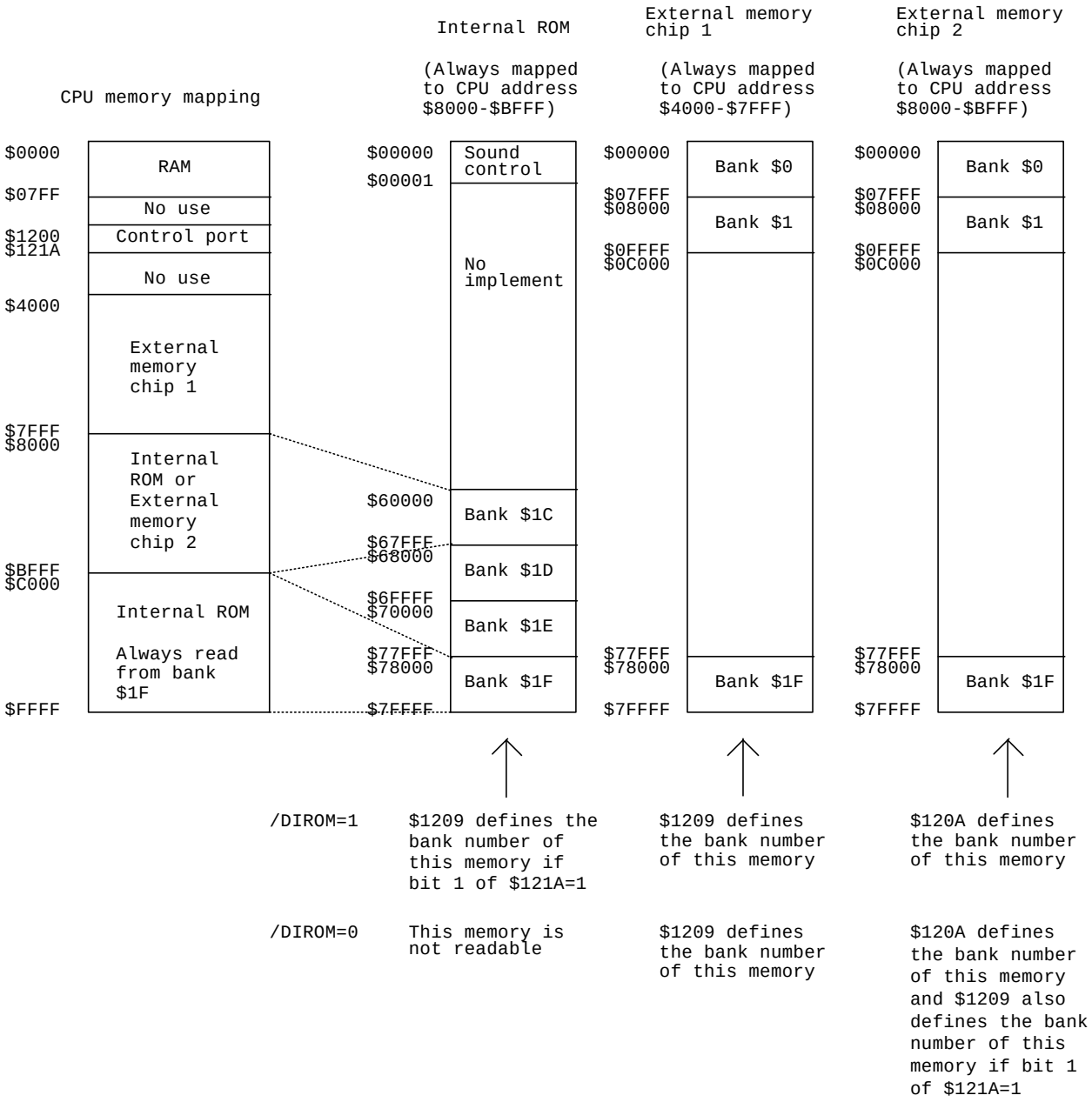
f) After the speech data is finished, repeat procedure a) and b) and then write set 0 to bit 0 of $8001.

g) Due to the value of $1209 will be changed during speech output, the speech output program should be located on the $C000-$FFFF area.

(Note : If there is no speech or melody output, then either the bit 0 of $8001 or $8000 should be kept at zero. Otherwise, a DC current may flow through the external speaker drive circuit.)

10) Summary for accessing each bank of memory:

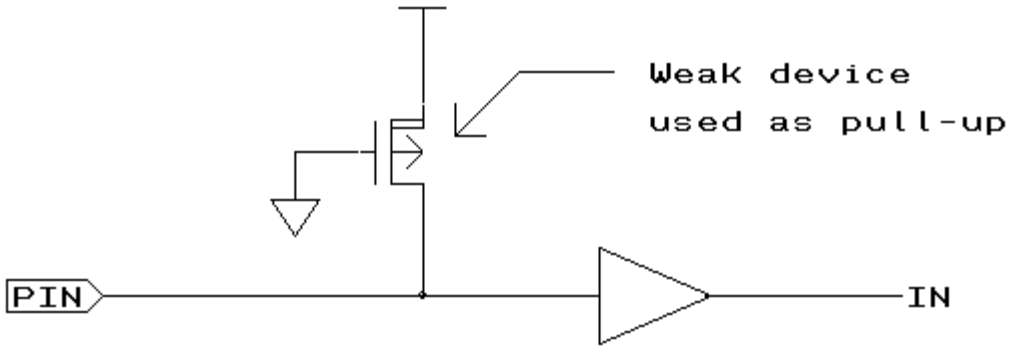
/DIROM	Bit 1 of $121A	Bit 0 of $121A	Remarks
0	0	0	$4000 - $7FFF: CE1, bank = ($1209) $8000 - $BFFF: CE2, bank = ($120A) $C000 - $FFFF: CE2, bank = $1F
0	0	1	Prohibited
0	1	0	$4000 - $7FFF: CE1, bank = ($1209) $8000 - $BFFF: CE2, bank = ($1209) $C000 - $FFFF: CE2, bank = $1F
0	1	1	Prohibited
1	0	0	$4000 - $7FFF: CE1, bank = ($1209) $8000 - $BFFF: CE2, bank = ($120A) $C000 - $FFFF: internal, bank = $1F
1	0	1	Prohibited
1	1	0	$4000 - $7FFF: CE1, bank = ($1209) $8000- $BFFF: internal, bank = ($1209) $C000 - $FFFF: internal, bank = $1F
1	1	1	$4000 - $7FFF: CE1 not accessible $8000 - $BFFF: internal, bank = ($1209) $C000 - $FFFF: internal, bank = $1F



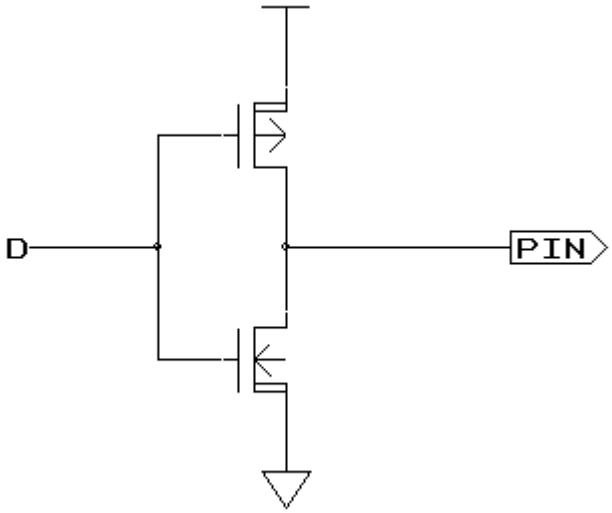
11) The sound volume or voice level can only be set at internal $C000-$FFFF bank or external $C000-$FFFF bank. (Unable to set at $8000- $BFFF bank , whether it is internal ROM program or external ROM program, also unable to set at $4000-$7FFF bank).

6. I/O STRUCTURE :

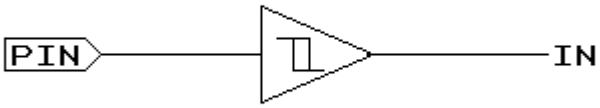
6.1 For L0-L3 :



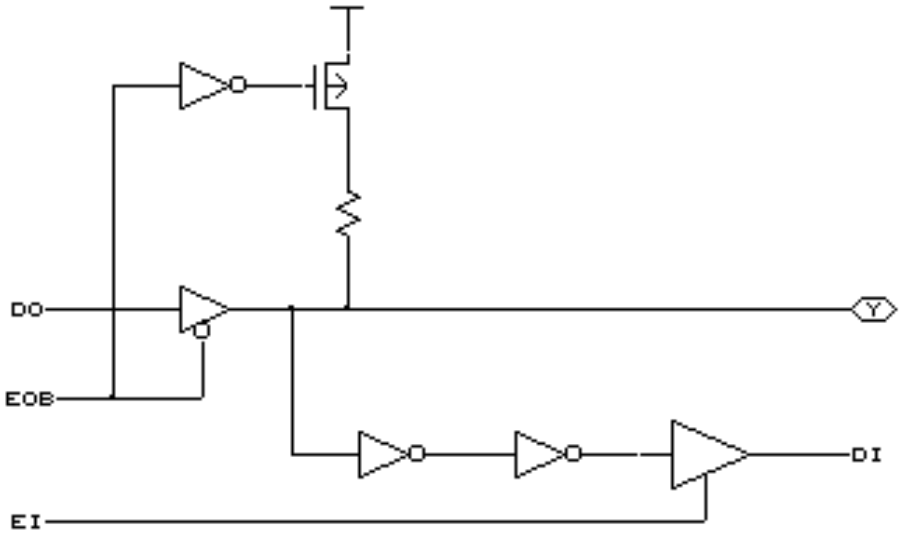
6.2 For output pins :



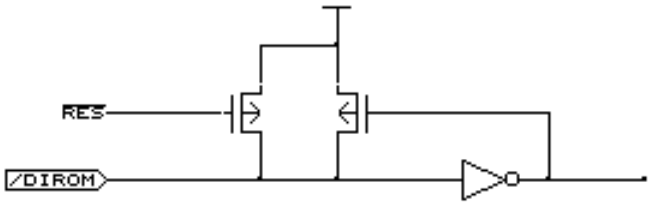
6.3 /RES pin :



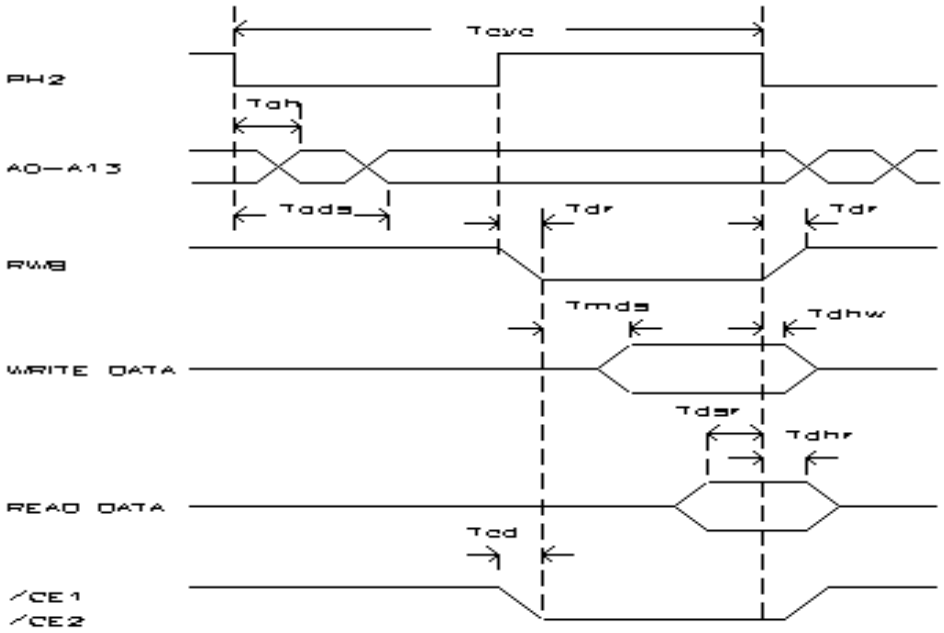
6.4 For I/O pins :



6.5 /DIROM pin :



7. TIMING DIAGRAM FOR EXTERNAL MEMORY ACCESS :



Description	Symbol	Min.	Typ.	Max.	Unit
Cycle Time	Tcyc		1		µS
Address hold time	Tah	10			nS
Delay time	Tdr			10	nS
Write data delay time	Tmds			100	nS
Write data hold time	Tdhw	10			nS

8. ABSOLUTE MAXIMUM RATINGS :

Operating temperature ..... 0 to 70℃

Storage temperature ..... -65 to 150℃

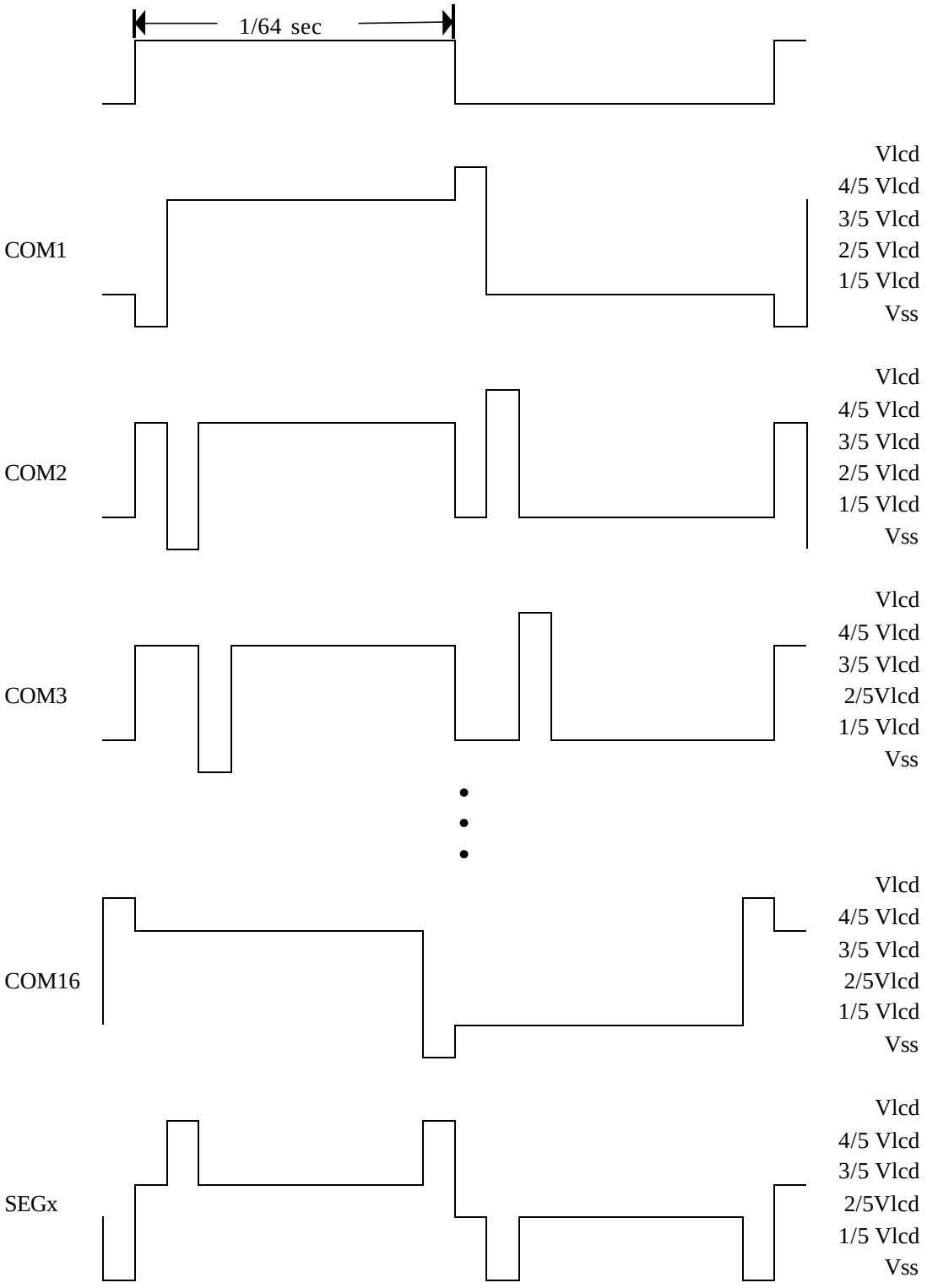
Supply voltage ..... 7 V

Input voltage ..... -0.6 to Vdd+0.6 V

9. ELECTRICAL CHARACTERISTIC :

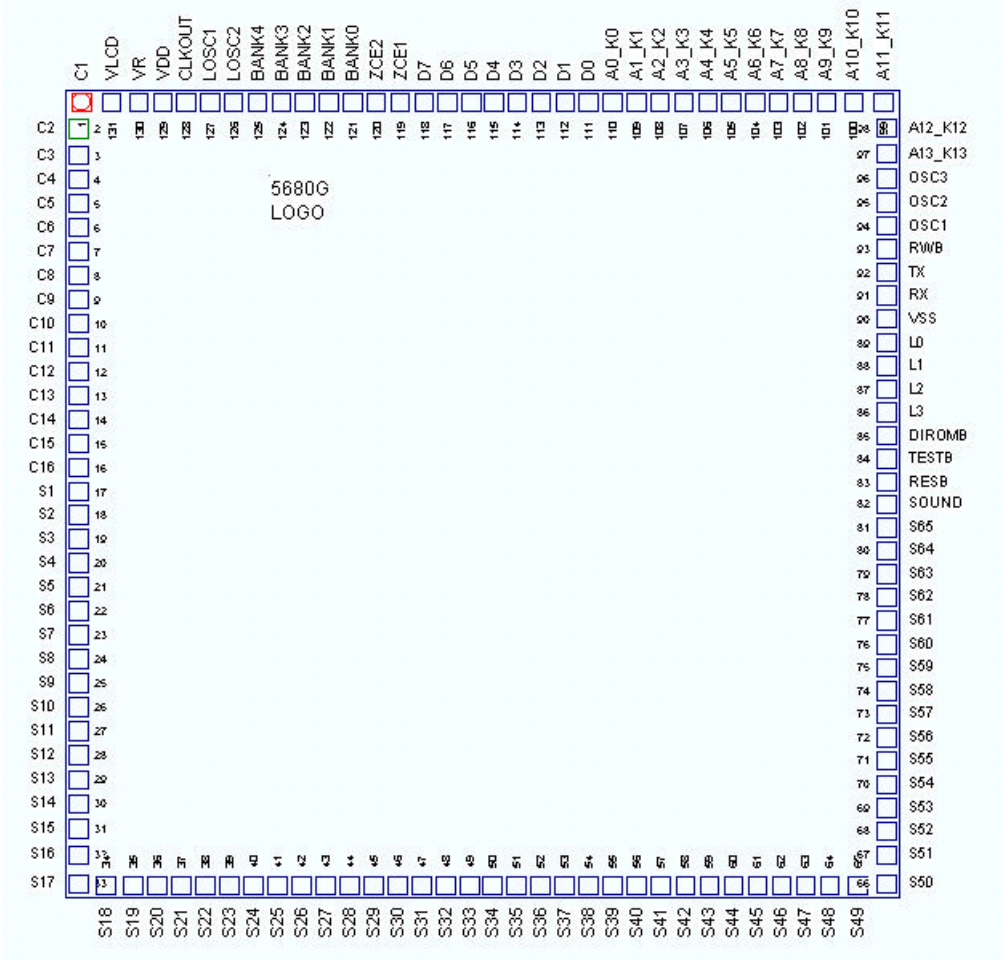
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	Vdd		2.5	3.0	6.5	V
Main system frequency	∅sys	Vdd=3V		2	5	Mhz
		Vdd=4.5V			7	Mhz
Crystal frequency	∅cry			32768		Hz
Operating current	Idd	Vdd=5V, ∅sys=1Mhz		2		mA
Standby current (LCD on)	Istdby	Vdd=2.5V,Vlcd=4V		56		µA
		Vdd=3V,Vlcd=5V		88		µA
		Vdd=3.5V,Vlcd=6V		124		µA
		Vdd=Vlcd=4V		55		µA
		Vdd=Vlcd=4.5V		67		µA
		Vdd=Vlcd=5V		93		µA
		Vdd=Vlcd=5.5V		110		µA
Standby current (LCD off)		Vdd=2.5V		2		µA
		Vdd=3V		2.8		µA
		Vdd=3.5V		3.8		µA
		Vdd=4V		5		µA
		Vdd=4.5V		6.5		µA
		Vdd=5V		8.1		µA
		Vdd=5.5V		10.5		µA
Input high voltage	Vih	Vdd=5.0V	2.0			V
Input low voltage	Vil	Vdd=5.0V	-0.6		0.8	V
Input high leakage current	Iih	Vih=Vdd			-1	µA
Input low leakage current	Iil	Vil=0			1	µA
Output high voltage (For SEGx and COMx)	Voh1	Ioh=-30µA	Vlcd-0.2		Vlcd	V
Output low voltage (for SEGx and COMx)	Vol1	Iol=40µA	0		0.2	V
Output high voltage (for other pins)	Voh2	Ioh=-4mA	Vdd-0.8		Vdd	V
Output low voltage (for other pins)	Vol2	Iol=4mA	0		0.8	V

10. LCD WAVEFORM :



There are two LCD matrix DOTs active at (SEGx,COM2) and (SEGx,COM16)

11. PAD LOCATION :



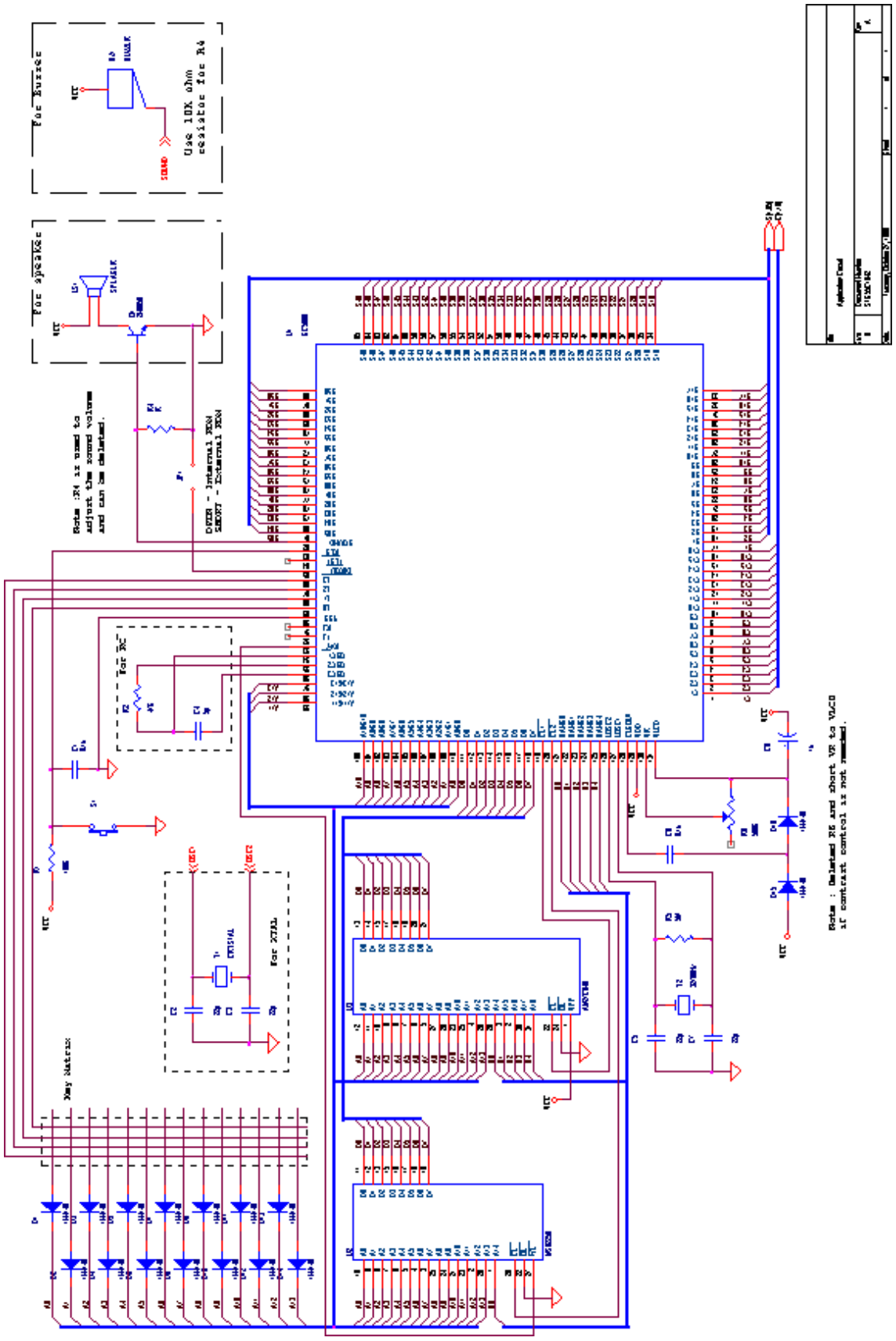
Chip size : 4180 x 4060 Unit : μM

PAD-No	Name	X	Y	PAD-No	Name	X	Y
1	C1	77.90	3995.70	67	S51	4117.10	217.20
2	C2	62.90	3863.60	68	S52	4117.10	337.20
3	C3	62.90	3733.40	69	S53	4117.10	454.20
4	C4	62.90	3612.70	70	S54	4117.10	571.20
5	C5	62.90	3492.00	71	S55	4117.10	688.20
6	C6	62.90	3371.30	72	S56	4117.10	805.20
7	C7	62.90	3250.60	73	S57	4117.10	922.20
8	C8	62.90	3129.90	74	S58	4117.10	1039.20
9	C9	62.90	3009.20	75	S59	4117.10	1156.20
10	C10	62.90	2888.50	76	S60	4117.10	1273.20
11	C11	62.90	2767.80	77	S61	4117.10	1390.20

PAD-No	Name	X	Y	PAD-No	Name	X	Y
12	C12	62.90	2647.10	78	S62	4117.10	1507.20
13	C13	62.90	2526.40	79	S63	4117.10	1624.20
14	C14	62.90	2405.70	80	S64	4117.10	1741.20
15	C15	62.90	2285.00	81	S65	4117.10	1858.20
16	C16	62.90	2164.30	82	SOUND	4117.10	1975.20
17	S1	62.90	2043.60	83	RESB	4117.10	2092.20
18	S2	62.90	1922.90	84	TESTB	4117.10	2209.20
19	S3	62.90	1802.20	85	DIROMB	4117.10	2326.20
20	S4	62.90	1681.50	86	L3	4117.10	2443.20
21	S5	62.90	1560.80	87	L2	4117.10	2560.20
22	S6	62.90	1440.10	88	L1	4117.10	2677.20
23	S7	62.90	1319.40	89	L0	4117.10	2794.20
24	S8	62.90	1198.70	90	VSS	4117.10	2911.20
25	S9	62.90	1078.00	91	RX	4117.10	3028.20
26	S10	62.90	957.30	92	TX	4117.10	3145.20
27	S11	62.90	836.60	93	RWB	4117.10	3262.20
28	S12	62.90	715.90	94	OSC1	4117.10	3379.20
29	S13	62.90	595.20	95	OSC2	4117.10	3496.20
30	S14	62.90	474.50	96	OSC3	4117.10	3616.30
31	S15	62.90	348.40	97	A13_K13	4117.10	3741.30
32	S16	62.90	217.20	98	A12_K12	4117.10	3866.30
33	S17	62.90	72.20	99	A11_K11	4102.10	3995.70
34	S18	198.80	64.20	100	A10_K10	3952.10	3995.70
35	S19	335.70	64.20	101	A9_K9	3814.80	3995.70
36	S20	456.20	64.20	102	A8_K8	3695.80	3995.70
37	S21	576.70	64.20	103	A7_K7	3576.80	3995.70
38	S22	697.20	64.20	104	A6_K6	3457.80	3995.70
39	S23	817.70	64.20	105	A5_K5	3338.80	3995.70
40	S24	938.20	64.20	106	A4_K4	3219.80	3995.70
41	S25	1058.70	64.20	107	A3_K3	3100.80	3995.70
42	S26	1179.20	64.20	108	A2_K2	2981.80	3995.70
43	S27	1299.70	64.20	109	A1_K1	2862.80	3995.70
44	S28	1420.20	64.20	110	A0_K0	2743.80	3995.70
45	S29	1540.70	64.20	111	D0	2624.80	3995.70

PAD-No	Name	X	Y	PAD-No	Name	X	Y
46	S30	1661.20	64.20	112	D1	2505.80	3995.70
47	S31	1781.70	64.20	113	D2	2386.80	3995.70
48	S32	1902.20	64.20	114	D3	2267.80	3995.70
49	S33	2022.70	64.20	115	D4	2148.80	3995.70
50	S34	2143.20	64.20	116	D5	2029.80	3995.70
51	S35	2263.70	64.20	117	D6	1910.80	3995.70
52	S36	2384.20	64.20	118	D7	1791.80	3995.70
53	S37	2504.70	64.20	119	ZCE1	1672.80	3995.70
54	S38	2625.20	64.20	120	ZCE2	1553.80	3995.70
55	S39	2745.70	64.20	121	BANK0	1434.80	3995.70
56	S40	2866.20	64.20	122	BANK1	1315.80	3995.70
57	S41	2986.70	64.20	123	BANK2	1196.80	3995.70
58	S42	3107.20	64.20	124	BANK3	1077.80	3995.70
59	S43	3227.70	64.20	125	BANK4	958.80	3995.70
60	S44	3348.20	64.20	126	LOSC2	839.80	3995.70
61	S45	3468.70	64.20	127	LOSC1	720.80	3995.70
62	S46	3589.20	64.20	128	CLKOUT	601.80	3995.70
63	S47	3709.70	64.20	129	VDD	482.80	3995.70
64	S48	3830.20	64.20	130	VR	363.80	3995.70
65	S49	3970.50	64.20	131	VLCD	227.90	3995.70
66	S50	4117.10	72.20				

12. APPLICATION CIRCUIT :



Syntek Semiconductor Co., Ltd.

Customer Information Sheet for STK55C1042 971014

1. Customer's Name : _____

2. Project title : _____

3. Syntek part number : _____ (will be filled by Syntek.)

4. Package ---------- ( ) Chip ( ) QFP

5. Options :

   Oscillator type ---------- ( ) RC ( ) XTAL

   Operating mode --------- ( ) STK55C1042 ( ) STK55C1041

6. Customer code :

   Code form ---------- ( ) EPROM ( ) file _____

   Checksum ---------- 8000-9FFF _____H

   A000-BFFF _____H

   C000-DFFF _____H

   E000-FFFF _____H

   8000-FFFF _____H

7. Operating conditions :

   All the operating conditions listed below are for Syntek reference. Syntek will not guaranty on these values. Please refer to data book or contact Syntek for the guaranty values.

   Operating voltage : _____-_____ V Voltage doubler : ( ) Yes ( ) No

   Operating current : _____ mA Operating frequency : _____ Hz

   Stand-by current : _____ μA (LCD On) _____ μA (LCD Off)

   Sleep current : : _____ μA (LCD Off)

   Others :

Customer : _____ Salesman : _____Date : __/__/__