SGS-THOMSON MICROELECTRONICS

ISB35000 SERIES

HCMOS STRUCTURED ARRAY

PRELIMINARY DATA

FEATURES

- 0.5 micron triple layer metal HCMOS process featuring retrograde well technology, low resistance salicided active areas, polysilicide gates and thin metal oxide.
- 3.3 V optimized transistor with 5 V I/O interface capability
- 2 - input NAND delay of 0.210 ns (typ) with fanout = 2.
- Broad I/O functionality including LVCMOS, LVTTL, GTL, PECL, and LVDS.
- High drive I/O; capability of sinking up to 48 mA with slew rate control, current spike suppression and impedance matching.
- Metallised generators to support SPRAM and DPRAM, plus an extensive embedded function library.
- Combines Standard Cell Features with Sea of Gates time to market.
- Fully independent power and ground configurations for inputs, core and outputs.
- Programmable I/O ring capability up to 1000 pads.
- Output buffers capable of driving ISA, EISA, PCI, MCA, and SCSI interface levels.
- Active pull up and pull down devices.
- Buskeeper I/O functions.
- Oscillators for wide frequency spectrum.
- Broad range of 400 SSI cells.
- 300 element macrofunction library.
- Design For Test includes LSSD macro library option and IEEE 1149.1 JTAG Boundary Scan architecture built in.
- Cadence and Mentor based design system with interfaces from multiple workstations.
- Broad ceramic and plastic package range.
- Latchup trigger current +/- 500 mA.
  ESD protection +/- 4000 volts.

Table 1. Product range

Internal Device Name	Total Sites[1]	Estimated Gates[2]	Total Usable Gates[3]	Maximum Device Pads[4]	Maximum I/O[5]
ISB35083	124,416	82,944	58,060	188	172
ISB35130	194,400	129,600	90,720	232	216
ISB35166	249,696	166,464	116,524	260	244
ISB35208	311,904	207,936	145,555	288	272
ISB35279	418,176	278,784	195,148	332	316
ISB35389	584,064	389,376	253,094	388	372
ISB35484	726,624	484,416	314,870	432	416
ISB35666	998,784	665,856	399,513	504	488
ISB35832	1,247,616	831,744	499,046	560	544

Notes : 1. Internal sites is based on the number of placement sites available to the route and place software
2. A factor of 1.5 is used to derive the gate complexity from the total available sites. This number is in Nand2 equivalents
3. Factors of 70%, 65%, and 60% have been used to calculate the routing efficiency. This number may vary depending on the design.
4. 16 corner pads are dedicated to internal and external power supplies. I/O pads may be configured for additional power.
5. Maximum I/O = total device pads minus power pads.

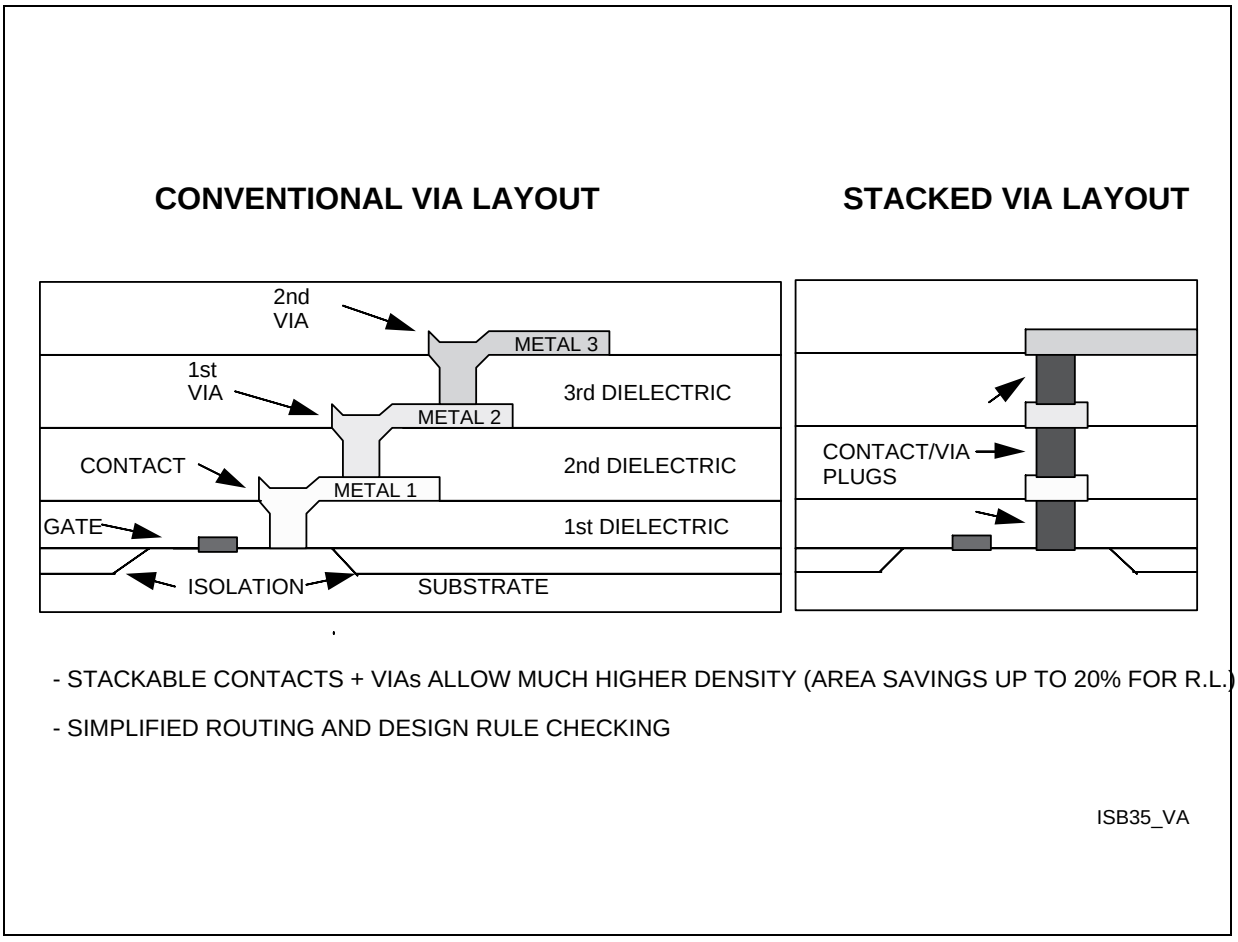
GENERAL DESCRIPTION

The ISB35000 array series uses a high performance, low voltage, triple level metal, HCMOS 0.5 micron process to achieve sub-nanosecond internal speeds while offering very low power dissipation and high noise immunity. The potential total gate count ranges above 1 million equivalent usable gates. The array operates over a Vdd voltage range of 2.7 to 3.6 volts.

The I/O count for this array family ranges to over 600 signals and 1000 pins dependent upon the package technology utilized. A Sea of I/O approach has been followed to give a solution to today's problems of drive levels and specialized interface standards. The array does not utilize a set bond pad spacing but allows for pad spacings from 80 microns upwards.

The I/O can be configured for circuits ranging from low voltage CMOS and TTL to 200 mHz plus low swing differential circuits. Standards like GTL, SCSI-2, 3.3 Volt PCI, CTI, and a limited set of 5.0 Volt interfaces are currently being addressed. A specialized set of impedance matched transmission line driver LVTTL type circuits are also available with 25, 35, 45, and 55 Ohm output impedance. These buffers sacrifice direct current capabilities for matching positive and negative voltage and current waveforms.

Figure 1. Advantages of stacked contacts and vias

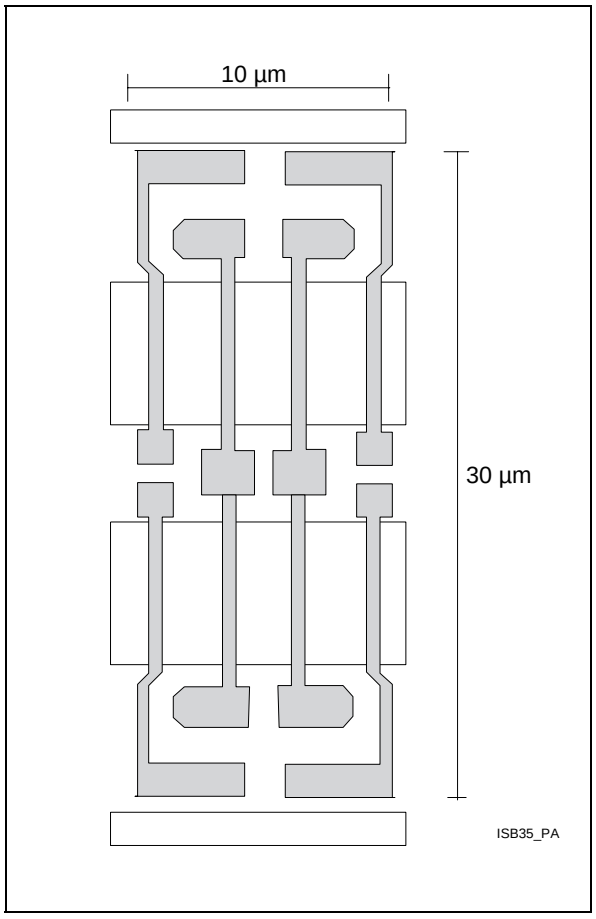


TECHNOLOGY OVERVIEW

The design of ISB35000 internal cell is a proprietary design variation of the CONTINUOUS ARRAY architecture previously used in ISB12000, 18000, and 24000 array families. This proprietary (patent pending) configuration has been named THE DOUBLE BUFFER CELL. This configuration provides a core that is completely filled with potently active transistors. Surrounding the core are configurational specialized transistors forming a Sea of I/O giving a high degree of flexibility to the system designer. The ISB35000 supports the routing of signals over unused transistors as needed. Three levels of metal are utilized, intracell and intercell wiring are limited to first metal with second and third metal levels dedicated to interconnect wiring and power distribution.

The basic cell is made up of four N and four P type transistors that are vertically arranged. The centre two pairs of transistor have common polysilicon gates, while the outer two pairs have separate gates for the polysilicon transistors. The cell was configured to allow extremely high density macro design for internal macro cell counts over one million gates while enabling paralleling of transistors to allow high drive capability and the symmetry of the rise and fall of macro outputs hence the DOUBLE BUFFER name. Each cell has twelve horizontal wiring channels on first metal, four vertical wiring channels on second metal and a further twelve channels on third metal. The HCMOS5 process technology allows for adjacent vias and stacked via1, via2 with or without silicon contacts. The transistor width utilized by the DOUBLE BUFFER cell is very small as compared to previous technologies. Even though the basic cell consists of eight transistors adjacent macros share transistors across the cell borders allowing high density usage of the resources.

Figure 2. Internal Core Cell



Macros are constructed using resources from one half cell to tens of cells dependent upon the complexity of the function. The transistors within and between cells are placed adjacent to each other sharing source and drain regions. All isolation is achieved by cutting off adjacent source drain regions with turned off transistors.

A further feature of the Double Buffer cell that helps allow it to obtain very high density usage is the proprietary (patent pending) method of localized power distribution. A major feature of the HCMOS5 process is salicided active areas. This results in source drain areas that are of one to two ohms resistance as opposed to the hundreds or thousands of ohms of source drain resistance in previous technologies. This very low resistance is one reason that very low transistor widths could be utilized in the cell design since drive is not lost due to source drain resistance. This use of low width transistors results in lower capacitance loading of the gates due to the smaller areas utilized. Low resistance, low capacitance, and small gates results in low power usage for inverters as compared to previous ISB technologies. This reduction in power allows the use of salicided active stripes for power distribution replacing the first level metal buses used in previous technologies. This removal of the metal one power buses simplified macro layout allowing additional wiring resources to be left for the router allowing a higher density usage of the array than would be achievable with previous power distribution techniques. One other gain in the performance of the array and its usability for the customer was derived from the use of the salicided

active power distribution. Since the power distribution serves as the well ties the inherent capacitance of the reversed biased well junctions is closely coupled into the power distribution and functions as localized decoupling capacitance helping to keep high frequency noise from being coupled from one macro to the other through the power distribution.

The salicided active local distribution of the DOUBLE BUFFER cell is supplied its power by a screen grid of power bused on both second and third metal. The second metal buses run every nine cells and are two wiring tracks wide. Vss and Vdd is interleaved every other bus. The third level buses run every thirty six tracks and are three tracks wide. This grid is sufficient to power all but the largest arrays though the use of custom structured cores or gate counts above 500,000 usable cells along with high clock rates may result in the need for supplemental power. The overall die power distribution is broken down into a minimum of three Vdd and three Vss distributions. Optionally other distributions for specialized I/O may be inserted. The standard distributions are Internal Vdd and Vss, serving the internal cells and the prebuffer sections of the I/O, External Vdd and Vss serving the output transistors only, and Receiver Vdd and Vss serving the first stages of the receiver cells. Optional distributions for 5.0V interface, GTL, CTL, and other standards can be utilized as necessary.

LIBRARY

The following section details the elements which make up the ISB35000 Series library. The elements are organised into three categories:

1. Macrocell library with Input, Output, Bidirectional Buffers including JTAG macrocells and Core cells.
2. Macrofunctions
3. Module generators
4. Embedded Functions

I/O BUFFERS

ISB35000 technology does not utilize a standard type I/O cell but is a leader in the emerging Sea of I/O approach to handling the chip interface problem. This approach starts at the bond pad area of the I/O where the pad size and pitch is not determined until the customers choice of packaging, signal interface standards and I/O count is considered. Wire bond pad spacings for 80 micron centres are available where large signal counts are most important. Pad spacing can be increased incrementally. It is expected that most designs will use 100 or 120 micron spacings. It is also possible to use different spacings for different width output sections when needed within the same device.

Along with the variable bond pad spacing the I/O output transistor section does not have a fixed width. Previous technologies utilized a design approach where the desired full function buffer was designed for a maximum current taking one pad location with the usual current in the range of twenty four milliamps. The approach followed in ISB35000 is to have identical twenty micron wide output transistor slices stepped around the die. Each slice contains one set of protection diodes to the external power rails and eight P and eight N transistors. The transistors are specifically laid out and selectively non salicided for ESD protection and latch up prevention. These slices are paralleled to meet the current needs of the user, for example, to construct a 24mA sink and 12mA source LVTTL buffer, a number of slices would be used. The next group of devices that makes up the I/O circuits is again a 20 u wide slice of specialized transistors that are utilized to form the slew rate control sections of the I/O. Each of these slices has circuits to control the switching of up two sections of P and N output transistors. These sections are of course created from the output transistor slice above the slew rate section and can be connected as desired by the designer. Many configurations of circuits can be created to supply the desired results with slew rate slices paralleled with multiple output sections. A further function of the scan circuits is current spike suppression during switching of the I/O transistors. The logic utilized causes the conducting transistors to turn off before the opposing set of transistors turn on.

Inside the slew rate sections the next slices of specialized designed components step on a 40 micron wide pattern. The first of these 40 micron wide sections is utilized for predriver circuits; these include specialized built in test functions for the I/O. The predriver of course interfaces the core signals controlling tristate and switching functions with the slew rate and output transistor sections but it also allows all Output Buffers to be driven high, low or put into tristate regardless of the state of the internal logic greatly simplifying parametric testing of the part and also assisting customers who wish to use this feature during board testing. Note that all output

buffers can be tristated by this function including buffers that normally do not tristate. This test function also turns off all pull up or down devices and shuts down all differential receivers and converts them into standard CMOS receivers. Inside the predriver is a section of specialized transistors used to create the receiver functions. This section includes specialized non salicide protection resistor diodes to further protect the gates of the receiver devices from ESD and latch up. Also present in this section are devices that can be utilized to form various parameteriseable pull up, pull down and buskeeper functions. A full set of standard receivers with pull up and pull down devices is present in the library. The technologies supported match the output buffer capabilities and include, LVCMOS, LVTTL, GTL, CTL, Differential, etc. and a five volt interface capability. The last section of devices that make up the I/O ring is a set of custom designed (for compactness) scan latches and supporting circuits that can be utilized to form various types of scan circuits conforming to the standard that the customer is utilizing in his systems. These circuits can be combined with internal transistors if needed.

Figure 3. ISB35000 I/O Technology

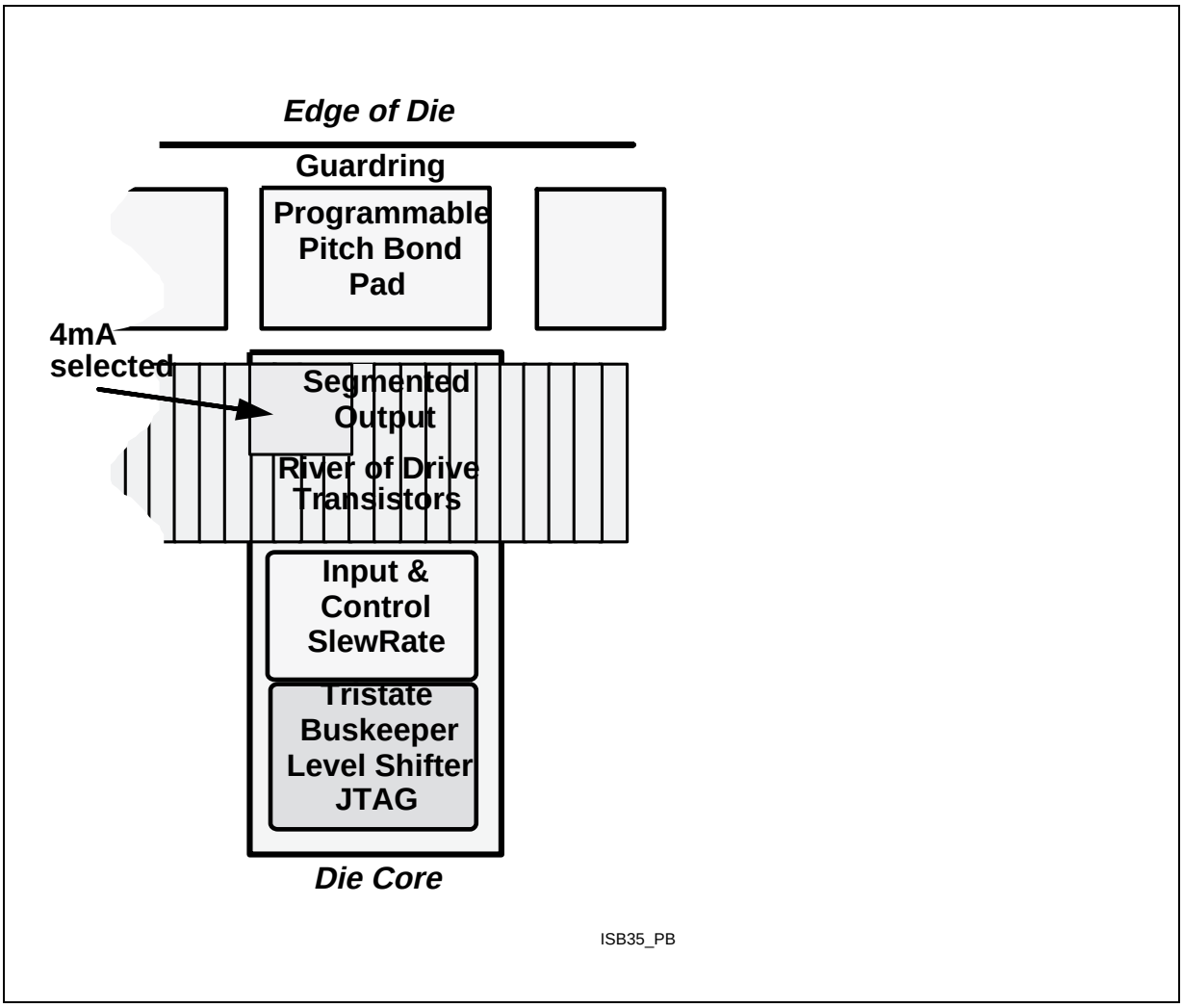


Figure 4a. D.C. Specifications for LVCMOS Input Receivers

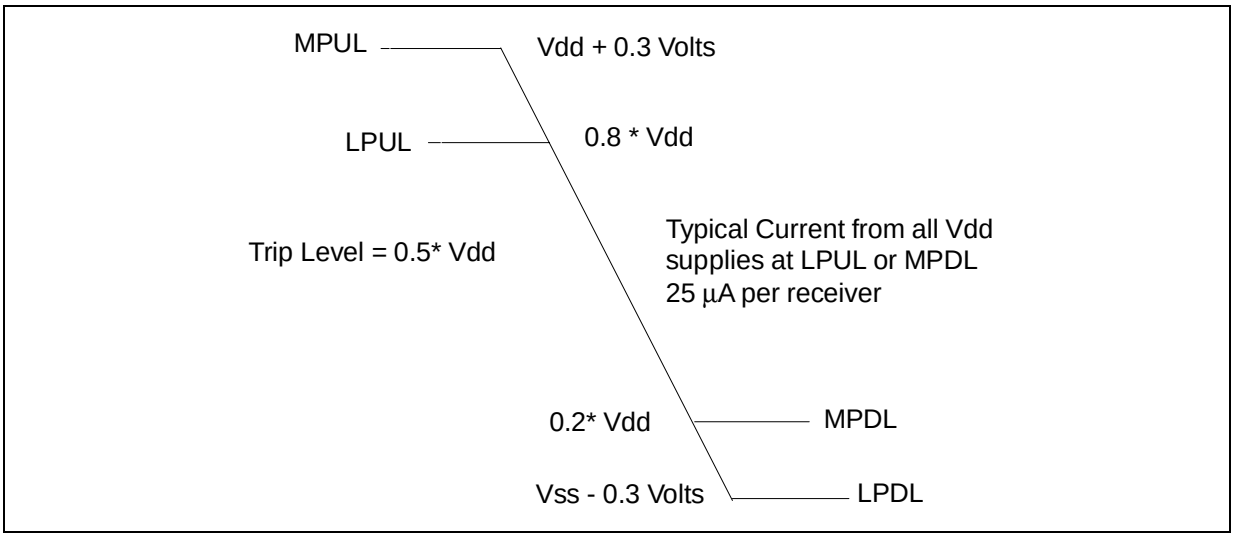


Figure 4b. D.C. Specifications for LVTTL Input Receivers

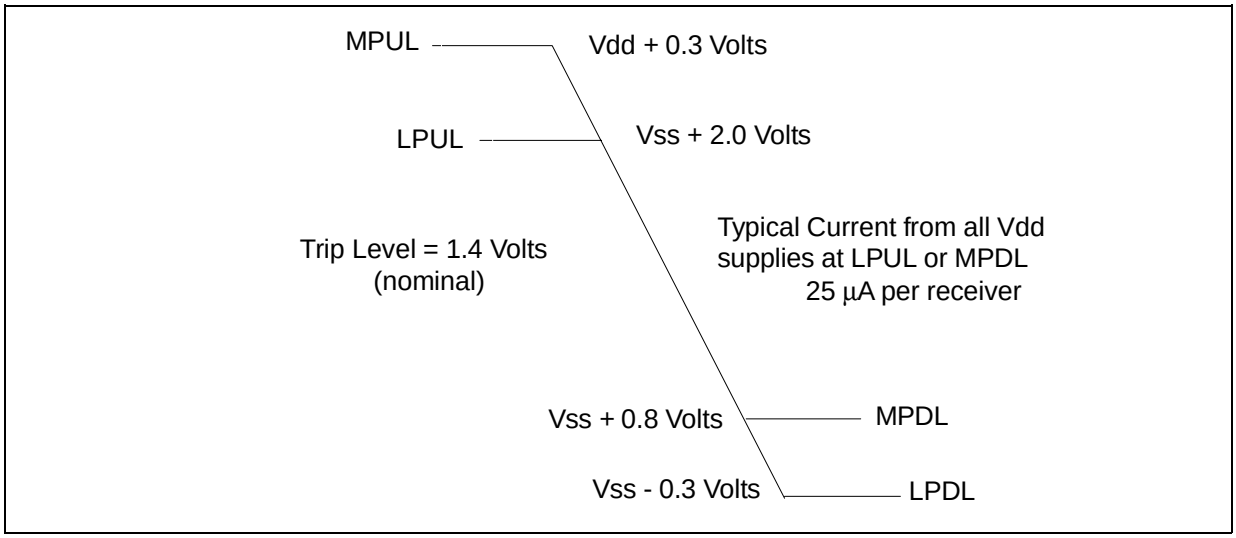


Table 2. I/O Drive Capacity for LVCMOS and LVTTL Slew Rate Buffers

Current Drive (mA)	Maximum Capacitance (pF)
2.0	50
4.0	100
8.0	200
12.0	300
16.0	400
24.0	800

Table 3. I/O Drive Capacity for LVCMOS and LVTTL Non Slew Rate Buffers

Current Drive (mA)	Maximum Capacitance (pF)
2.0	50
4.0	100
8.0	200
12.0	300
16.0	400
24.0	800

Table 4. Temperature (Junction) and Voltage Multipliers

Temperature °C	K_T
-55	0.77
-40	0.83
25	1.00
70	1.13
85	1.17
125	1.27
V_{DD}	K_V
2.7	1.20
3.0	1.11
3.3	1.00
3.6	0.94

All pads except the sixteen corner pads can be configured as power or I/O pads. The configured power pads are known as placeable pads and have an associated current handling capability. Their placement is dependent on the types of output buffers used in the design. For rules governing the placement of pads, please contact your local SGS-THOMSON design centre.

CORE LOGIC

The propagation delays shown in the ISB35000 data book are given for nominal processing, 3.3V operation, and 25 C temperature conditions.

However there are additional factors that affect the delay characteristics of the macrocells. These include loading due to fanout and interconnect routing, voltage supply, junction temperature of the device, processing tolerance and input signal transition time. Prior to physical layout, the design system can estimate the delays associated with any critical path. The impact of the placement and routing can be accurately RC back annotated from the layout for final simulations of critical timing. The effects of junction temperature, (K_T) and voltage supply (K_V) on the delay numbers are summarized in Table 4. A third factor, is associated with process variation. This multiplier has a minimum of 0.6 and a maximum of 1.6.

MACROCELLS AND MACROFUNCTIONS

The ISB35000 series has internal macrocells that are robust in variety and performance. The cell selection has been driven by the need of Synthesis and HDL based design techniques. This offering is rich in buffers, complex combinatorial cells and multi power drive cells, which allow the Synthesis tool to create a netlist compatible with the requirements of Place and Route tools.

Macrofunctions are a series of soft-macros facilitating quick capture of large functional blocks and are available for such functions as counters, shift register and adders. Macrofunctions are implemented at layout by utilizing macrocells and interconnecting to create the logic function.

MODULE GENERATORS

A series of module generators are available to support a range of megafunctions. These modules enable the designer to choose individual parameters in order to create a compiled cell, which meets the specific application requirements.

Generators are available for megafunctions such as single port RAM and dual port RAM. These are constructed utilising the existing base array transistors, and are also referred to as metallised megafunctions.

EMBEDDED FUNCTIONS

In addition to the metallised functions described above, embedded megafunction generators are also available. These include single port RAM, dual port RAM and ROM.

The compiled cell generators construct custom cells, which are implemented using a special leaf cell technique, ensuring predictable layout and accurate module characteristics.

In choosing megafunctions the designer can consider the trade-offs between speed and area to generate a fully customized cell which meets their specific device requirements.

These megafunction generators are complemented by a group of embedded megacells.

Table 5. Module Generator Library

Cell		Description
SPRAM	Metallised	8K bits max 2048 word max 64 bit max Zero static current Tristate output
	Embedded	256K bits max 16K word max 64 bit max Zero static current Tristate outputs
DPRAM	Metallised	4K bits max 1024 word max 64 bit max Zero static current Separate read/write ports Tristate outputs
	Embedded	128K bits max 8K word max 64 bit max Zero static current Tristate outputs
ROM	Embedded	2M bits max 32K word max 64 bit max Diffusion programmable Tristate outputs

These allow access to technologies that have been hitherto the domain of standard products.

Examples include mixed mode cells for graphics, DAC/ADC's (4-9 bit), PLL applications, and Digital Signal Processor functions for cellular comms, fax and high-speed modem.which initially consist of a Triple 8-bit DAC, Graphics RAM, Clock Multiplier PLL and Frequency Synthesis PLL.

100 Mbps serial transputer links coupled with large and fast memory can be used for pipelining, caching and synchro circuits in modern RISC computing architectures.

Viterbi and Reed Solomon cores aim at the HDTV and satellite transmission markets. To support telecom needs for CCITT standard applications, ADPCM cells supporting CT2 protocol have been developed.

DESIGN FOR TESTABILITY

The time and cost for ASIC testing increases exponentially as the complexity and size of the ASIC grows. Using a design for testability methodology allows large, more complex ASICs to be efficiently and economically tested.

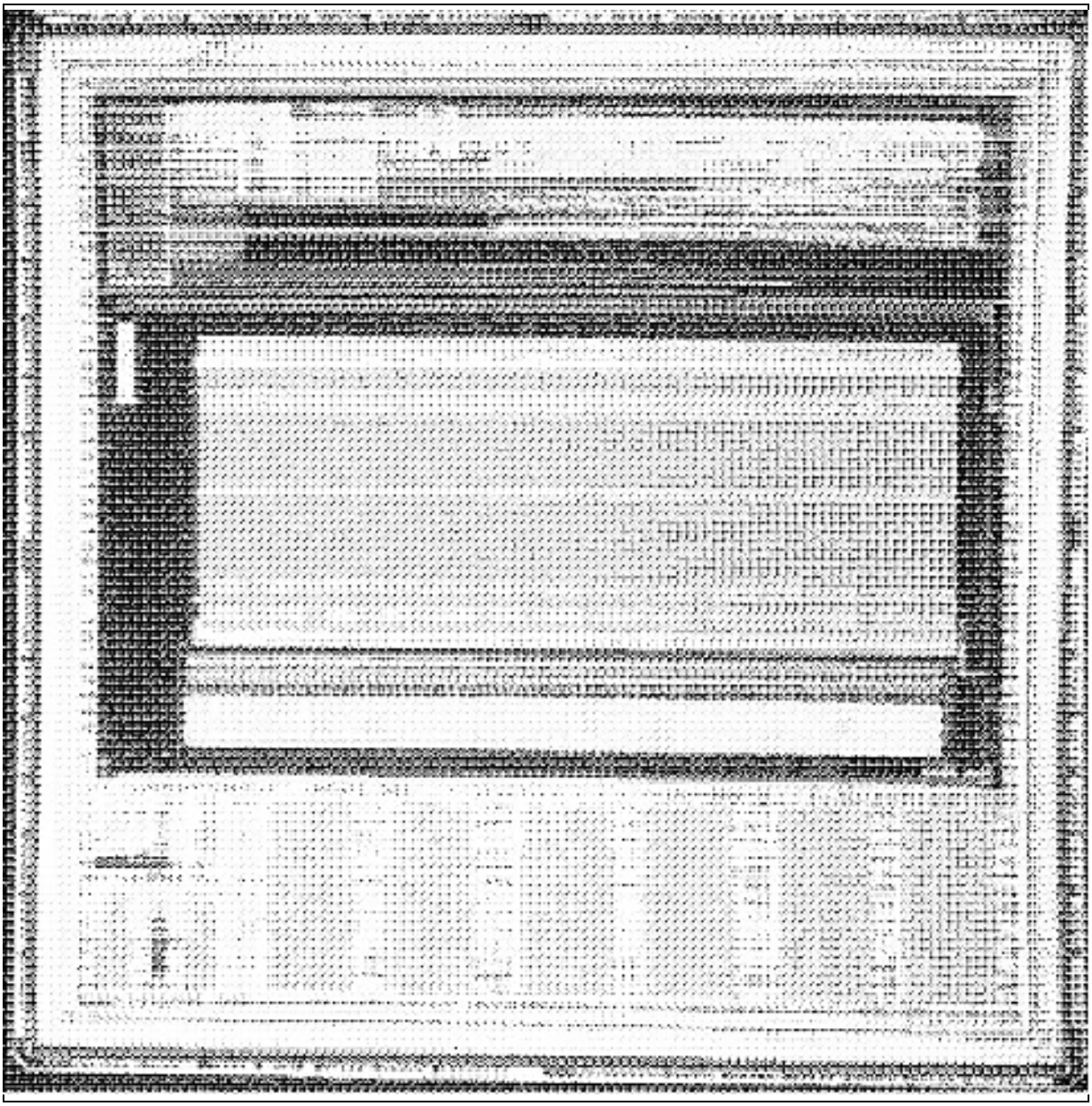
ISB35000 supports the JTAG boundary Scan and both edge and level sensitive scan design techniques by providing the necessary macrocells. Scan testing aids device testability by permitting access to internal nodes without requiring a separate external connection for each node accessed. Testability is assured at device level with the close coupling of LSSD latch elements, Automatic Test Pattern Generation (ATPG) and high pattern depth tester architecture.

At system level, SGS-THOMSON fully supports IEEE 1149.1, within the I/O structure utilised in this family. Several types of core scan cells are provided in the ISB35000 Series library. Examples include FDxS/FJKxS cells which are edge sensitive and LSxx cells which are true LSSD cells.

EVALUATION DEVICE

An evaluation device is used to demonstrate the performance of the ISB35000 series as well as verify the effectiveness of the design system. The device has path delays, latches, a host of macrocells and embedded functions which were used to verify the simulated characteristics that are supplied in the data book. Characterization of the path delays including interconnect shows typical delays of 210 ps for a 2 input NAND with receivers/drivers operating at frequencies of 200 MHz. The evaluation device is available in a 208 pin plastic quad flat pack.

Figure 5. Evaluation Device



PACKAGE AVAILABILITY

The ISB28000 Series is designed to be compatible with QFP, BGA and SBC package types, in addition to the more traditional types found.

The options include Plastic Leaded Chip Carriers (PLCC) from 28 to 84 pins, while the Metric Quad Flat Pack (xQFP) offering ranges up to 304 pins. Both high performance and high power variants are available as well as the TQFP thin types.

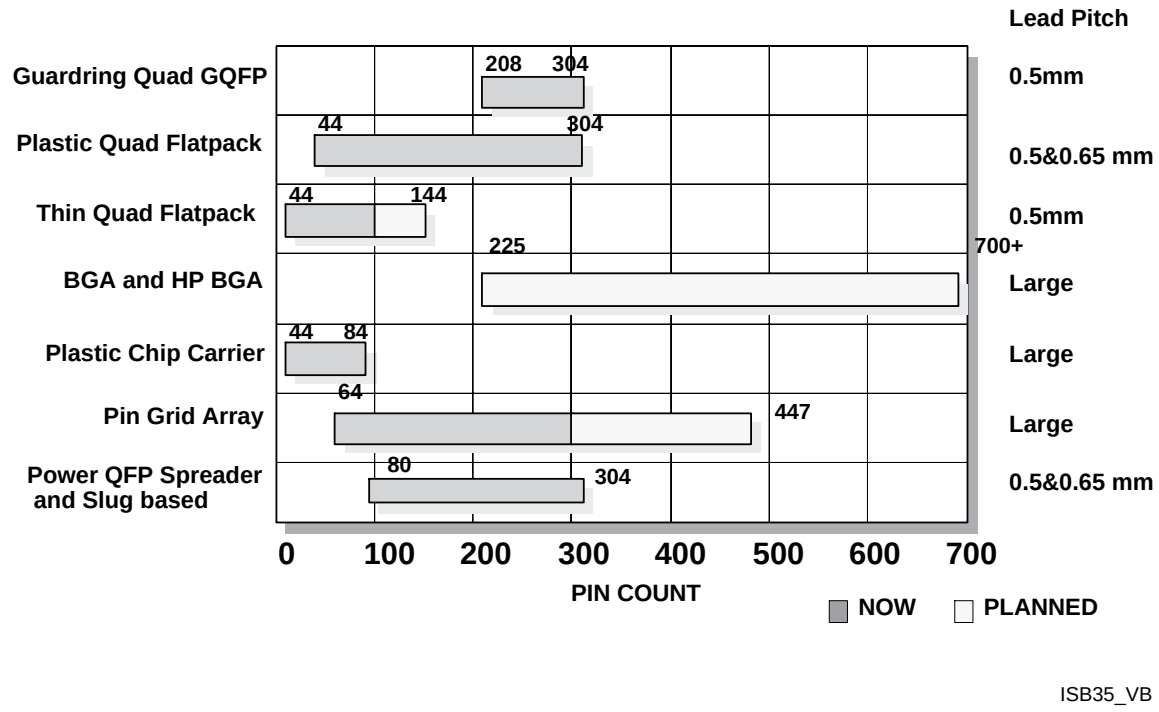
Ball Grid Array (BGA) packages are available from 160 to 500 pins and SBC types allow the pin count to reach the area of 1000 pins.

Pin counts for through board mounting range up to 299. For higher pin counts the range is compatible with the industry standard JEDEC and EIA-J Guardring Quad Flatpack (GQPF) with pin counts from 186 to 304.

The diversity in pin count and package style gives the designer the opportunity to find the best compromise for system size, cost and performance requirements.

All packages for the military market are hermetically sealed to meet MIL-STD-883 Method. Prototypes are developed in ceramic packages for fast turnaround evaluation.

Figure 6. Packaging Capability



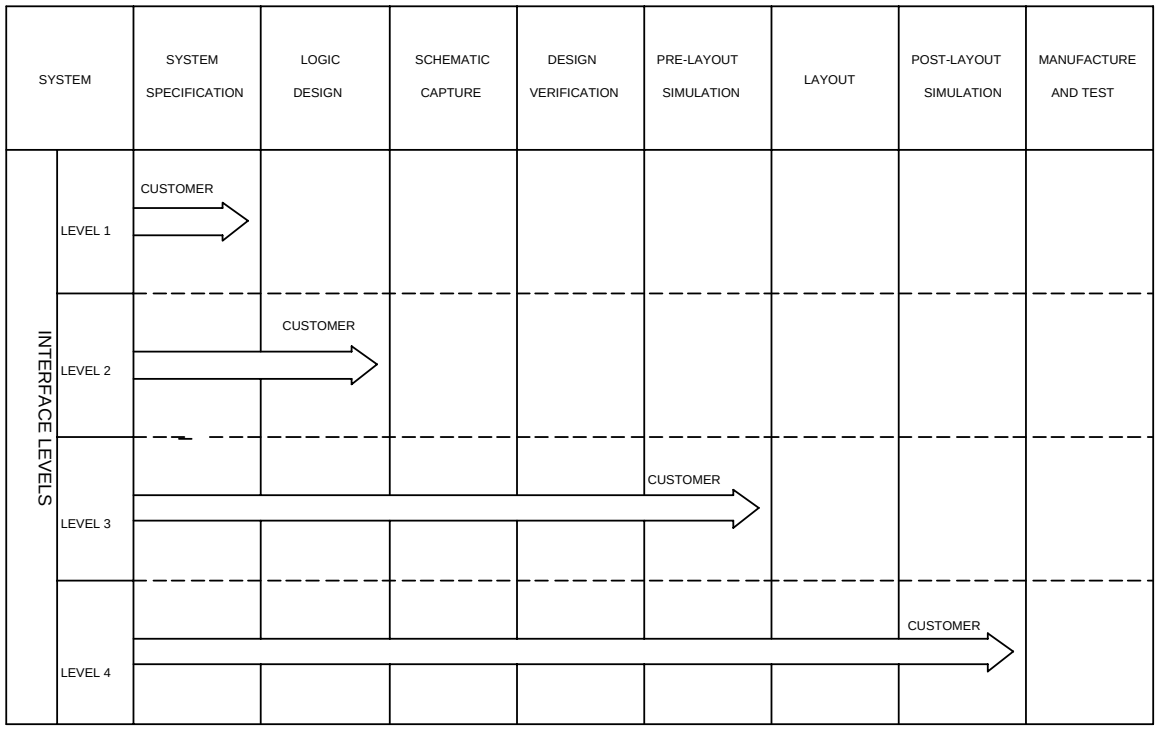
DESIGN ENVIRONMENT

Several interface levels are possible between SGS-THOMSON and the customer in the undertaking of an ASIC design. The four levels of interface are shown in Figure 7. Level 1 is characterized by SGS-THOMSON receiving the system specification and taking the design through to validation and fabrication. At level 2 interface the designer supplies a complete logic design implemented in a standard generic logic family. SGS-THOMSON then takes the design through to layout, validation and fabrication.

Level 3 is the most common and preferred interface level. Logic capture and pre-layout simulation are performed by the designer using an SGS-THOMSON supported design kit. The design is then taken through layout, validation and fabrication by SGS-THOMSON.

The SGS-THOMSON design system validates all designs before fabrication. Design kits are provided that allow schematic capture entry via Mentor Graphics and Cadence Amadeus. Simulation is supported on Cadence Amadeus and Mentor Graphics. Full support is also provided for Cadence Verilog, Synopsys VSS and System Hilo simulators. Figure 8 shows the SGS-THOMSON Design Flow.

Figure 7. Customer/SGS-THOMSON Interface Levels



ISB35_VC

Figure 8. SGS-THOMSON Design Flow

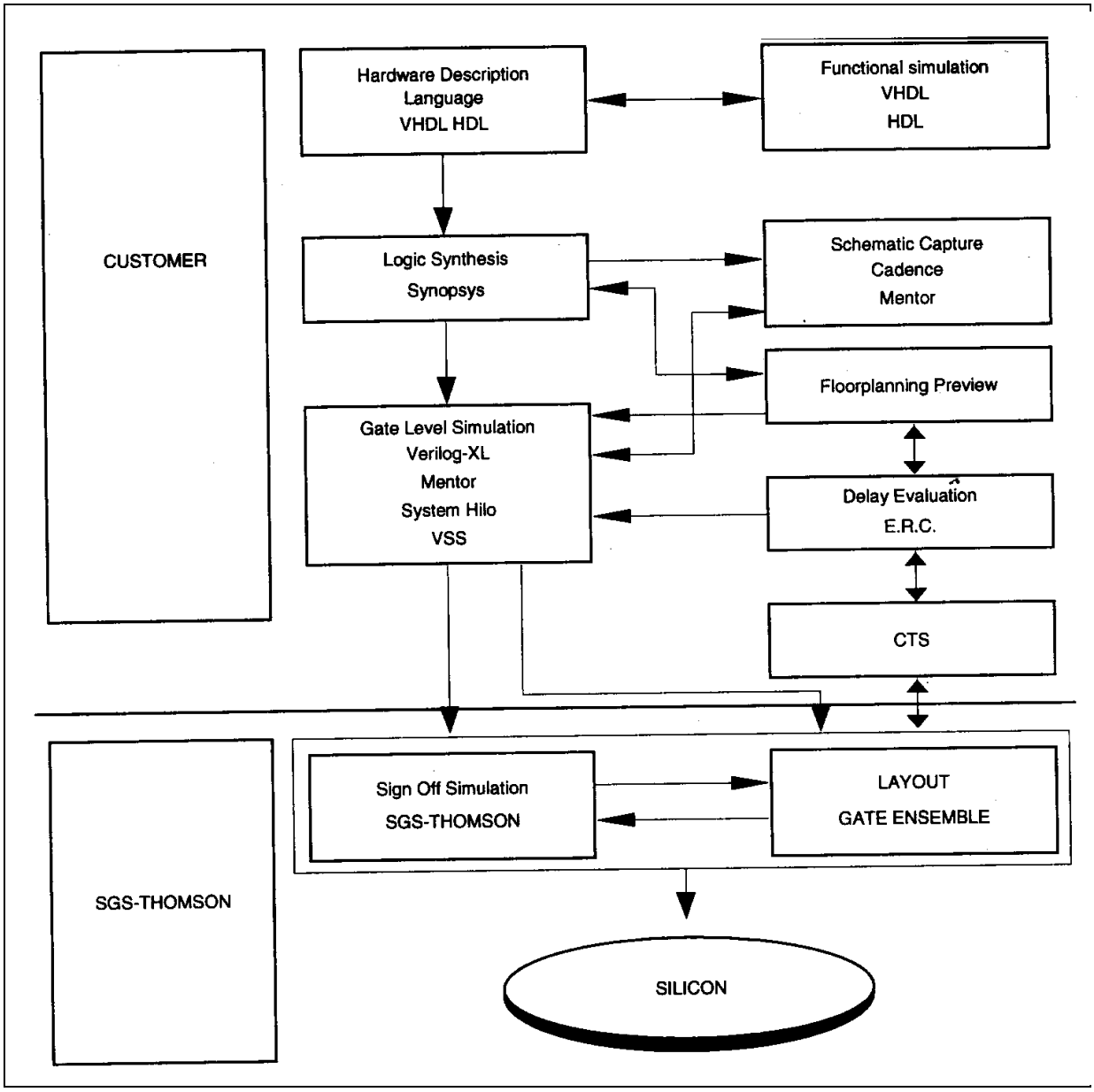


Table 6. Absolute Maximum Ratings (note1)

Supply Voltage, V_{dd}	-0.5 V to +6.0 V
Input or Output Voltage	-0.5 V to (V_{dd} + 0.5V)
DC Forward Bias Current, Input or Output	-24mA source, +24mA sink
Storage Temperature Ceramic	-65 to 150 degrees Centigrade
Storage Temperature Plastic	-40 to 125 degrees Centigrade

Note 1. Referenced to Vss. Stresses above those listed under “absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 7. Recommended DC Operating Conditions

Normal Operating Supply Voltage V_{dd} (note 1)	3.3 V +/- 10% (3.0 V to 3.6 V)
Extended Operating Supply Voltage V_{dd} (notes 1,2)	3.3 V + 0.3V/-0.6V (2.7V to 3.6V)
Operating Ambient Temperature Commercial (note 3) Industrial (note 3) Military (note 4)	 0 to 70 degrees Centigrade -40 to +85 degrees Centigrade -55 to +125 degrees Centigrade

Note 1. Commercial, Industrial, and Military Conditions
Note 2. Low Voltage TTL Circuits are NOT functional to specifications below 3.0 Volts
Note 3. All circuits will operate to full specifications with a V_{DD} of 3.0V to 3.6V and a junction temperature of -40 to +125 degrees centigrade. These junction temperatures are compatible with the Commercial and Industrial Temperature Ranges.
Note 4. All circuits will be functional from -55 to +150 degrees centigrade junction temperature (military Ambient Temperature Range) but will not necessary operate to published specifications. Only circuits specified as operational to extended temperature range may be used when operating to Military temperature conditions.

Table 8. Special Voltages (V_{cc}) Operating Conditions

FVI (Five Volt Interface) Supply Voltage (notes 1,2)	5.0V +/- 10% (4.5 V to 5.5 V)
GTL (Gunning Transistor Logic) Supply Voltage (notes 1,3)	1.2V +/- 5% (1.14 V to 1.26 V)
CTT (Center Tap Terminated) Supply Voltage (notes 1,4)	1.5V +/- 10% (1.35 V to 1.65 V)

Note 1. Commercial, and Industrial Use Only -40 +85 degrees Centigrade
Note 2. I/O Circuits Only takes Special External Power Distribution and May NOT be mixed with GTL or CTL circuits on any one side of the die. Only a very limited buffer set is available.
Note 3. I/O Circuits Only takes Special External Power Distribution and May NOT be mixed with FVI or CTL circuits on any one side of the die. Only a very limited buffer set is available.
Note 4. I /O Circuits Only takes Special External Power Distribution and May NOT be mixed with FVI or GTL circuits on any one side of the die. Only a very limited buffer set is available.

Table 9. LVTTL Interface DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{IL}	Low Level Input Voltage				0.8	Volts	2,3
V_{IH}	High Level Input Voltage		2.0			Volts	2,3
V_{OL}	Low Level Output Voltage	I_{OL} = Rated Buffer Current		0.2	0.4	Volts	2,3,4
V_{OH}	High Level Output Voltage	I_{OH} = Rated Buffer Current	2.4	3.0		Volts	2,3,4
V_{t+}	Schmitt Trigger +Ve Threshold			1.7	1.9	Volts	2,3
V_{t-}	Schmitt Trigger -Ve Threshold		0.9	1.1		Volts	2,3

Note 1. These are normal Voltage and extended temperature specifications V_{DD} from 3.0 V to 3.6 V
Temperature Ambient from -55 to 125 degrees Centigrade
Note 2. Adherence to rules in Power Pin / Pad Specifications Required
Note 3. Refer to the ISB35000 Gate Array Specification for full Testing Levels and Conditions
Note 4. Buffers offered in 2, 4, 8, 12, 16, and 24 mA TTL options

Table 10. LVCMOS Interface DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{IL}	Low Level Input Voltage				$0.2xV_{DD}$	Volts	2,3,4
V_{IH}	High Level Input Voltage		$0.8xV_{DD}$			Volts	2,3,4
V_{OL}	Low Level Output Voltage	I_{OL} = Rated Buffer Current		0.2	0.4	Volts	2,3,4,5,6
V_{OH}	High Level Output Voltage	I_{OH} = Rated Buffer Current	0.85 x V_{DD}	0.9 x V_{DD}		Volts	2,3,4,5,6
V_{t+}	Schmitt Trigger +Ve Threshold			1.7	1.9	Volts	2,3
V_{t-}	Schmitt Trigger -Ve Threshold		0.9	1.1		Volts	2,3

Note 1. These are extended voltage and temperature specifications
V_{DD} from 2.7 V to 3.6 V
Temperature Ambient from -55 to 125 degrees Centigrade
Note 2. Adherence to rules in Power Pin / Pad Specifications Required
Note 3. Refer to the ISB35000 Gate Array Specification for full Testing Levels and Conditions
Note 4. Buffers offered in 2, 4, and 8 mA CMOS options
Note 5. Note only one CMOS buffer may sink or source DC current when parametric measurements are taken due to the reason that the power supply specifications for CMOS product are not written to support DC current. If more than one buffer is active voltage drops in the supply may cause false failure readings.
Note 6. If no buffers are sinking or sourcing current and all internal pull up or pull down resistors in bidi buffers have been disabled by having the T2 Test Pin positive V_{OL} (max) = 0.05 Volts and V_{OH} (min)=V_{DD}-0.05 Volts

Table 11. General Interface DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
I_{IL}	Low Level Input Current	$V_I = V_{ss}$			+/-10	uA	2
I_{IH}	High Level Input Current	$V_I = V_{dd}$			+/-10	uA	2
I_{OZ}	Tri-State Output Leakage	V_O = 0V or V_{dd}			+/-10	uA	2
C_{IN}	Input Capacitance	Freq=1MHz		2.0	4.0	pF	3,4
C_O	Output Capacitance	Freq=1MHz		4.0		pF	3,4
C_{IO}	Bidi, I/O Capacitance	Freq=1MHz	0.9	1.1		Volts	3,4
I_{KLU}	I/O Latch Up Current	$V<V_{SS}$, $V>V_{DD}$	200	500		mA	
V_{ESD}	Electrostatic Protection	HBM	2000	4000		V	5

Note 1. These are extended voltage and temperature specifications
V_{DD} from 2.7 V to 3.6 V
Temperature Ambient from -55 to 125 degrees Centigrade
Note 2. Adherence to rules in Power Pin / Pad Specifications Required
Note 3. Excluding Package
Note 4. At 0.0 Volts
Note 5. Human Body Model