

**8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS**

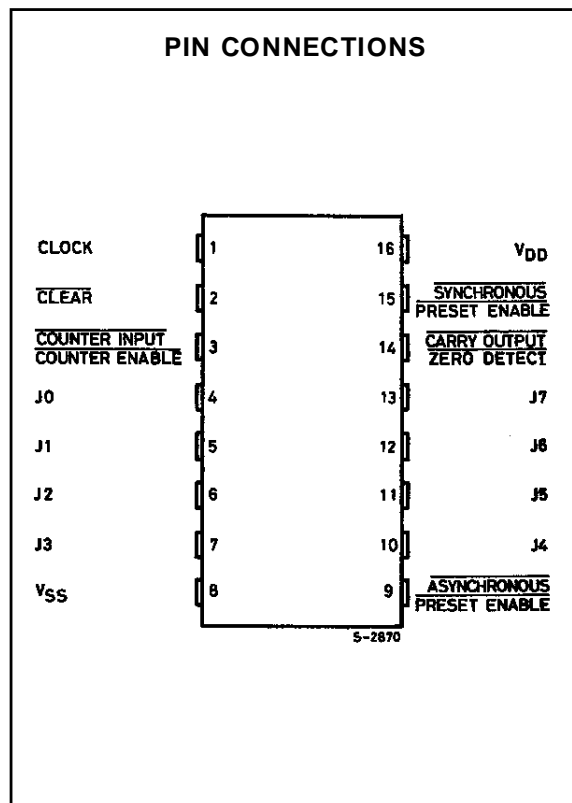
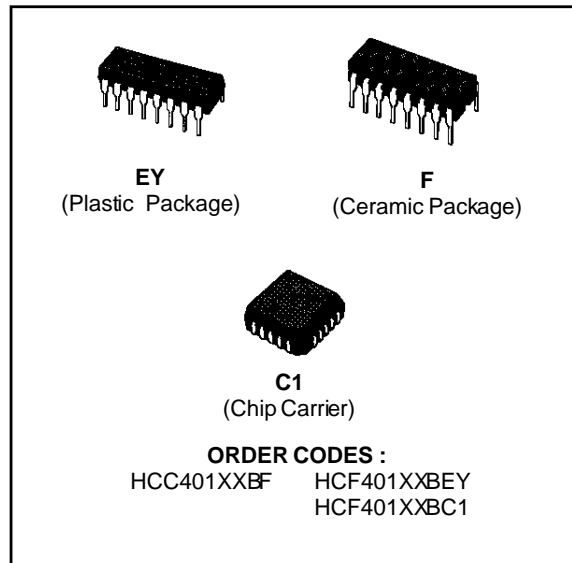
**40102B 2-DECADE BCD TYPE**

**40103B 8-BIT BINARY TYPE**

- SYNCHRONOUS OR ASYNCHRONOUS PRESET
- MEDIUM-SPEED OPERATION :  $f_{CL} = 3.6\text{MHz}$  (TYP.) @  $V_{DD} = 10\text{V}$
- CASCADABLE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N° 13 A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

**DESCRIPTION**

The **HCC40102B**, **HCC40103B**, (extended temperature range) and the **HCF40102B**, **HCF40103B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF40102B**, and **HCC/HCF40103B** consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The **HCC/HCF40102B** is configured as two cascaded 4-bit BCD counters, and the **HCC/HCF40103B** contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE (CI/CE) input is high. The CARRY-OUT/ZERO-DETECT (CO/ZD) output goes low when the count reaches zero if the CI/CE input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the CI/CE input. When the ASYNCHRONOUS PRESET-ENABLE (APE) input is low, data at the

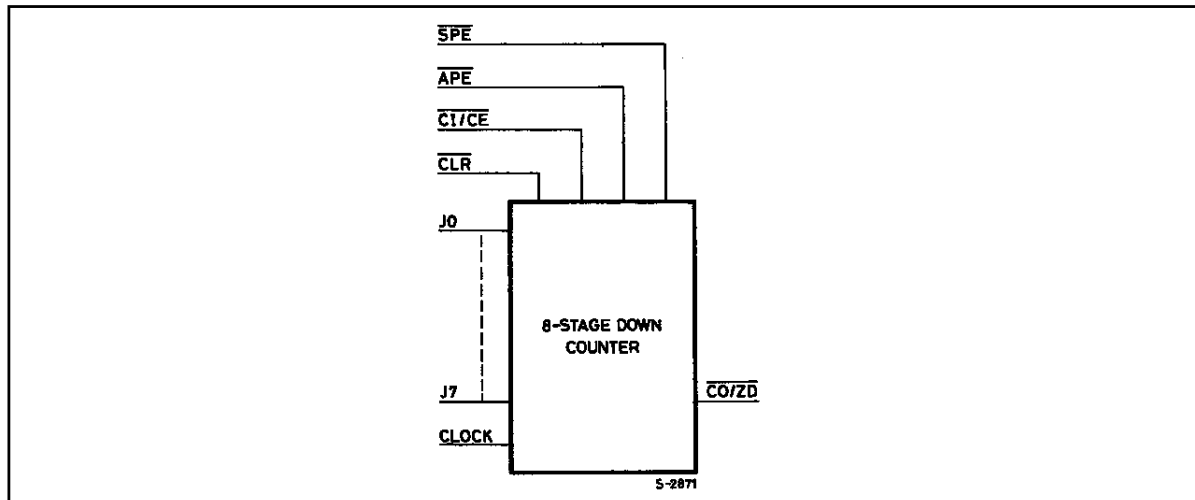


## HCC/HCF40102B/40103B

JAM inputs is asynchronously forced into the counter regardless of the state of the  $\overline{SPE}$ ,  $\overline{CI/CE}$ , or  $\overline{CLOCK}$  inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the **HCC/HCF40102B** and a single 8-bit binary word for the **HCC/HCF40103B**. When the  $\overline{CLEAR}$  (CLR) input is low, the counter is asynchronously cleared to its maximum count (99<sub>10</sub> for the **HCC/HCF40102B** and 255<sub>10</sub> for

the **HCC/HCF40103B**) regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long. The **HCC/HCF40102B** and **HCC/HCF40103B** may be cascaded using the  $\overline{CI/CE}$  input and the

### FUNCTIONAL DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}^*$	Supply Voltage : <b>HCC</b> Types <b>HCF</b> Types	- 0.5 to + 20	V
		- 0.5 to + 18	V
$V_i$	Input Voltage	- 0.5 to $V_{DD} + 0.5$	V
$I_i$	DC Input Current (any one input)	$\pm 10$	mA
$P_{tot}$	Total Power Dissipation (per package) Dissipation per Output Transistor for $T_{op}$ = Full Package-temperature Range	200	mW
		100	mW
$T_{op}$	Operating Temperature : <b>HCC</b> Types <b>HCF</b> Types	- 55 to + 125	°C
		- 40 to + 85	°C
$T_{stg}$	Storage Temperature	- 65 to + 150	°C

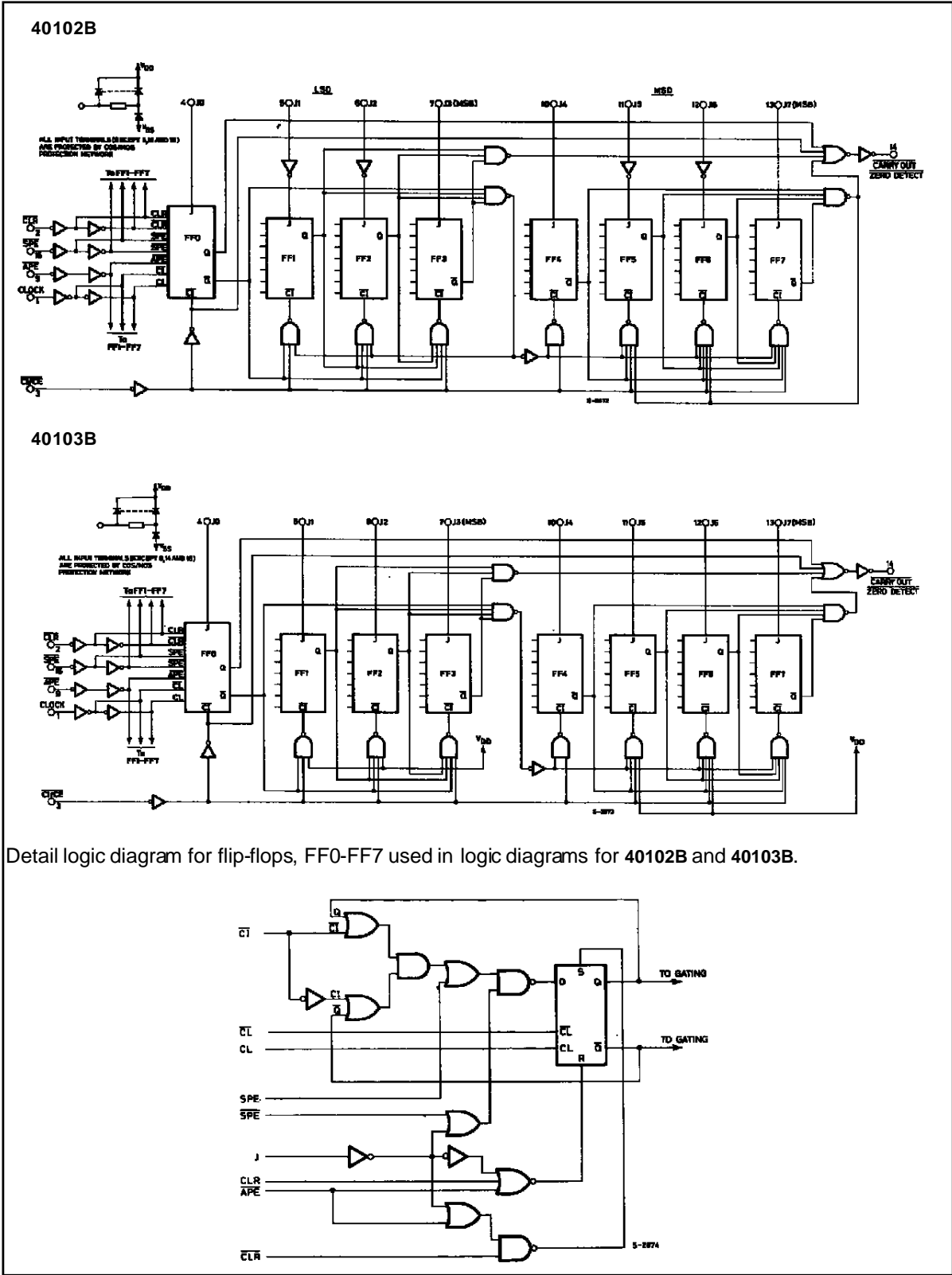
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

\* All voltages are with respect to  $V_{SS}$  (GND).

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage : <b>HCC</b> Types <b>HCF</b> Types	3 to 18	V
		3 to 15	V
$V_i$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature : <b>HCC</b> Types <b>HCF</b> Types	- 55 to + 125	°C
		- 40 to + 85	°C

LOGIC DIAGRAMS

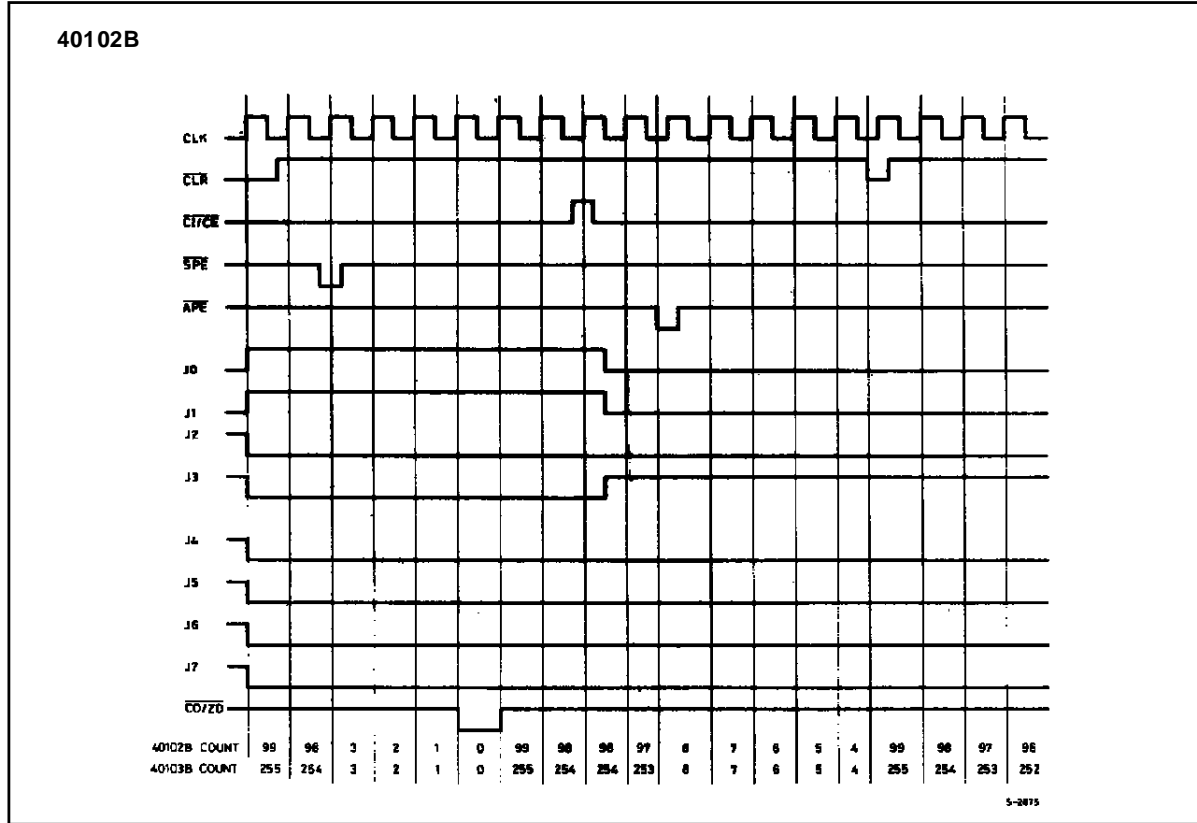


Detail logic diagram for flip-flops, FF0-FF7 used in logic diagrams for 40102B and 40103B.

# HCC/HCF40102B/40103B

## LOGIC DIAGRAMS (continued)

Timing Diagram for 40102B and 40103B



## TRUTH TABLE

Control Inputs				Preset Mode	Action
CLR	APE	SPE	CI/CE		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset on Next Positive Clock Transition
1	0	X	X	Asynchronous	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

- Notes :**
- 0 = Low level  
1 = High level  
X = Don't care
  - Clock connected to clock input.
  - Synchronous operation : changes occur on negative-to-positive clock transitions..  
JAM inputs : HCC/HCF010B ; MSD = J7, J6, J5, J4 (J7 is MSB)  
LSD = J3, J2, J1, J0 (J3 is MSB)  
HCC/HCF40103B Binary ; MSB = J7, LSB = J0

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value						Unit	
			V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>Low</sub> *		25°C			T <sub>High</sub> *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	$\mu$ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000		
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
0/15				15		80		0.04	80		600			
V <sub>OH</sub>	Output High Voltage	0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V <sub>OL</sub>	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V <sub>IH</sub>	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V <sub>IL</sub>	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I <sub>OH</sub>	Output Drive Current	HCC Types	0/ 5	2.5		5	- 2		- 1.6	- 3.2		- 1.15	mA	
			0/ 5	4.6		5	- 0.64		- 0.51	- 1		- 0.36		
			0/10	9.5		10	- 1.6		- 1.3	- 2.6		- 0.9		
		0/15	13.5		15	- 4.2		- 3.4	- 6.8		- 2.4			
		HCF Types	0/ 5	2.5		5	- 1.53		- 1.36	- 3.2		- 1.1		
			0/ 5	4.6		5	- 0.52		- 0.44	- 1		- 0.36		
0/10	9.5			10	- 1.3		- 1.1	- 2.6		- 0.9				
0/15	13.5		15	- 3.6		- 3.0	- 6.8		- 2.4					
I <sub>OL</sub>	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I <sub>IH</sub> , I <sub>IL</sub>	Input Leakage Current	HCC Types	0/18	Any Input	18		$\pm$ 0.1		$\pm 10^{-5}$	$\pm$ 0.1		$\pm$ 1	$\mu$ A	
		HCF Types	0/15		15		$\pm$ 0.3		$\pm 10^{-5}$	$\pm$ 0.3		$\pm$ 1		
C <sub>I</sub>	Input Capacitance			Any Input					5	7.5			pF	

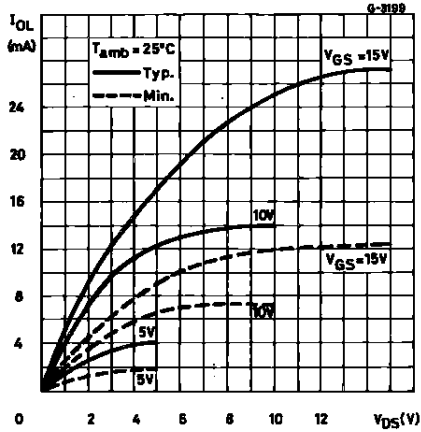
\* T<sub>Low</sub> = - 55°C for HCC device : - 40°C for HCF device.\* T<sub>High</sub> = + 125°C for HCC device : + 85°C for HCF device.The Noise Margin for both "1" and "0" level is : 1V min. with V<sub>DD</sub> = 5V, 2V min. with V<sub>DD</sub> = 10V, 2.5V min. with V<sub>DD</sub> = 15V.

## HCC/HCF40102B/40103B

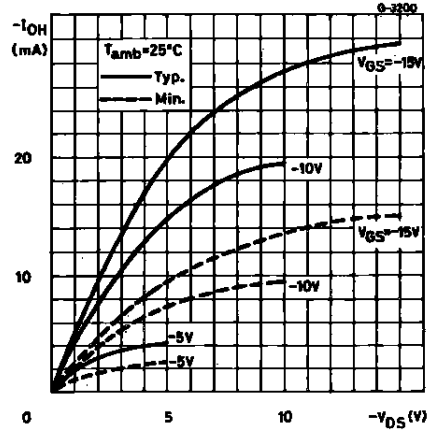
**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$ , typical temperature coefficient for all  $V_{DD}$  values is  $0.3\%/^{\circ}\text{C}$ , all input rise and fall time = 20ns)

Symbol	Parameter		Test Conditions		Value			Unit
			$V_{DD}$ (V)	Min.	Typ.	Max.		
$t_{PHL}$ , $t_{PLH}$	Propagation Delay Time	Clock to-out	5		300	600	ns	
			10		130	260		
			15		95	190		
		Carry In/Counter Enable-to-output	5		200	400	ns	
			10		90	180		
			15		65	130		
		Asynchronous Preset Enable-to-output	5		650	1300		
			10		300	600		
			15		200	400		
		Clear-to-output	5		375	750	ns	
			10		180	360		
			15		100	200		
$t_{THL}$ , $t_{TLH}$	Transition Time		5		100	200	ns	
			10		50	100		
			15		40	80		
$t_w$	Pulse Width	Clock Pulse Width	5	300	150		ns	
			10	180	90			
			15	80	40			
		CLR Pulse Width	5	320	160		ns	
			10	160	80			
			15	100	50			
		APE Pulse Width	5	360	180		ns	
			10	160	80			
			15	120	60			
$t_{setup}$	Setup Time	SPE Setup Time	5	280	140		ns	
			10	140	70			
			15	100	50			
		JAM Setup Time	5	200	100		ns	
			10	80	40			
			15	60	30			
$f_{CL}$	Maximum Clock Input Frequency		5	0.7	1.4		MHz	
			10	1.8	3.6			
			15	2.4	4.8			

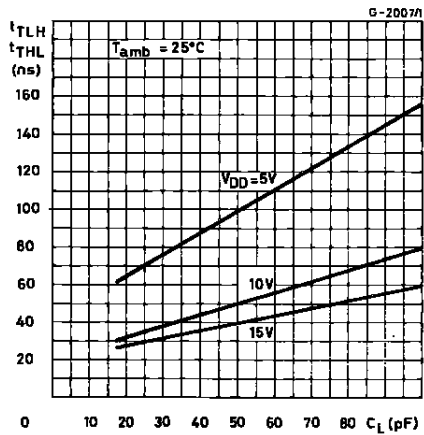
Output Low (sink) Current Characteristics.



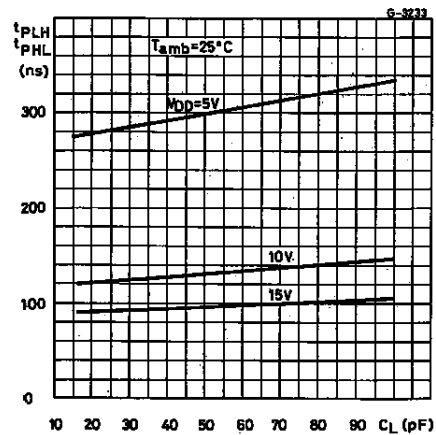
Output High (source) Current Characteristics.



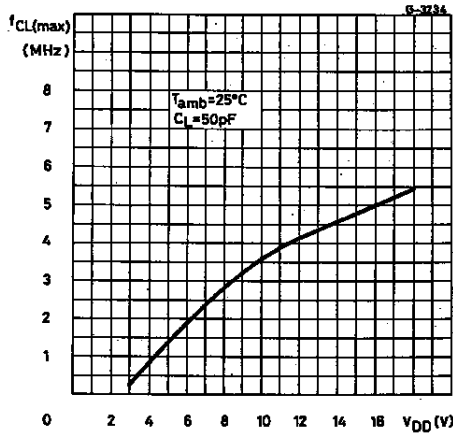
Typical Transition Time vs. Load Capacitance.



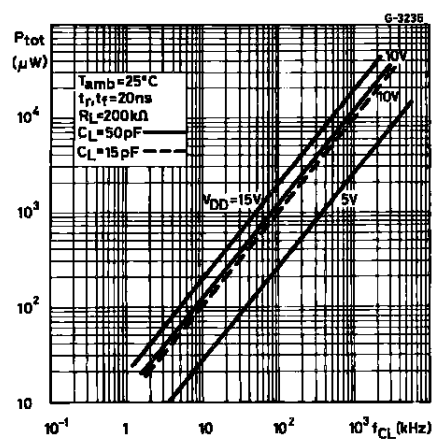
Typical Propagation Delay Time vs. Load Capacitance (clock to CO/ZD).



Typical Maximum Clock Input Frequency vs. Supply Voltage.

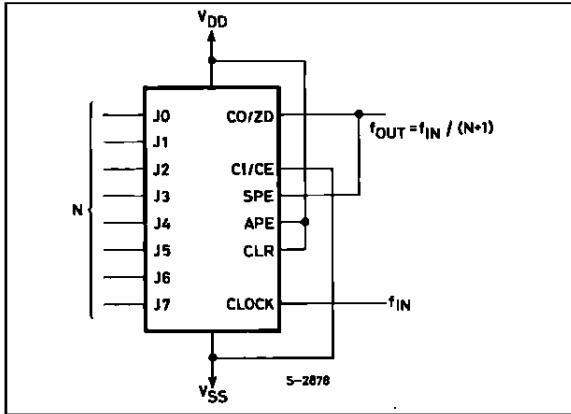


Typical Dynamic Power Dissipation vs. Frequency.

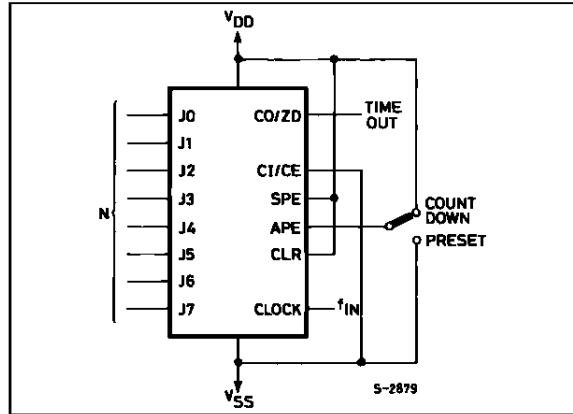


TYPICAL APPLICATIONS

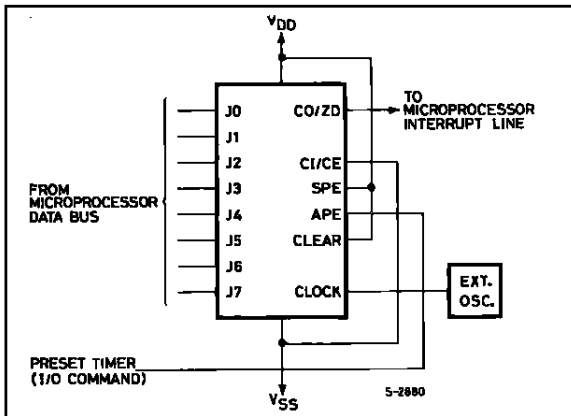
Divide-by-"N" Counter.



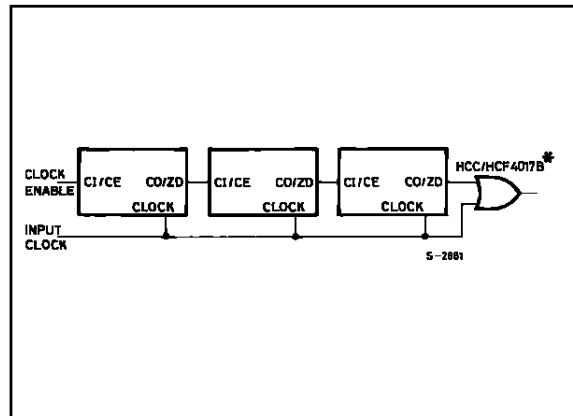
Programmable Timer.



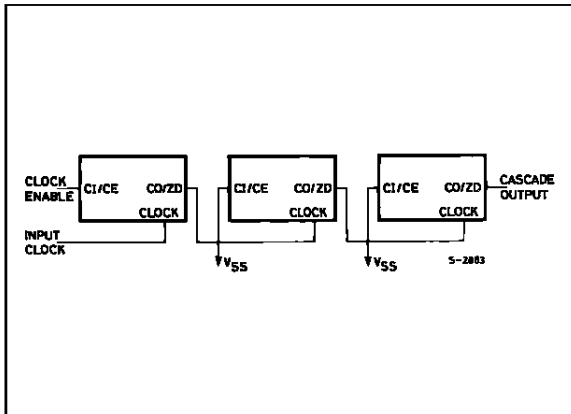
Microprocessor Interrupt Timer.



Synchronous Cascading.



Microprocessor Interrupt Timer.

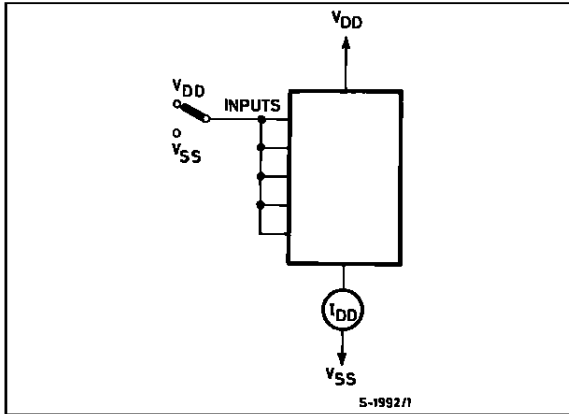


\* An output spike (160ns @ V<sub>DD</sub> = 5V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

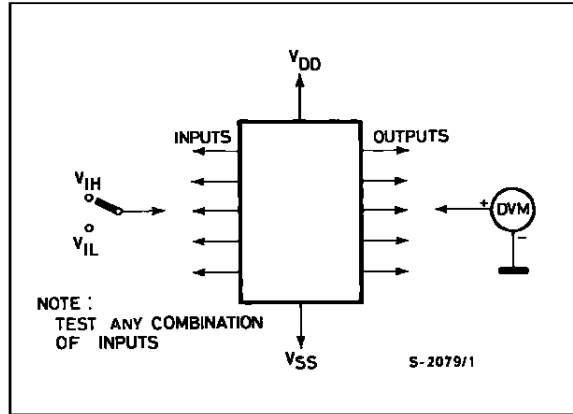


TEST CIRCUITS

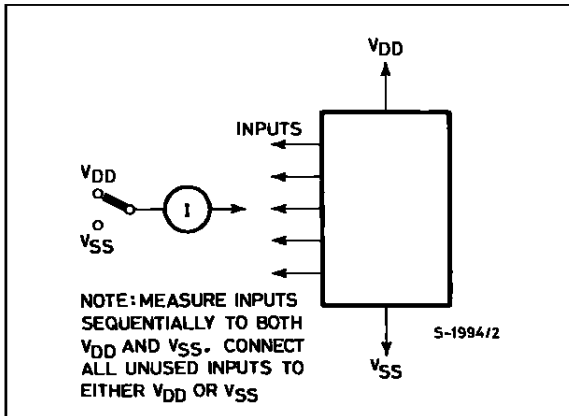
Quiescent Device Current.



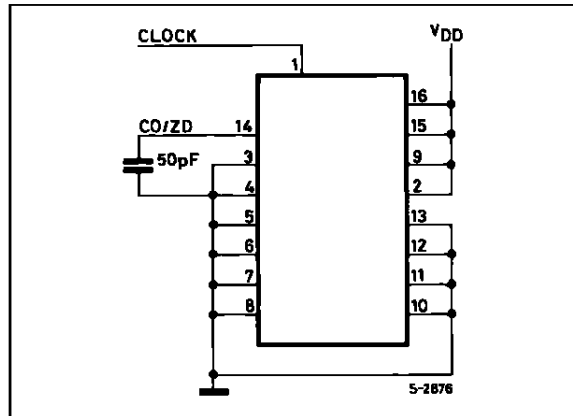
Input Voltage.



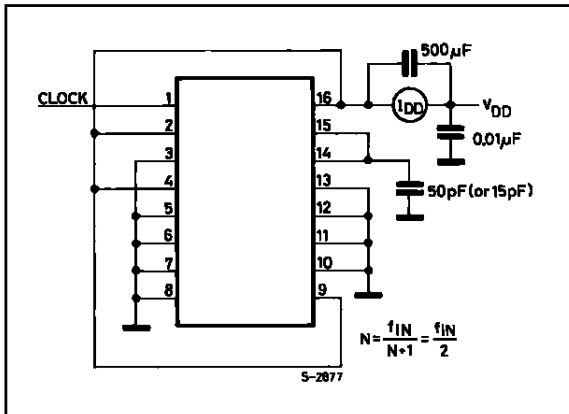
Input Current.



Maximum Clock Frequency.

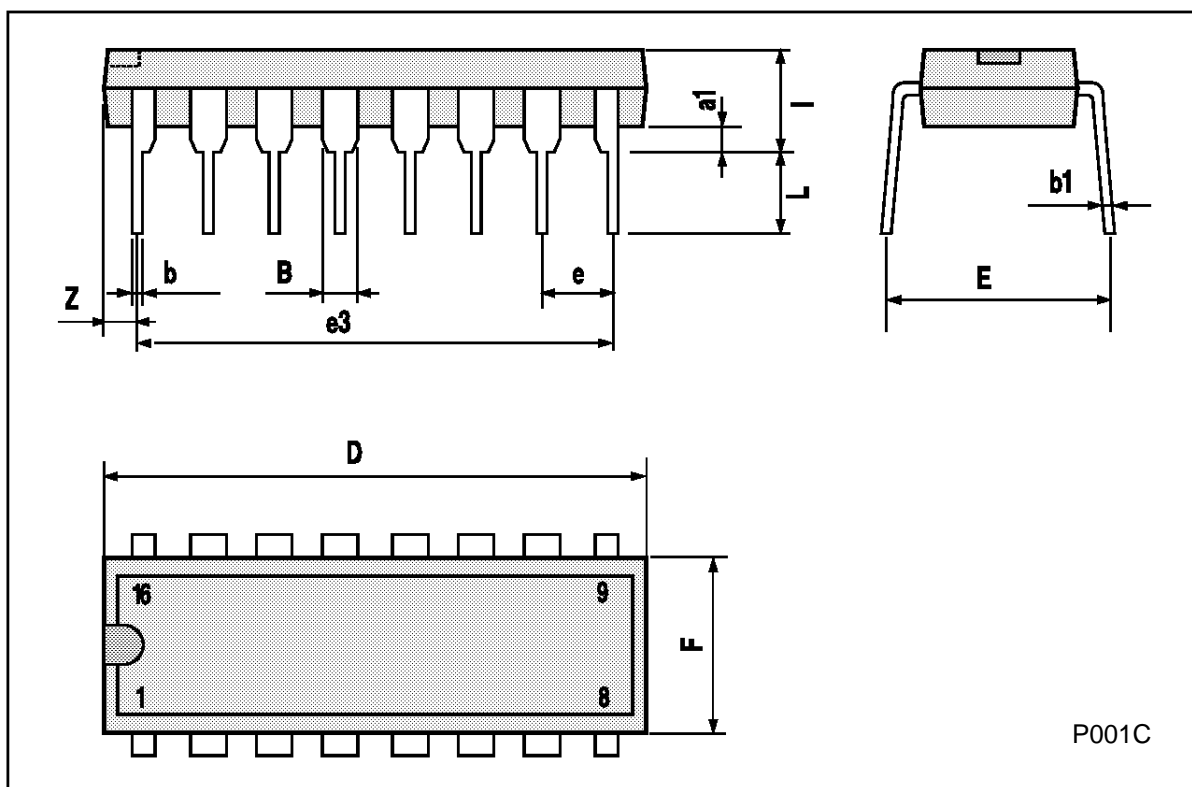


Dynamic Power Dissipation.



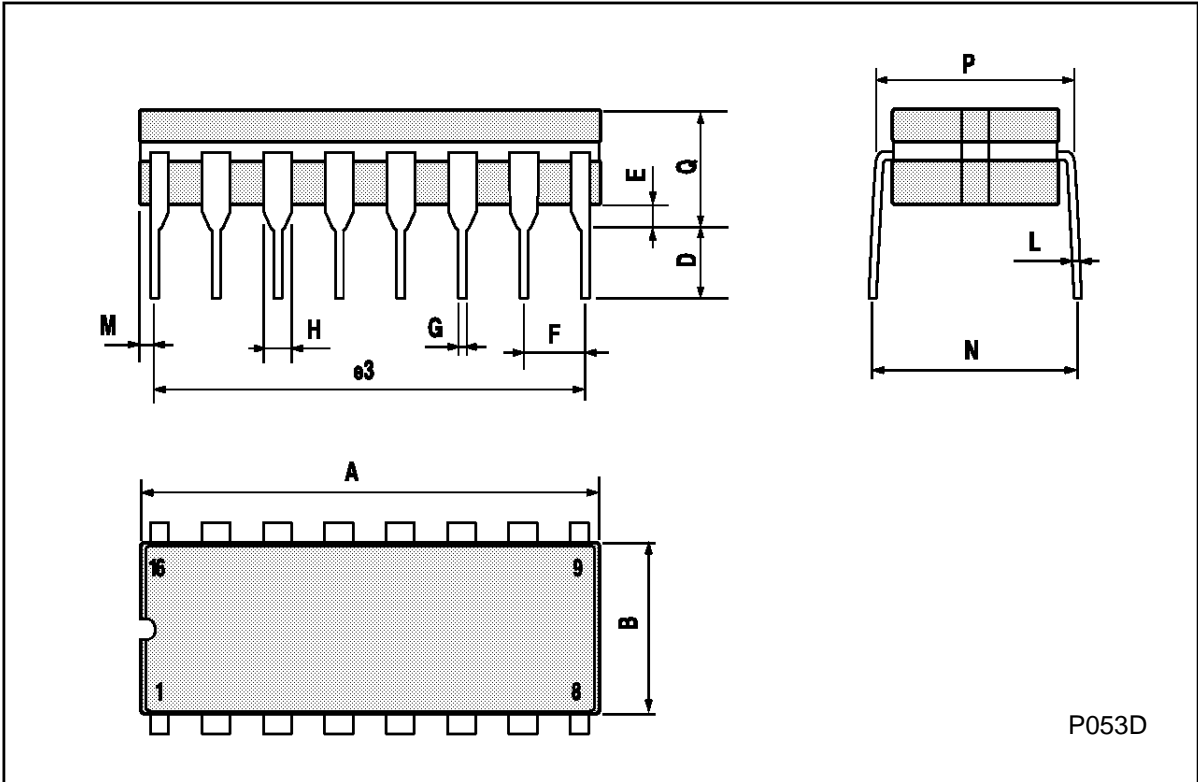
**Plastic DIP16 (0.25) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



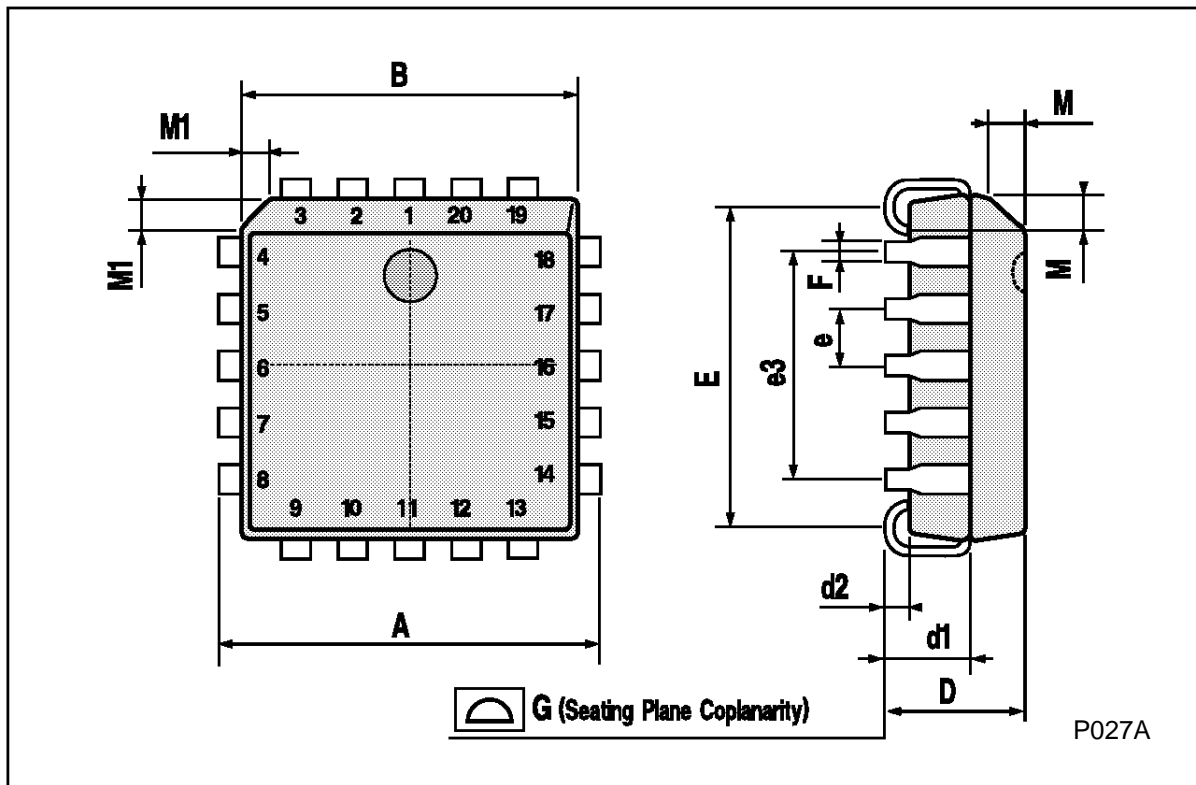
**Ceramic DIP16/1 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



**PLCC20 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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