

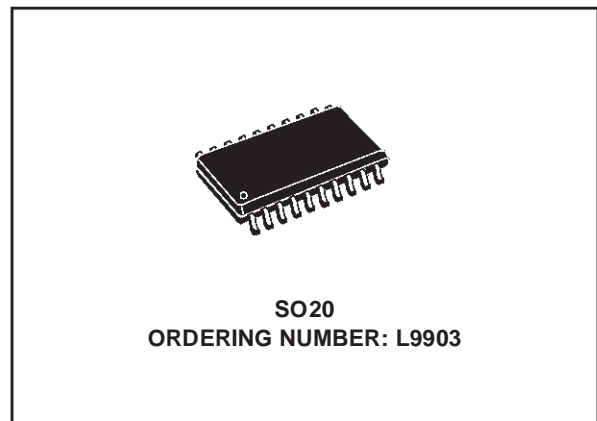


L9903

MOTOR BRIDGE CONTROLLER

PRODUCT PREVIEW

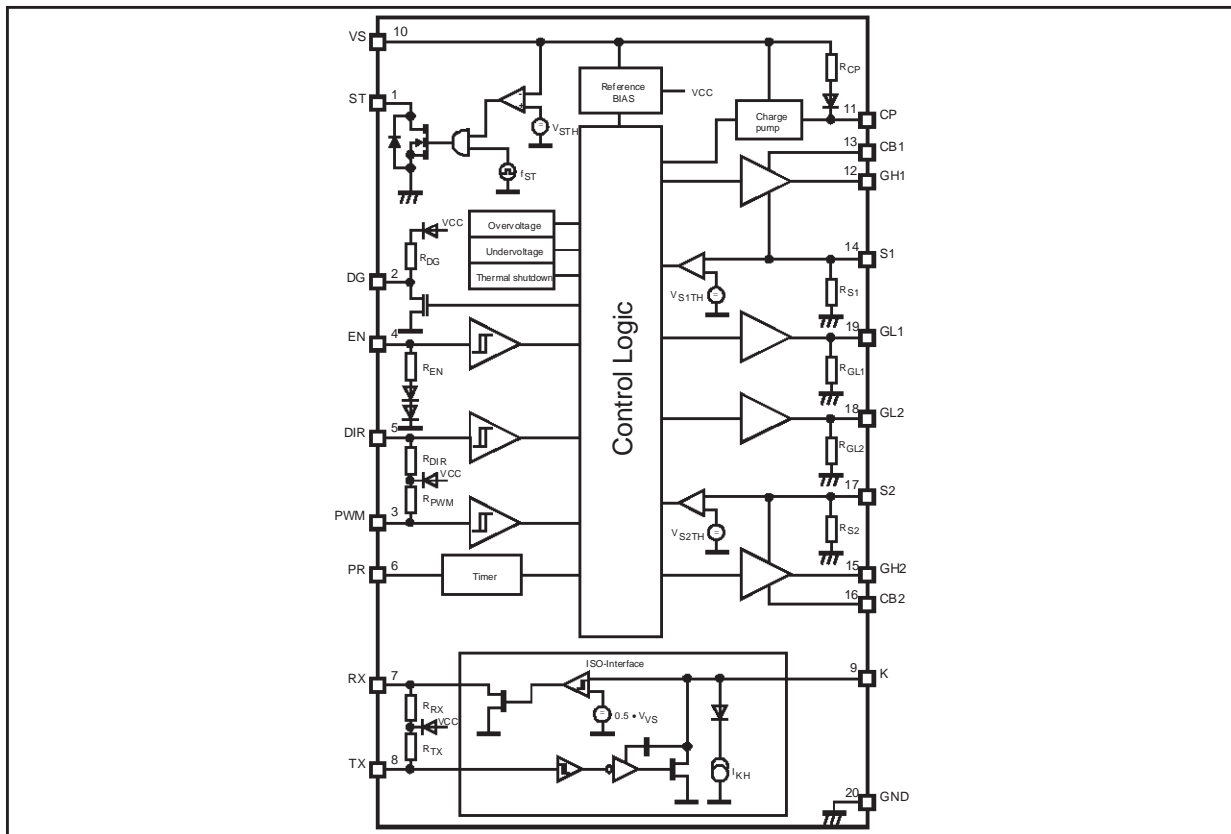
- OPERATING SUPPLY VOLTAGE 8V TO 20V, OVERVOLTAGE MAX. 40V
- OPERATING SUPPLY VOLTAGE 6V WITH IMPLEMENTED STEPUP CONVERTER
- QUIESCENT CURRENT IN STANDBY MODE LESS THAN 50 μ A
- ISO 9141 COMPATIBLE INTERFACE
- CHARGE PUMP FOR DRIVING A POWER MOS AS REVERSE BATTERY PROTECTION
- PWM OPERATION FREQUENCY UP TO 30KHZ
- PROGRAMMABLE CROSS CONDUCTION PROTECTION TIME
- OVERVOLTAGE, UNDERVOLTAGE, SHORT CIRCUIT AND THERMAL PROTECTION
- REAL TIME DIAGNOSTIC



DESCRIPTION

Control circuit for power MOS bridge driver in automotive applications with ISO 9141bus interface.

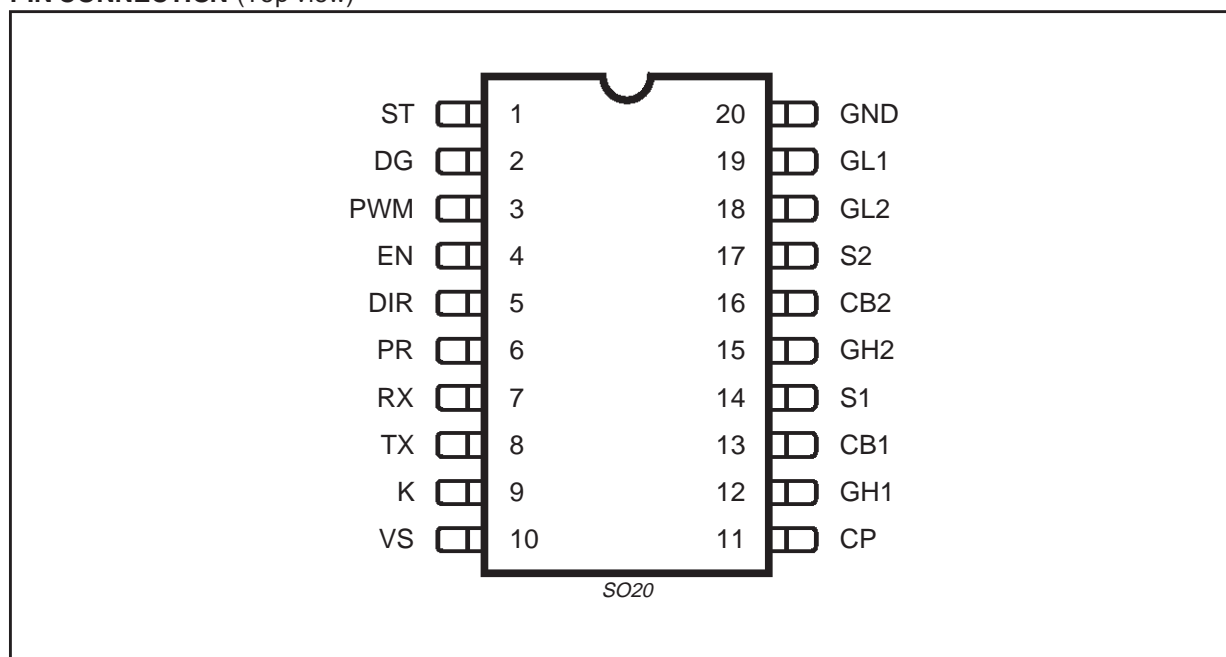
BLOCK DIAGRAM



PIN FUNCTION

| N° | Pin | Description |
|----|-----|---|
| 1 | ST | Open Drain Switch for Stepup converter |
| 2 | DG | Open drain diagnostic output |
| 3 | PWM | PWM input for H-bridge control |
| 4 | EN | Enable input |
| 5 | DIR | Direction select input for H-bridge control |
| 6 | PR | Programmable cross conduction protection time |
| 7 | RX | ISO 9141 interface, receiver output |
| 8 | TX | ISO 9141 interface, transmitter input |
| 9 | K | ISO 9141 Interface, bidirectional communication K-line |
| 10 | VS | Supply voltage |
| 11 | CP | Charge pump for driving a power MOS as reverse battery protection |
| 12 | GH1 | Gate driver for power MOS highside switch in halfbridge 1 |
| 13 | CB1 | External bootstrap capacitor |
| 14 | S1 | Source/drain of halfbridge 1 |
| 15 | GH2 | Gate driver for power MOS highside switch in halfbridge 2 |
| 16 | CB2 | External bootstrap capacitor |
| 17 | S2 | Source/drain of halfbridge 2 |
| 18 | GL2 | Gate driver for power MOS lowside switch in halfbridge 2 |
| 19 | GL1 | Gate driver for power MOS lowside switch in halfbridge 1 |
| 20 | GND | Ground |

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------------------------|---------------------------------------|-----------------------|------|
| V_{CB1}, V_{CB2} | Bootstrap voltage | -0.3 to 40 | V |
| I_{CB1}, I_{CB2} | Bootstrap current | -100 | mA |
| V_{CP} | Charge pump voltage | -0.3 to 40 | V |
| I_{CP} | Charge pump current | -1 | mA |
| $V_{DIR}, V_{EN}, V_{PWM}, V_{TX}$ | Logic input voltage | -0.3 to 7 | V |
| $I_{DIR}, I_{EN}, I_{PWM}, I_{TX}$ | Logic input current | ± 1 | mA |
| V_{DG}, V_{RX} | Logic output voltage | -0.3 to 7 | V |
| I_{DG}, I_{RX} | Logic output current | -1 | mA |
| V_{GH1}, V_{GH2} | Gate driver voltage | -0.3 to $V_{SX} + 10$ | V |
| I_{GH1}, I_{GH2} | Gate driver current | -1 | mA |
| V_{GL1}, V_{GL2} | Gate driver voltage | -0.3 to 10 | V |
| I_{GL1}, I_{GL2} | Gate driver current | -10 | mA |
| V_K | K-line voltage | -20 to V_S | V |
| V_{PR} | Programming input voltage | -0.3 to 7 | V |
| I_{PR} | Programming input current | -1 | mA |
| V_{S1}, V_{S2} | Source/drain voltage | -2 to $V_{VS} + 2$ | V |
| I_{S1}, I_{S2} | Source/drain current | -10 | mA |
| V_{ST} | Output voltage | -0.3 to 40 | V |
| I_{ST} | Step up output current | -1 | mA |
| V_{VSDC} | DC supply voltage | -0.3 to 27 | V |
| V_{VSP} | Pulse supply voltage (T \leq 500ms) | 40 | V |
| I_{VS} | DC supply current | -10 | mA |

For externally applied voltages or currents exceeding these limits damage of the device may occur!

All pins of the IC are protected against ESD. The verification is performed according to MIL883C, human body model with $R=1.5k\Omega$, $C=100pF$ and discharge voltage $\pm 2kV$, corresponding to a maximum discharge energy of 0.2mJ.

THERMAL DATA

| Symbol | Parameter | Value | Unit |
|-----------------------|--|------------|------|
| T _J | Operating junction temperature | -40 to 150 | °C |
| T _{JSD} | Junction temperature thermal shutdown threshold | min 150 | °C |
| T _{JSDH} | Junction thermal shutdown hysteresis | typ 15 | °C |
| R _{th j-amb} | Thermal resistance junction to ambient ¹⁾ | 85 | °C/W |

1. see application note 110 for SO packages.

ELECTRICAL CHARACTERISTICS (8V < V_{VS} < 20V, V_{EN} = HIGH, -40°C ≤ T_J ≤ 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when current flows into the pin.

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|--|------|------|------|------|
| Supply (VS) | | | | | | |
| V _{VS OVH} | Overvoltage disable HIGH threshold | | 20 | 22 | 24 | V |
| V _{VS OVh} | Overvoltage threshold hysteresis ²⁾ | | | 1.6 | | V |
| V _{VS UVH} | Undervoltage disable HIGH threshold | | 6 | | 7 | V |
| V _{VS UVh} | Undervoltage threshold hysteresis ²⁾ | | | 0.66 | | V |
| I _{VSL} | Supply current | V _{EN} = 0 ; V _{VS} = 13.5V; T _J < 85°C | | | 50 | μA |
| I _{VSH} | Supply current | V _{VS} = 13.5V; V _{EN} = HIGH; V _{DIR} = LOW; f _{PWM} = 20kHz; C _{CBX} = 0.1μF; C _{GLX} = 4.7nF; C _{GHX} = 4.7nF; R _{PR} = 10kΩ; C _{PR} = 150pF | | | 20 | mA |
| Enable input (EN) | | | | | | |
| V _{ENL} | Low level | | | | 1.5 | V |
| V _{ENH} | High level | | 3.5 | | | V |
| V _{ENh} | Hysteresis threshold ²⁾ | | | 1 | | V |
| R _{EN} | Input pull down resistance | V _{EN} = 5V | 16 | 50 | 100 | kΩ |
| H-bridge control inputs (DIR, PWM) | | | | | | |
| V _{DIRL} V _{PWML} | Input low level | | | | 1.5 | V |
| V _{DIRH} V _{PWMH} | Input high level | | 3.5 | | | V |
| V _{DIRh} V _{PWMh} | Input threshold hysteresis ²⁾ | | | 1 | | V |
| R _{DIR} R _{PWM} | Internal pull up resistance to internal VCC ³⁾ | V _{DIR} = 0; V _{PWM} = 0 | 16 | 50 | 100 | kΩ |

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--|--|--|------------------------|-------------------------|------------------------|------|
| DIAGNOSTIC output (DG) | | | | | | |
| V _{DG} | Output drop | I _{DG} = 1mA | | | 0.6 | V |
| R _{DG} | Internal pull up resistance to internal VCC ³⁾ | V _{DG} = 0V | 10 | 20 | 40 | kΩ |
| Programmable cross conduction protection⁴⁾ | | | | | | |
| N _{PR} | Threshold voltage ratio V _{PRH} /V _{PRL} | R _{PR} = 10kΩ | 1.8 | 2 | 2.2 | |
| I _{PR} | Current capability | V _{PR} = 2V | -0.5 | | | mA |
| ISO interface, transmission input (TX) | | | | | | |
| V _{TXL} | Input low level | | | | 1.5 | V |
| V _{TXH} | Input high level | | 3.5 | | | V |
| V _{TXh} | Input hysteresis voltage 2) | | | 1 | | V |
| R _{TX} | Internal pull up resistance to internal VCC ³⁾ | V _{TX} = 0 | 10 | 20 | 40 | kΩ |
| ISO interface, receiver output (RX) | | | | | | |
| V _{RXL} | Output voltage high stage | TX = HIGH; I _{RX} = 0; V _K = V _{VS} | 4.5 | | 5.5 | V |
| R _{RX} | Internal pull up resistance to internal VCC ³⁾ | TX = HIGH; V _{RX} = 0V | 5 | 10 | 20 | kΩ |
| R _{RXON} | ON resistance to ground | TX = LOW; I _{RX} = 1mA | | 40 | 90 | W |
| t _{RXH} | Output high delay time | Fig. 1 | | 0.5 | | μs |
| t _{RXL} | Output low delay time | | | 0.5 | | μs |
| ISO interface, K-line (K) | | | | | | |
| V _{KL} | Input low level | | -20V | | 0.45 · V _{VS} | |
| V _{KH} | Input high level | | 0.55 · V _{VS} | | V _{VS} | |
| V _{Kh} | Input hysteresis voltage 2) | | | 0.025 · V _{VS} | 0.8V | |
| I _{KH} | Input current | V _{TX} = HIGH | -5 | | 25 | μA |
| R _{KON} | ON resistance to ground | V _{TX} = LOW; I _K = 10mA | | 10 | 30 | W |
| I _{KSC} | Short circuit current | V _{TX} = LOW | 40 | | 130 | mA |
| f _K | Transmission frequency | | 60 | 100 | | kHz |

2. not tested in production: guaranteed by design and verified in characterization

3. Internal V_{VCC} is 4.5V ... 5.5V

4. see page 18 for calculation of programmable cross conduction protection time

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--|---|--|---|------|--|-------------|
| t_{kr} | Rise time | $V_{VS} = 13.5V$; Fig. 1 External loads at K-line: $R_K = 510\Omega$ pull up to V_{VS} $C_K = 2.2nF$ to GND | | 2 | 6 | μs |
| t_{kf} | Fall time | | | 2 | 6 | μs |
| t_{KH} | Switch high delay time | | | 4 | 17 | μs |
| t_{KL} | Switch low delay time | | | 4 | 17 | μs |
| t_{SH} | Short circuit detection time | $V_{VS} = 13.5V$; TX = LOW $V_K > 0.55 \cdot V_{VS}$ | 10 | | 40 | μs |
| Charge pump | | | | | | |
| V_{CP} | Charge pump voltage | $V_{VS} = 8V$ $V_{VS} = 13.5V$ $V_{VS} = 20V$ | $V_{VS} + 7V$ $V_{VS} + 10V$ $V_{VS} + 10V$ | | $V_{VS} + 14V$ $V_{VS} + 14V$ $V_{VS} + 14V$ | |
| I_{CP} | Charging current $V_{CP} = V_{VS} + 8V$ | $V_{VS} = 13.5V$ | -50 | -75 | | μA |
| t_{CP} | Charging time ²⁾ $V_{CP} = V_{VS} + 8V$ | $V_{VS} = 13.5V$ $C_{CP} = 10nF$ | | 1.2 | 4 | ms |
| f_{CP} | Charge pump frequency | $V_{VS} = 13.5V$ | 250 | 500 | 750 | kHz |
| Drivers for external highside power MOS | | | | | | |
| V_{CB1} V_{CB2} | Bootstrap voltage | $V_{VS} = 8V$; $I_{CBX} = 0$; $V_{SX} = 0$ $V_{VS} = 13.5V$; $I_{CBX} = 0$; $V_{SX} = 0$ $V_{VS} = 20V$; $I_{CBX} = 0$; $V_{SX} = 0$ | 7.5 10 10 | | 14 14 14 | V V V |
| R_{GH1L} R_{GH2L} | ON-resistance of SINK stage | $V_{CBX} = 8V$; $V_{SX} = 0$ $I_{GHX} = 50mA$; $T_J = 25^\circ C$ | | | 10 | W |
| | | $V_{CBX} = 8V$; $V_{SX} = 0$ $I_{GHX} = 50mA$; $T_J = 125^\circ C$ | | | 20 | W |
| R_{GH1H} R_{GH2H} | ON-resistance of SOURCE stage | $I_{GHX} = -50mA$; $T_J = 25^\circ C$ $I_{GHX} = -50mA$; $T_J = 125^\circ C$ | | | 10 20 | W W |
| V_{GH1H} V_{GH2H} | Gate ON voltage (SOURCE) | $V_{VS} = V_{SX} = 8V$; $I_{GHX} = 0$; $C_{CBX} = 0.1\mu F$ | $V_{VS} + 6.5V$ | | $V_{VS} + 14V$ | |
| | | $V_{VS} = V_{SX} = 13.5V$; $I_{GHX} = 0$; $C_{CBX} = 0.1\mu F$ | $V_{VS} + 10V$ | | $V_{VS} + 14V$ | |
| | | $V_{VS} = V_{SX} = 20V$; $I_{GHX} = 0$; $C_{CBX} = 0.1\mu F$ | $V_{VS} + 10V$ | | $V_{VS} + 14V$ | |

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|-------------------------------|--|------------------|------|---|--------|
| R _{GH1} R _{GH2} | Gate discharge resistance | EN = LOW | 10 | 100 | | kΩ |
| R _{S1} R _{S2} | Sink resistance | | 10 | 100 | | kΩ |
| Drivers for external lowside power MOS | | | | | | |
| R _{GL1L} R _{GL2L} | ON-resistance of SINK stage | I _{GLX} = 50mA; T _J = 25°C I _{GLX} = 50mA; T _J = 125°C | | | 10 20 | W W |
| R _{GL1H} , R _{GL2H} | ON-resistance of SOURCE stage | I _{GLX} = -50mA; T _J = 25°C I _{GLX} = -50mA; T _J = 125°C | | | 10 20 | W W |
| V _{GL1H} , V _{GL2H} | Gate ON voltage (SOURCE) | V _{VS} = 8V; I _{GLX} = 0 V _{VS} = 13.5V; I _{GLX} = 0 V _{VS} = 20V; I _{GLX} = 0 | 7V 10V 10V | | V _{VS} V _{VS} 14V | |
| R _{GL1} R _{GL2} | Gate discharge resistance | EN = LOW | 10 | 100 | | kΩ |

2. not tested in production: guaranteed by design and verified in characterization

| Timing of the drivers | | | | | | |
|--|--|--|-----|---|-----|----|
| t _{GH1LH} t _{GH2LH} | Propagation delay time | Fig. 2 V _{VS} = 13.5V V _{S1} = V _{S2} = 0 C _{CBX} = 0.1μF R _{PR} = 10kΩ | | | 500 | ns |
| t _{GH1LH} t _{GH2LH} | Propagation delay time including cross conduction protection time t _{CCP} | Fig. 2 V _{VS} = 13.5V V _{S1} = V _{S2} = 0 C _{CBX} = 0.1μF | 0.7 | 1 | 1.3 | μs |
| t _{GH1HL} t _{GH2HL} | Propagation delay time | C _{PR} = 150pF; R _{PR} = 10kΩ; 5) | | | 500 | ns |
| t _{GL1LH} t _{GL2LH} | Propagation delay time | Fig. 2 V _{VS} = 13.5V V _{S1} = V _{S2} = 0 C _{CBX} = 0.1μF R _{PR} = 10kΩ | | | 500 | ns |
| t _{GL1LH} t _{GL2LH} | Propagation delay time including cross conduction protection time t _{CCP} | Fig. 2 V _{VS} = 13.5V V _{S1} = V _{S2} = 0 C _{CBX} = 0.1μF | 0.7 | 1 | 1.3 | μs |
| t _{GL1HL} t _{GL2HL} | Propagation delay time | C _{PR} = 150pF; R _{PR} = 10kΩ; 5) | | | 500 | ns |

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--|---|---|------|------|------|------|
| t _{GH1r} t _{GH2r} | Rise time | Fig. 2 V _{VS} = 13.5V V _{S1} = V _{S2} = 0 C _{CBX} = 0.1μF C _{GHX} = 4.7nF C _{GLX} = 4.7nF R _{PR} = 10kΩ; | | | 1 | μs |
| t _{GH1f} t _{GH2f} | Fall time | | | | 1 | μs |
| t _{GL1r} t _{GL2r} | Rise time | | | | 1 | μs |
| t _{GL1f} t _{GL2f} | Fall time | | | | 1 | μs |
| Short Circuit Detection | | | | | | |
| V _{S1TH} V _{S2TH} | Threshold voltage | | | 4 | | V |
| t _{SCd} | Detection time | | 5 | 10 | 15 | μs |
| Step up converter (ST) (5.2V ≤ V_{VS} < 10V) | | | | | | |
| V _{STH} | ST disable HIGH threshold | | | | 10 | V |
| V _{STh} | ST disable threshold hysteresis voltage ²⁾ | | 1 | | 2 | V |
| R _{DSON} | Open drain ON resistance | V _{VS} = 5.2V; I _{ST} = 50mA | | | 20 | Ω |
| f _{ST} | Clock frequency | | 50 | 100 | 149 | kHz |

2. not tested in production: guaranteed by design and verified in characterization

5. tested with differed values in production but guaranteed by design and verified in characterization

Figure 1. Timing of the ISO-interface

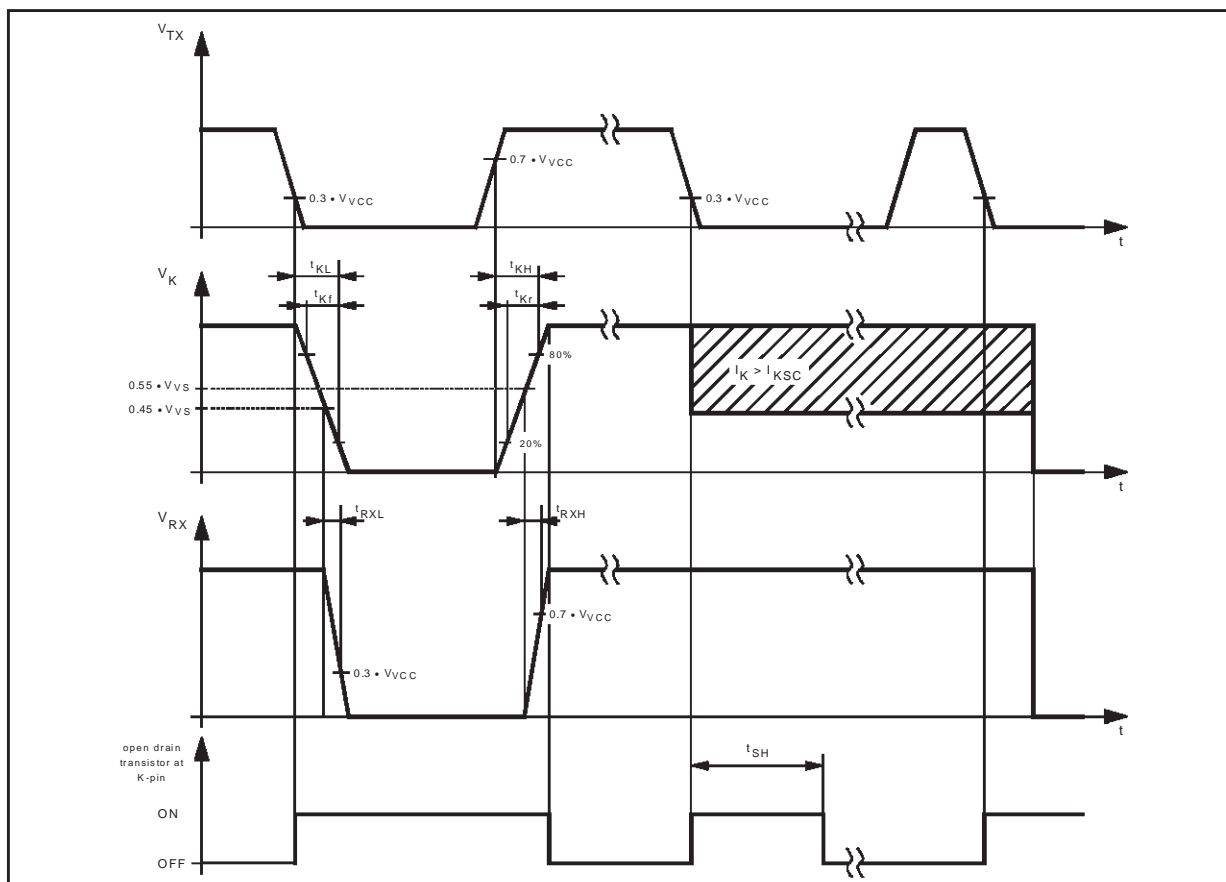


Figure 2. Timing of the drivers for the external MOS regarding the inputs DIR and PWM

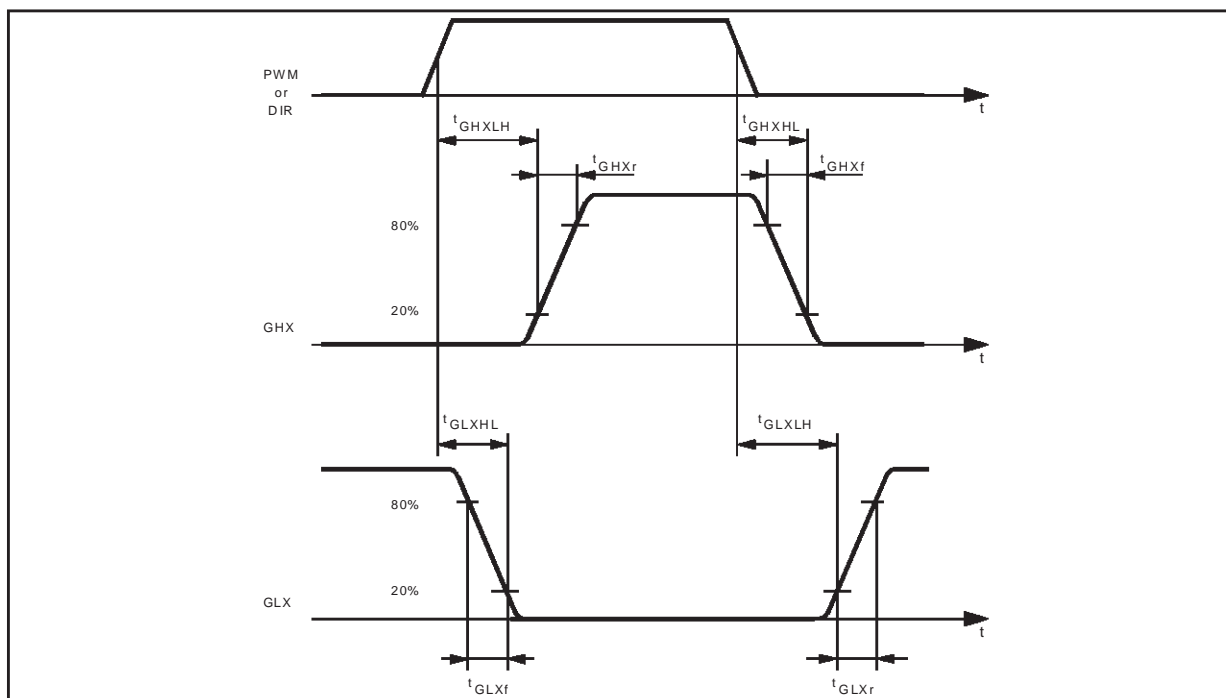


Figure 3. I(V) characteristics of the K-Line for TX = HIGH and VVS=13.5V

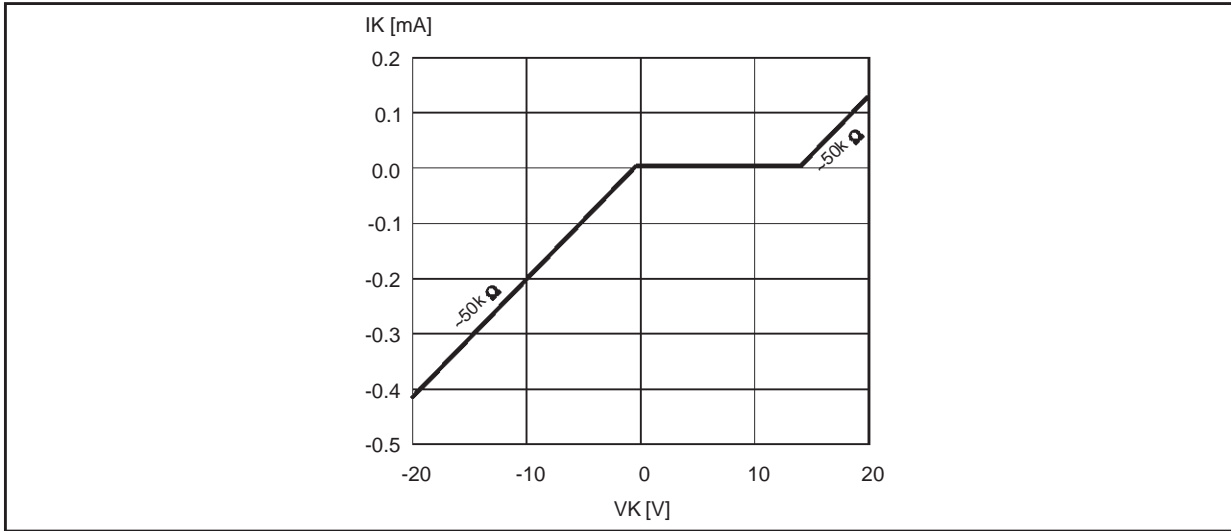


Figure 4. Driving sequence

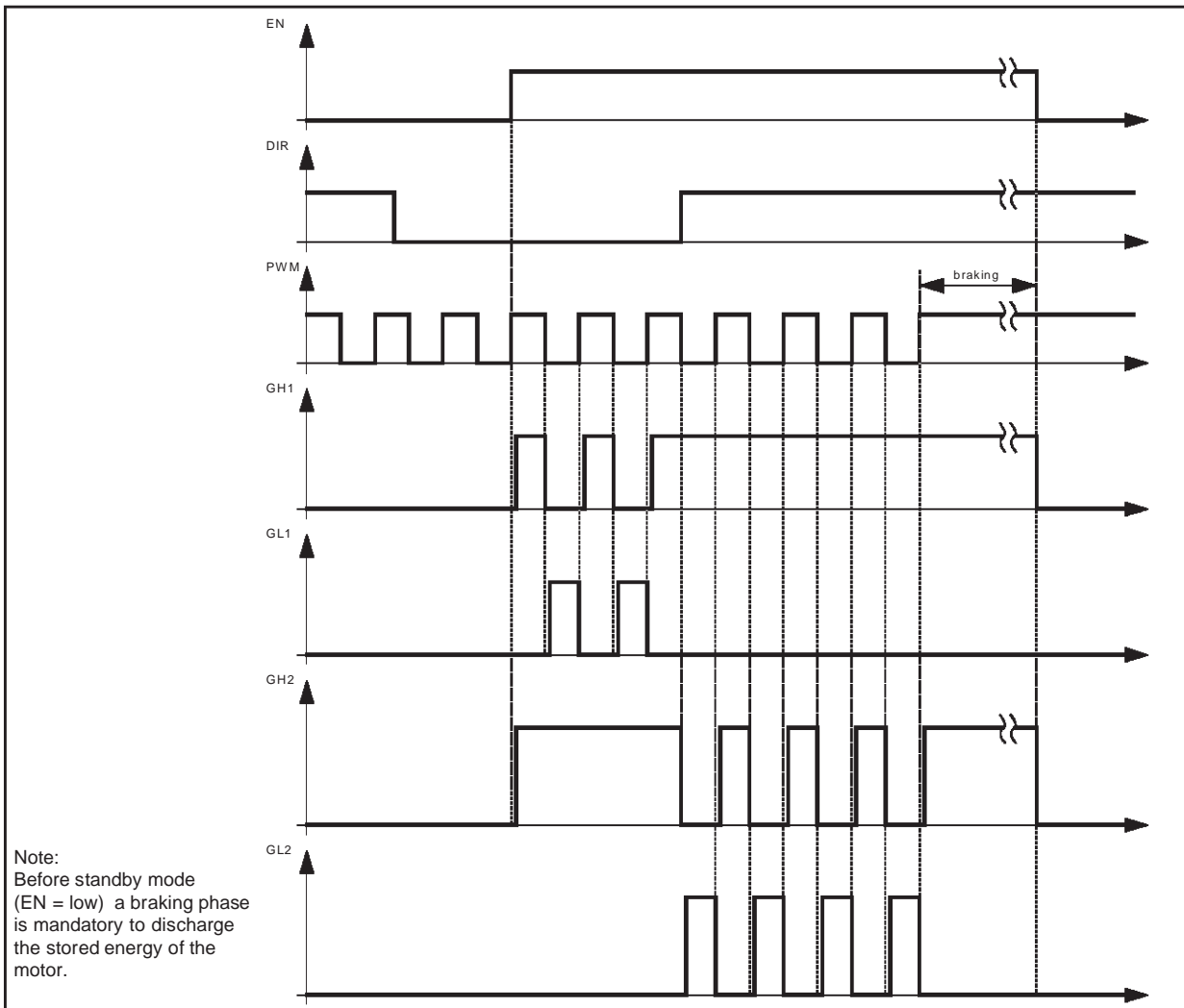


Figure 5. Charging time of an external capacitor of 10nF connected to CP pin at $V_S=8V$ and $V_{VS}=13.5V$

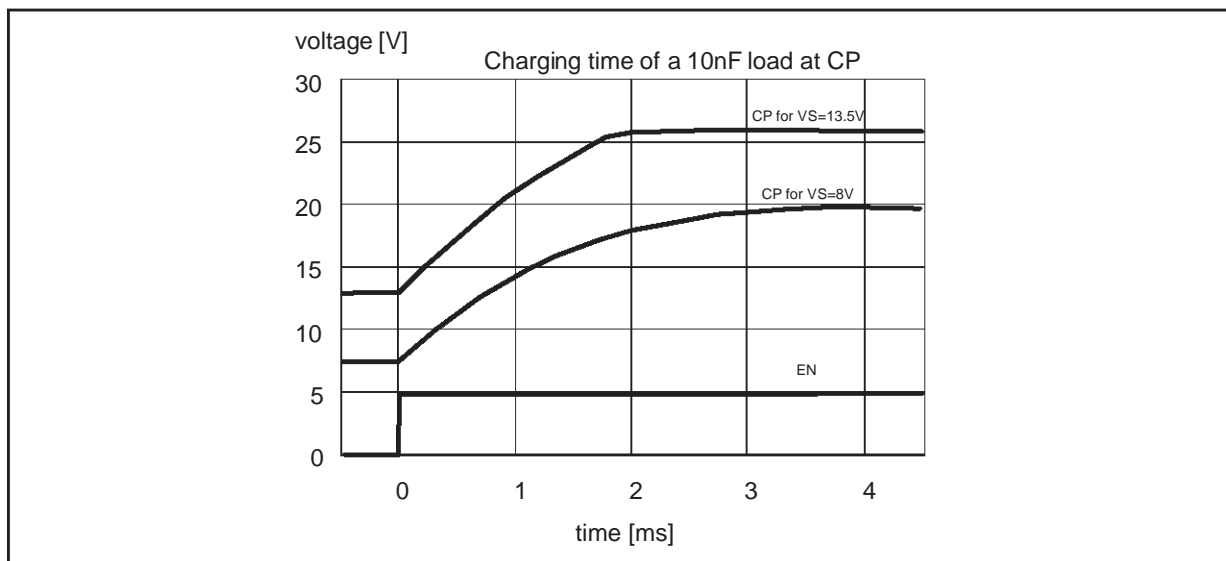
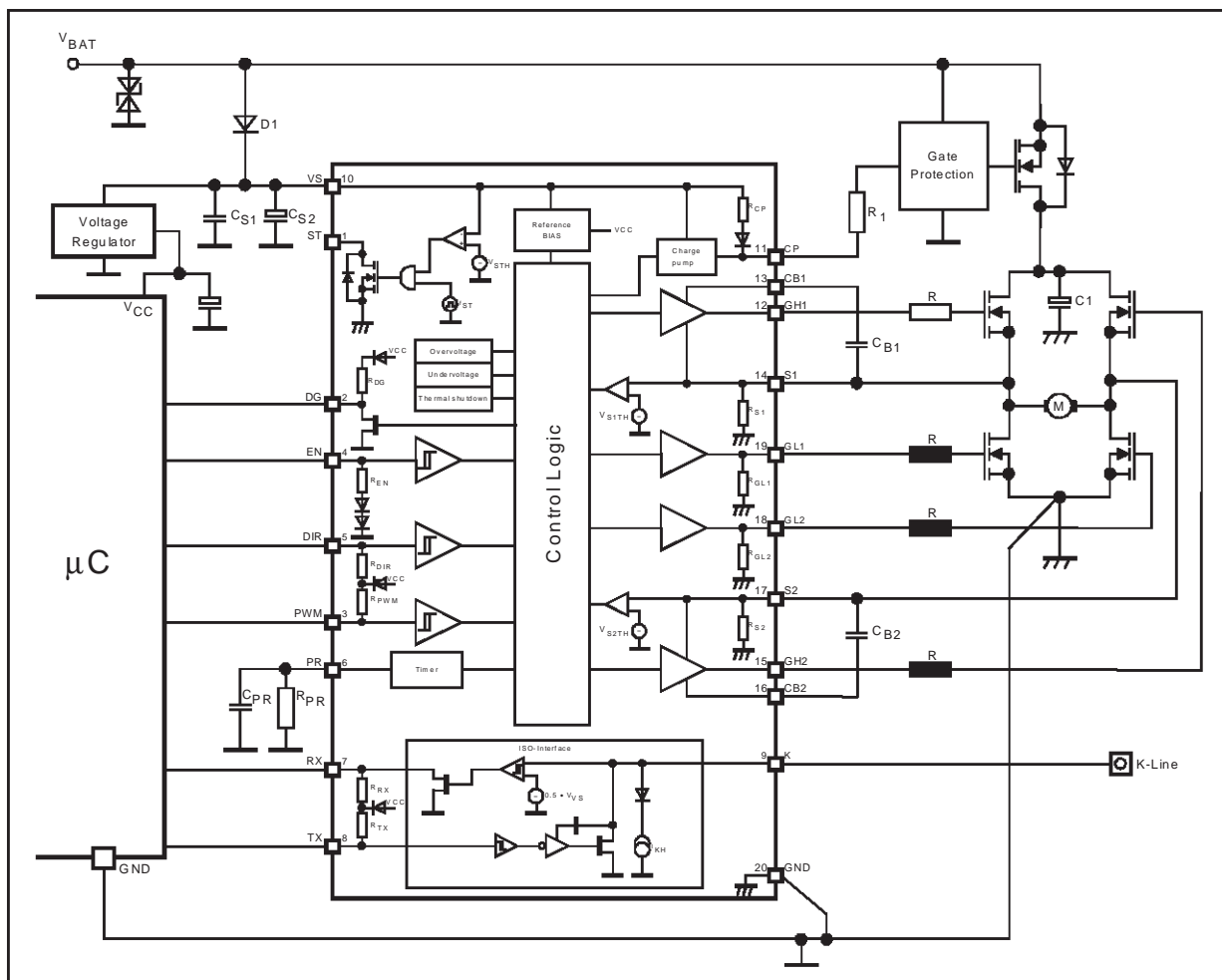


Figure 6. Application Circuit Diagram



FUNCTIONAL DESCRIPTION

General

The L9903 integrated circuit (IC) is designed to control four external N-channel MOS transistors in H-Bridge configuration for DC-motor driving in automotive applications. It includes an ISO9141 compatible interface. A typical application is shown in fig.6.

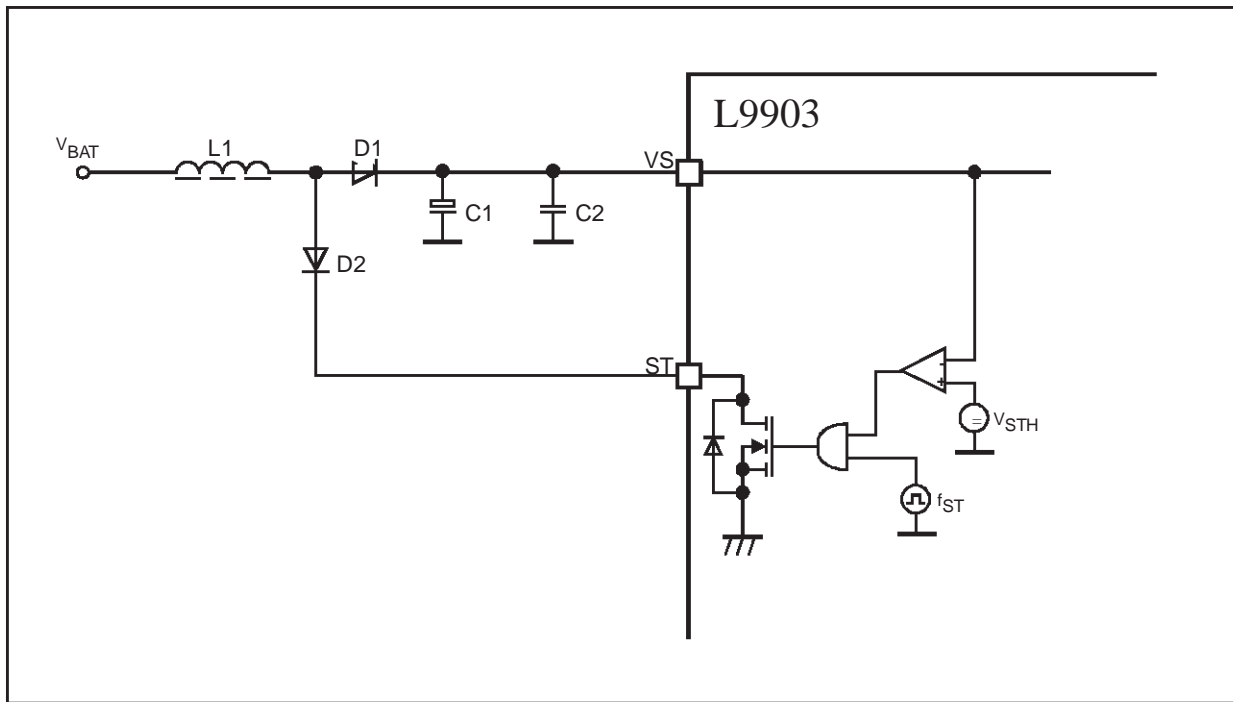
Voltage supply

The IC is supplied via an external reverse battery protection diode to the V_{VS} pin. The typical operating voltage range is down to 8V.

Extended supply voltage range (ST)

The operating battery voltage range can be extended down to 6V using the additional components shown in fig.7. A small inductor of $L \sim 150\mu\text{H}$ ($I_{\text{peak}} \sim 500\text{mA}$) in series to the battery supply builds up a step up converter with the switching open drain output ST. The switching frequency is typical 100kHz with a fixed duty cycle of 50%. The step up converter starts below $V_{VS} < 8\text{V}$, increases the supply voltage at the VS pin and switches off at $V_{VS} > 10\text{V}$ to avoid EME at nominal battery voltage. The diode D2 in series with the ST pin is necessary only for systems with negative battery voltage. No additional load can be driven by the step up converter.

Figure 7.



FUNCTIONAL DESCRIPTION (continued)**Control inputs (EN, DIR, PWM)**

The cmos level inputs drive the device as shown in fig.4 and described in the truth table.

The device is activated with enable input HIGH signal. For enable input floating (not connected) or VEN=0V the device is in standby mode. When activating the device a wake-up time of 50µs is recommended to stabilize the internal supplies.

The DIR and PWM inputs control the driver of the external H-Bridge transistors. The motor direction can be chosen with the DIR input, the duty cycle and frequency with the PWM input. Unconnected inputs are defined by internal pull up resistors. During wake-up and braking and before deactivating the IC via enable both inputs should be driven HIGH.

Truth table:

| Status | Control inputs | | | Device status | | | | Driver stage for external power MOS | | | | Diagnostic | Comment |
|--------|----------------|-----|-----|---------------|----|----|----|-------------------------------------|-----------------|-----------------|-----------------|------------|-----------------------------|
| | EN | DIR | PWM | TS | OV | UV | SC | GH1 | GL1 | GH2 | GL2 | | |
| 1 | 0 | x | x | x | x | x | x | R | R | R | R | T | standby mode |
| 2 | 1 | x | x | 1 | 0 | 0 | 0 | L | L | L | L | L | thermal shutdown |
| 3 | 1 | x | x | 0 | 1 | 0 | 0 | L | L | L | L | L | overvoltage |
| 4 | 1 | x | x | 0 | 0 | 1 | 0 | L | L | L | L | L | undervoltage |
| 5 | 1 | x | x | 0 | 0 | 0 | 1 | X ⁶⁾ | X ⁶⁾ | X ⁶⁾ | X ⁶⁾ | L | short circuit ⁶⁾ |
| 6 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | L | H | H | L | H | |
| 7 | 1 | x | 1 | 0 | 0 | 0 | 0 | H | L | H | L | H | braking mode |
| 8 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | H | L | L | H | H | |

Symbols: x Don't care

0: Logic LOW or not active

1: Logic HIGH or active

R:Resistive output

L: Output in sink condition

H: Output in source condition

T: Tristate

TS:Thermal shutdown

OV:Overvoltage

UV:Undervoltage

SC:Short Circuit

6. Only those external MOS transistors of the H-Bridge which are in short circuit condition are switched off. All others remain driven by DIR and PWM.

Thermal shutdown

When the junction temperature exceeds T_{JSD} all driver are switched in sink condition (L), the K- output is off and the diagnostic DG is LOW until the junction temperature drops below $T_{JSD} - T_{JHYST}$.

Overvoltage Shutdown

When the supply voltage V_{VS} exceeds the overvoltage threshold V_{VSOVH} all driver are switched in sink condition (L), the K- output is off and the diagnostic DG is LOW.

FUNCTIONAL DESCRIPTION (continued)**Undervoltage Shutdown**

For supply voltages below the undervoltage disable threshold the gate driver remains in sink condition (L) and the diagnostic DG is low.

Short Circuit Detection

The output voltage at the S1 and S2 pin of the H-Bridge is monitored by comparators to detect shorts to ground or battery. The activated external highside MOS transistor will be switched off if the voltage drop remains below the comparator threshold voltage V_{S1TH} and V_{S2TH} for longer than the short current detection time t_{SCd} . The transistor remains in off condition, the diagnostic output goes LOW until the DIR or PWM input status will be changed. The status doesn't change for the other MOS transistors. The external lowside MOS transistor will be switched off if the voltage drop passes over the comparator threshold voltage V_{S1TH} and V_{S2TH} for longer than the short current detection time t_{SCd} . The transistor remains in off condition, the diagnostic output goes LOW until the DIR or PWM input status will be changed. The status doesn't change for the other MOS transistors.

Diagnostic Output (DG)

The diagnostic output provides a real time error detection, if monitors the following error stacks: Thermal shutdown, overvoltage shutdown, undervoltage shutdown and short circuit shutdown. The open drain output with internal pull up resistor is LOW if an error is occurring.

Bootstrap capacitor (CB1,CB2)

To ensure, that the external power MOS transistors reach the required $R_{DS(ON)}$, a minimum gate source voltage of 5V for logic level and 10V for standard power MOS transistors has to be guaranteed. The highside transistors require a gate voltage higher than the supply voltage. This is achieved with the internal chargepump circuit in combination with the bootstrap capacitor. The bootstrap capacitor is charged, when the highside MOS transistor is OFF and the lowside is ON. When the lowside is switched OFF, the charged bootstrap capacitor is able to supply the gate driver of the highside power MOS transistor. For effective charging the values of the bootstrap capacitors should be larger than the gate-source capacitance of the power MOS and respect the required PWM ratio.

Chargepump circuit (CP)

The reverse battery protection can be obtained with an external N-channel MOS transistor as shown in fig.6. In this case its drain-bulk diode provides the protection. The output CP is intended to drive the gate of this transistor above the battery voltage to switch on the MOS and to bypass the drain-bulk diode with the $R_{DS(ON)}$. The CP has a connection to VS through an internal diode and a 20k Ω resistor.

Gate drivers for the external N-channel power MOS transistors (GH1, GH2, GL1, GL2)

High level at EN activates the driver of the external MOS under control of the DIR and PWM inputs (see truth table and driving sequence fig.4). The external power MOS gates are connected via series resistors to the device to reduce electro magnetic emission (EME) of the system. The resistors influence the switching behaviour. They have to be chosen carefully. Too large resistors enlarge the charging and discharging time of the power MOS gate and can generate cross current in the halfbridges. The driver assures a longer switching delay time from source to sink stage in order to prevent the cross conduction.

The gate source voltage is limited to 14V. The charge/discharge current is limited by the $R_{DS(ON)}$ of the driver. The drivers are not protected against shorts.

FUNCTIONAL DESCRIPTION (continued)**Programmable cross conduction protection**

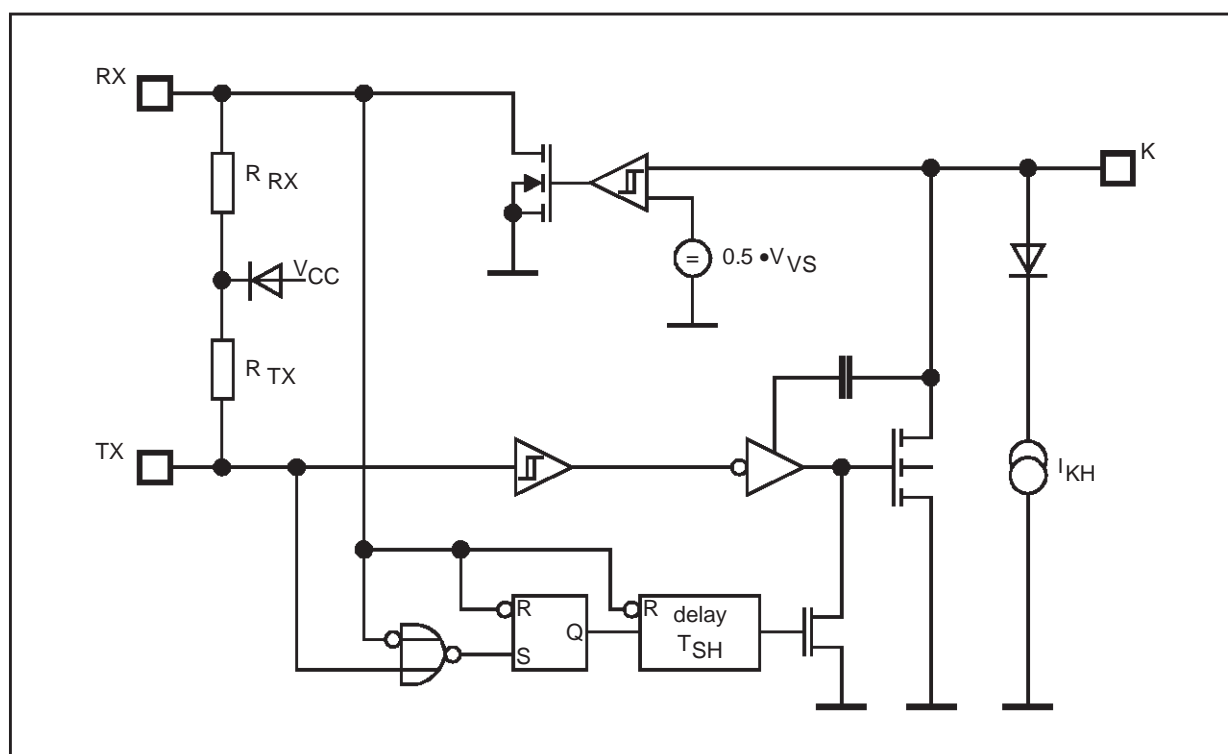
The external power MOS transistors in H-Bridge (two half bridges) configuration are switched on with an additional delay time t_{CCP} to prevent cross conduction in the halfbridge. The cross conduction protection time t_{CCP} is determined by the external capacitor C_{PR} and resistor R_{PR} at the PR pin. The capacitor C_{PR} is charged up to the voltage limit V_{PRH} . A level change on the control inputs DIR and PWM switches off the concerned external MOS transistor and the charging source at the PR pin. The resistor R_{PR} discharges the capacitor C_{PR} . The concerned external power MOS transistor will be switched on again when the voltage at PR reaches the value of V_{PRL} . After that the CPR will be charged again. The capacitor C_{PR} should be chosen between 100pF and 1nF. The resistor R_{PR} should be higher than 7kΩ. The delay time can be expressed as follows:

$$t_{CCP} = R_{PR} \cdot C_{PR} \cdot \ln N_{PR} \quad \text{with } N_{PR} = V_{PRH} / V_{PRL} = 2$$

$$t_{CCP} = 0.69 \cdot R_{PR} \cdot C_{PR}$$

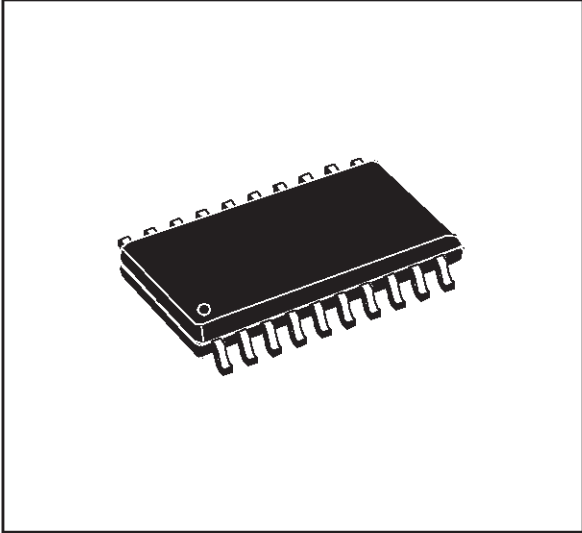
ISO-Interface

The ISO-Interface provides the communication between the micro controller and a serial bus with a baud rate up to 60kbit/s via a single wire which is V_{BAT} and GND compatible. The logic level transmission input TX drives the open drain K-output. The K output can be connected to a serial bus with a pull up resistor to V_{BAT} . The K-pin is protected against overvoltage, short to GND and V_S and can be driven beyond V_{VS} and GND. During lack of V_{VS} or GND the output shows high impedance characteristic. The open drain output RX with an internal pull up resistor monitors the status at the K-pin to read the received data and control the transmitted data. Short circuit condition at K-pin is recognized if the internal open drain transistor isn't able to pull the voltage potential at K-pin below the threshold of $0.45 \cdot V_{VS}$. Then the RX stays in high condition. A timer starts and switches the open drain transistor after typ. 20μs off. A next low at the TX input resets the timer and the open drain transistor switches on again.

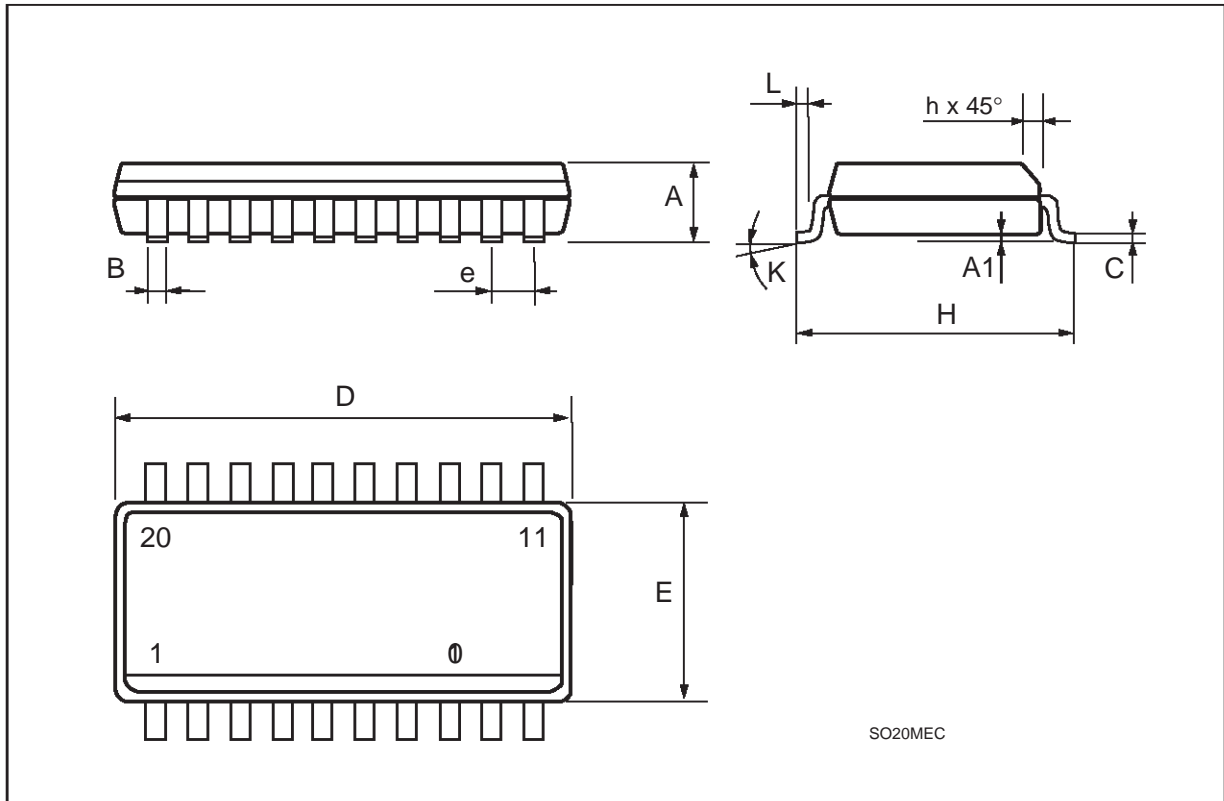
Figure 8. Functional schematic of the ISO-interface

| DIM. | mm | | | inch | | |
|------|--------------------|------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.35 | | 2.65 | 0.093 | | 0.104 |
| A1 | 0.1 | | 0.3 | 0.004 | | 0.012 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.23 | | 0.32 | 0.009 | | 0.013 |
| D | 12.6 | | 13 | 0.496 | | 0.512 |
| E | 7.4 | | 7.6 | 0.291 | | 0.299 |
| e | | 1.27 | | | 0.050 | |
| H | 10 | | 10.65 | 0.394 | | 0.419 |
| h | 0.25 | | 0.75 | 0.010 | | 0.030 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| K | 0° (min.)8° (max.) | | | | | |

OUTLINE AND MECHANICAL DATA



SO20



SO20MEC

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