



# ST72104G, ST72215G, ST72216G, ST72254G

## 8-BIT MCU WITH SINGLE VOLTAGE FLASH MEMORY, ADC, 16-BIT TIMERS, SPI, I<sup>2</sup>C INTERFACES

PRELIMINARY DATA

### ■ Memories

- 4K or 8K bytes Program memory (ROM and single voltage FLASH) with read-out protection and in-situ programming (remote ISP)
- 256 bytes RAM

### ■ Clock, Reset and Supply Management

- Enhanced reset system
- Enhanced low voltage supply supervisor with 3 programmable levels
- Clock sources: crystal/ceramic resonator oscillators or RC oscillators, external clock, backup Clock Security System
- Clock-out capability
- 3 Power Saving Modes: Halt, Wait and Slow

### ■ Interrupt Management

- 7 interrupt vectors plus TRAP and RESET
- 22 external interrupt lines (on 2 vectors)

### ■ 22 I/O Ports

- 22 multifunctional bidirectional I/O lines
- 14 alternate function lines
- 8 high sink outputs

### ■ 3 Timers

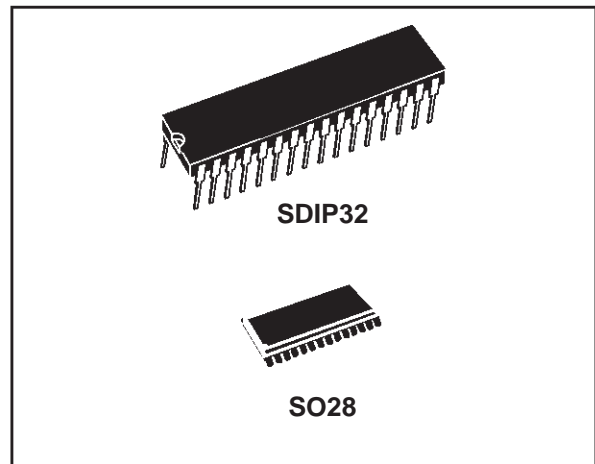
- Configurable watchdog timer
- Two 16-bit timers with: 2 input captures, 2 output compares, external clock input on one timer, PWM and Pulse generator modes (one only on ST72104Gx and ST72216G1)

### ■ 2 Communications Interfaces

- SPI synchronous serial interface
- I2C multimaster interface (only on ST72254Gx)

### ■ 1 Analog peripheral

- 8-bit ADC with 6 input channels (except on ST72104Gx)



### ■ Instruction Set

- 8-bit data manipulation
- 63 basic instructions
- 17 main addressing modes
- 8 x 8 unsigned multiply instruction
- True bit manipulation

### ■ Development Tools

- Full hardware/software development package

### Device Summary

Features	ST72104G1	ST72104G2	ST72216G1	ST72215G2	ST72254G1	ST72254G2
Program memory - bytes	4K	8K	4K	8K	4K	8K
RAM (stack) - bytes	256 (128)					
Peripherals	Watchdog timer, One 16-bit timer, SPI		Watchdog timer, One 16-bit timer, SPI, ADC	Watchdog timer, Two 16-bit timers, SPI, ADC	Watchdog timer, Two 16-bit timers, SPI, I <sup>2</sup> C, ADC	
Operating Supply	3.0V to 5.5V					
CPU Frequency	Up to 8 MHz (with oscillator up to 16 MHz)					
Operating Temperature	-40°C to +85°C (-40°C to +105/125°C optional)					
Packages	SO28 / SDIP32					

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1/135

This is preliminary information on a new product in development or undergoing evaluation. Details are subject to change without notice.

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**1 INTRODUCTION**

The ST72104G, ST72215G, ST72216G and ST72254G devices are members of the ST7 microcontroller family. They can be grouped as follows:

- ST72254G devices are designed for mid-range applications with ADC and I<sup>2</sup>C interface capabilities.
- ST72215/6G devices target the same range of applications but without I<sup>2</sup>C interface.
- ST72104G devices are for applications that do not need ADC and I<sup>2</sup>C peripherals.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

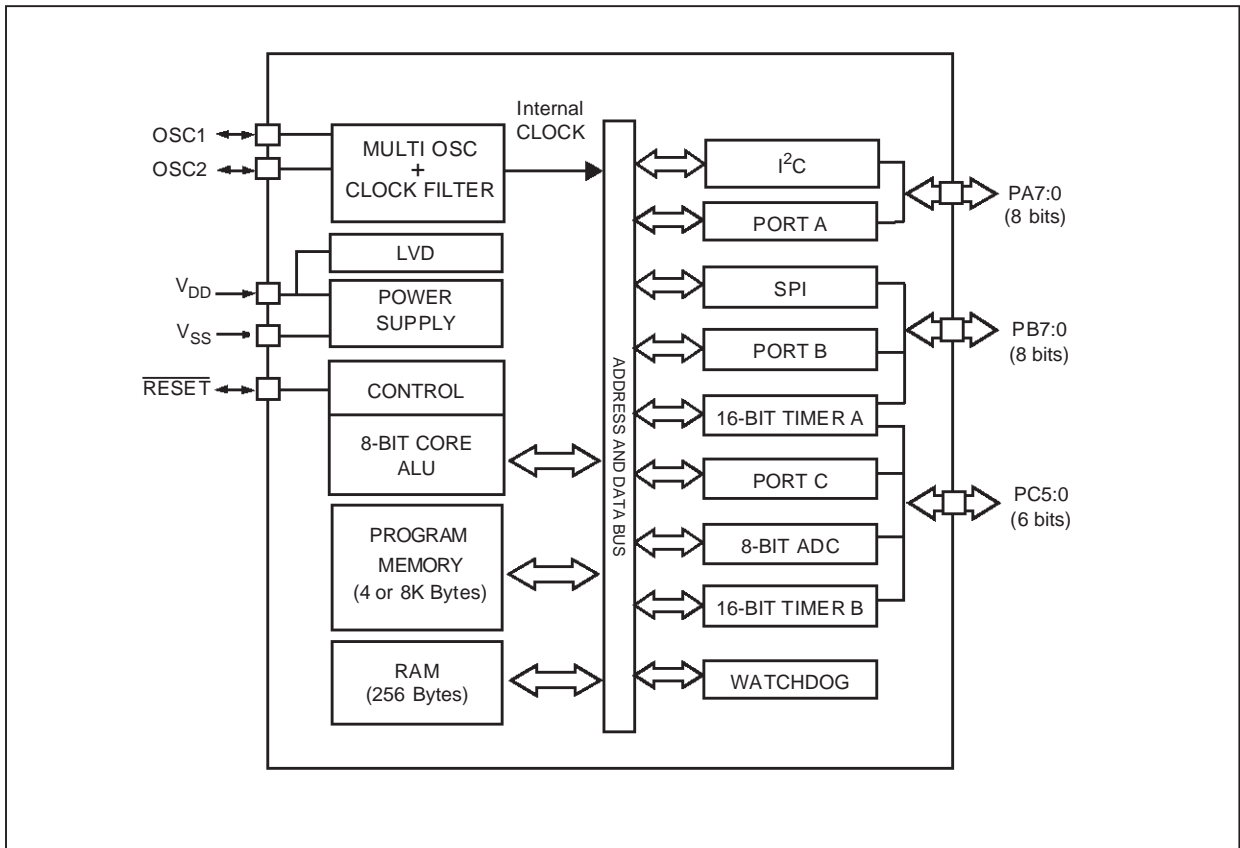
The ST72C104G, ST72C215G, ST72C216G and ST72C254G versions feature single-voltage FLASH memory with byte-by-byte In-Situ Programming (ISP) capability.

Under software control, all devices can be placed in WAIT, SLOW, or HALT mode, reducing power consumption when the application is in idle or standby state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

For easy reference, all parametric data are located in Section 13 on page 96.

**Figure 1. General Block Diagram**



## 2 PIN DESCRIPTION

Figure 2. 28-Pin SO Package Pinout

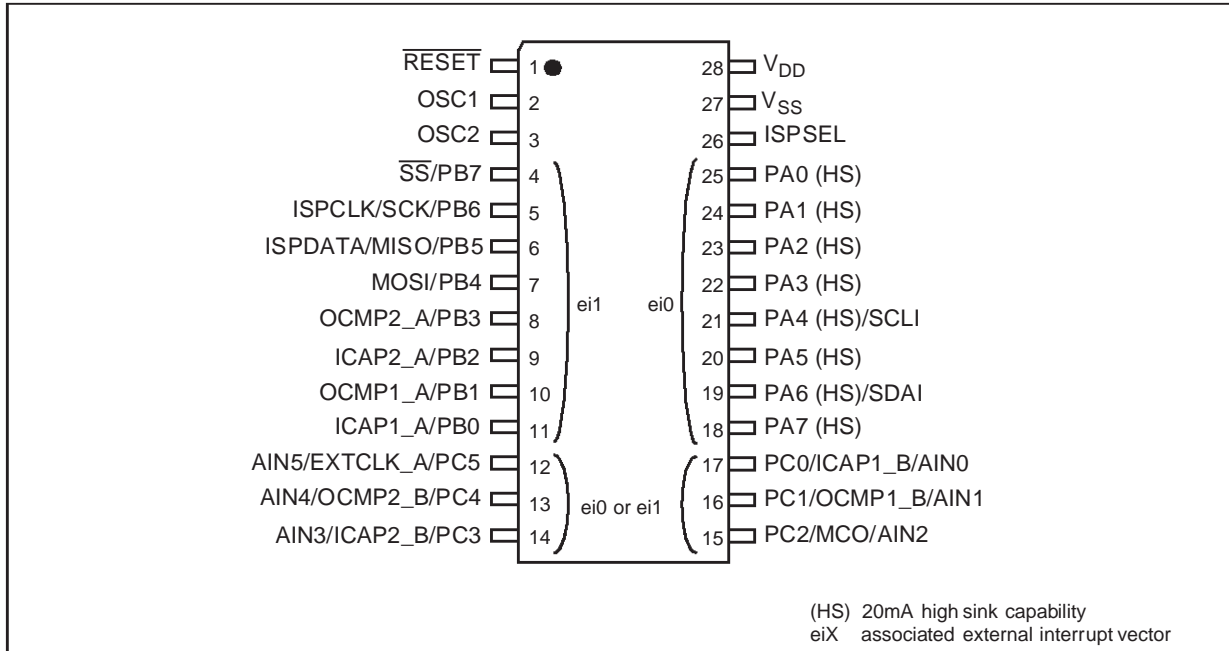
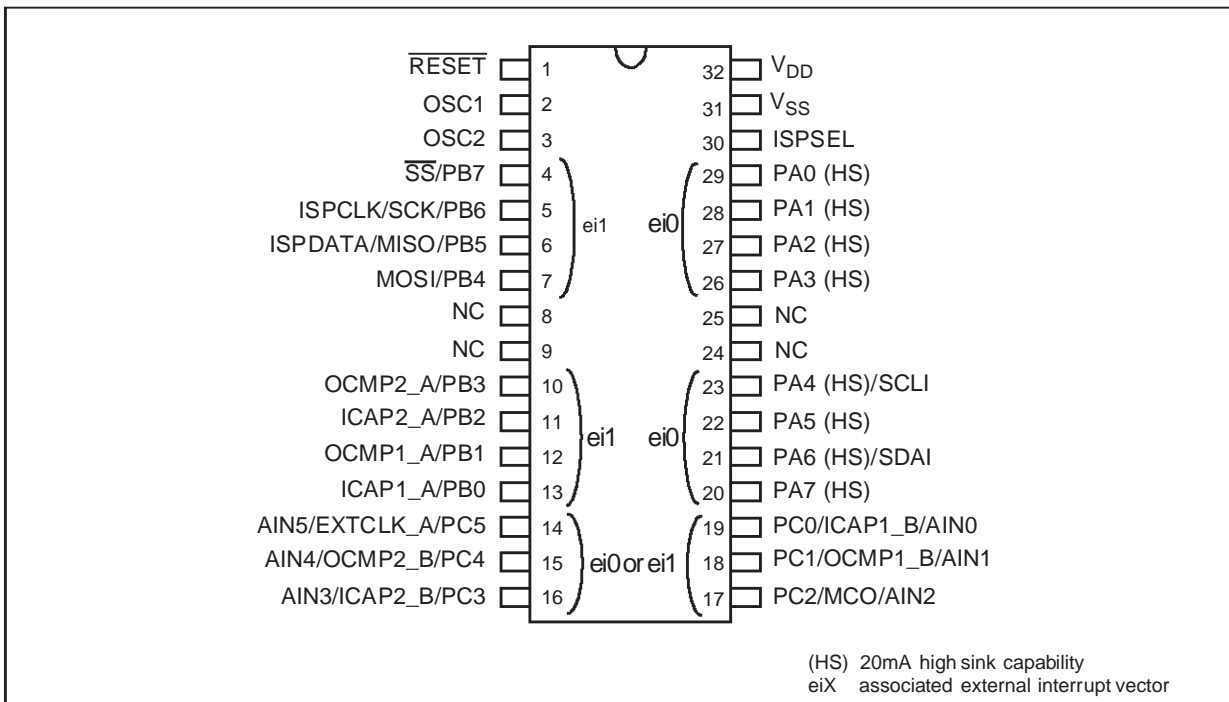


Figure 3. 32-Pin SDIP Package Pinout



**PIN DESCRIPTION (Cont'd)**

For external pin connection guidelines, refer to Section 13 "ELECTRICAL CHARACTERISTICS" on page 96.

**Legend / Abbreviations for Table 1:**

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C = CMOS 0.3V<sub>DD</sub>/0.7V<sub>DD</sub>,  
C<sub>T</sub> = CMOS 0.3V<sub>DD</sub>/0.7V<sub>DD</sub> with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt <sup>1)</sup>, ana = analog
- Output: OD = open drain <sup>2)</sup>, PP = push-pull

Refer to Section 9 "I/O PORTS" on page 30 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

**Table 1. Device Pin Description**

Pin n°	SDIP32	SO28	Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
					Input	Output	Input				Output			
							float	wpu	int	ana	OD	PP		
1	1	<b>RESET</b>	I/O	C <sub>T</sub>			X				X		Top priority non maskable interrupt (active low)	
2	2	OSC1 <sup>3)</sup>	I										External clock input or Resonator oscillator inverter input or resistor input for RC oscillator	
3	3	OSC2 <sup>3)</sup>	O										Resonator oscillator inverter output or capacitor input for RC oscillator	
4	4	PB7/ <b>SS</b>	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B7</b>	SPI Slave Select (active low)	
5	5	PB6/SCK/ISPCLK	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B6</b>	SPI Serial Clock or ISP Clock	
6	6	PB5/MISO/ISPDATA	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B5</b>	SPI Master In/ Slave Out Data or ISP Data	
7	7	PB4/MOSI	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B4</b>	SPI Master Out / Slave In Data	
8		NC	Not Connected											
9		NC												
10	8	PB3/OCMP2_A	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B3</b>	Timer A Output Compare 2	
11	9	PB2/ICAP2_A	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B2</b>	Timer A Input Capture 2	
12	10	PB1 /OCMP1_A	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B1</b>	Timer A Output Compare 1	
13	11	PB0 /ICAP1_A	I/O	C <sub>T</sub>	X	ei1				X	X	<b>Port B0</b>	Timer A Input Capture 1	
14	12	PC5/EXTCLK_A/AIN5	I/O	C <sub>T</sub>	X	ei0/ei1				X	X	<b>Port C5</b>	Timer A Input Clock or ADC Analog Input 5	
15	13	PC4/OCMP2_B/AIN4	I/O	C <sub>T</sub>	X	ei0/ei1				X	X	<b>Port C4</b>	Timer B Output Compare 2 or ADC Analog Input 4	
16	14	PC3/ ICAP2_B/AIN3	I/O	C <sub>T</sub>	X	ei0/ei1	X			X	X	<b>Port C3</b>	Timer B Input Capture 2 or ADC Analog Input 3	
17	15	PC2/MCO/AIN2	I/O	C <sub>T</sub>	X	ei0/ei1	X			X	X	<b>Port C2</b>	Main clock output (f <sub>CPU</sub> ) or ADC Analog Input 2	





Pin n°		Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
SDIP32	SO28			Input	Output	Input				Output			
						float	wpu	int	ana	OD	PP		
18	16	PC1/OCMP1_B/AIN1	I/O	C <sub>T</sub>	X	ei0/ei1	X	X	X			<b>Port C1</b>	Timer B Output Compare 1 or ADC Analog Input 1
19	17	PC0/ICAP1_B/AIN0	I/O	C <sub>T</sub>	X	ei0/ei1	X	X	X			<b>Port C0</b>	Timer B Input Capture 1 or ADC Analog Input 0
20	18	PA7	I/O	C <sub>T</sub>	HS	X	ei0		X	X		<b>Port A7</b>	
21	19	PA6 /SDAI	I/O	C <sub>T</sub>	HS	X	ei0		T			<b>Port A6</b>	I <sup>2</sup> C Data
22	20	PA5	I/O	C <sub>T</sub>	HS	X	ei0		X	X		<b>Port A5</b>	
23	21	PA4 /SCLI	I/O	C <sub>T</sub>	HS	X	ei0		T			<b>Port A4</b>	I <sup>2</sup> C Clock
24		NC	Not Connected										
25		NC											
26	22	PA3	I/O	C <sub>T</sub>	HS	X	ei0		X	X		<b>Port A3</b>	
27	23	PA2	I/O	C <sub>T</sub>	HS	X	ei0		X	X		<b>Port A2</b>	
28	24	PA1	I/O	C <sub>T</sub>	HS	X	ei0		X	X		<b>Port A1</b>	
29	25	PA0	I/O	C <sub>T</sub>	HS	X	ei0		X	X		<b>Port A0</b>	
30	26	ISPSEL	I	C		X							In situ programming selection (Should be tied low in standard user mode).
31	27	V <sub>SS</sub>	S										Ground
32	28	V <sub>DD</sub>	S										Main power supply

**Notes:**

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.
2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V<sub>DD</sub> are not implemented). See Section 9 “I/O PORTS” on page 30 and Section 13.8 “I/O PORT PIN CHARACTERISTICS” on page 114 for more details.
3. OSC1 and OSC2 pins connect a crystal or ceramic resonator, an external RC, or an external source to the on-chip oscillator see Section 2 “PIN DESCRIPTION” on page 7 and Section 13.5 “CLOCK AND TIMING CHARACTERISTICS” on page 104 for more details.

### 3 REGISTER & MEMORY MAP

As shown in the Figure 4, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register location, 256 bytes of RAM and up to 8Kbytes of user program memory. The RAM space includes up to 128 bytes for the stack from 0100h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

**IMPORTANT:** Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 4. Memory Map

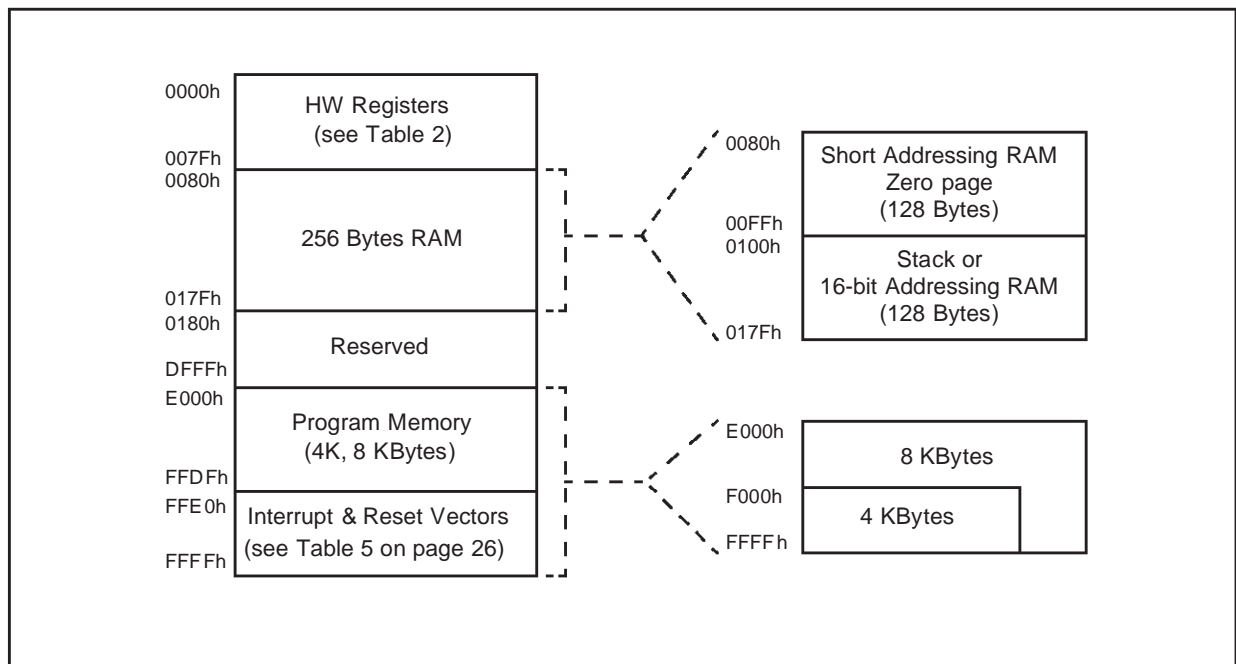


Table 2. Hardware Register Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h 0001h 0002h	Port C	PCDR PCDDR PCOR	Port C Data Register Port C Data Direction Register Port C Option Register	00h <sup>1)</sup> 00h 00h	R/W <sup>2)</sup> R/W <sup>2)</sup> R/W <sup>2)</sup>
0003h	Reserved (1 Byte)				
0004h 0005h 0006h	Port B	PBDR PBDDR PBOR	Port B Data Register Port B Data Direction Register Port B Option Register	00h <sup>1)</sup> 00h 00h	R/W R/W R/W.
0007h	Reserved (1 Byte)				
0008h 0009h 000Ah	Port A	PADR PADDR PAOR	Port A Data Register Port A Data Direction Register Port A Option Register	00h <sup>1)</sup> 00h 00h	R/W R/W R/W
000Bh to 001Fh	Reserved (21 Bytes)				
0020h		MISCR1	Miscellaneous Register 1	00h	R/W
0021h 0022h 0023h	SPI	SPIDR SPICR SPISR	SPI Data I/O Register SPI Control Register SPI Status Register	xxh 0xh 00h	R/W R/W Read Only
0024h	WATCHDOG	WDGCR	Watchdog Control Register	7Fh	R/W
0025h		CRSR	Clock, Reset, Supply Control / Status Register	000x 000x	R/W
0026h 0027h	Reserved (2 bytes)				
0028h 0029h 002Ah 002Bh 002Ch 002Dh 002Eh	I <sup>2</sup> C	I2CCR I2CSR1 I2CSR2 I2CCCR I2COAR1 I2COAR2 I2CDR	Control Register Status Register 1 Status Register 2 Clock Control Register Own Address Register 1 Own Address Register 2 Data Register	00h 00h 00h 00h 00h 00h 00h	R/W Read Only Read Only R/W R/W R/W R/W
002Fh to 0030h	Reserved (4 Bytes)				

**ST72104G, ST72215G, ST72216G, ST72254G**

Address	Block	Register Label	Register Name	Reset Status	Remarks
0031h	TIMER A	TACR2	Timer A Control Register 2	00h	R/W
0032h		TACR1	Timer A Control Register 1	00h	R/W
0033h		TASR	Timer A Status Register	xxh	Read Only
0034h		TAIC1HR	Timer A Input Capture 1 High Register	xxh	Read Only
0035h		TAIC1LR	Timer A Input Capture 1 Low Register	xxh	Read Only
0036h		TAOC1HR	Timer A Output Compare 1 High Register	80h	R/W
0037h		TAOC1LR	Timer A Output Compare 1 Low Register	00h	R/W
0038h		TACHR	Timer A Counter High Register	FFh	Read Only
0039h		TACL	Timer A Counter Low Register	FCh	Read Only
003Ah		TAACHR	Timer A Alternate Counter High Register	FFh	Read Only
003Bh		TAACL	Timer A Alternate Counter Low Register	FCh	Read Only
003Ch		TAIC2HR	Timer A Input Capture 2 High Register	xxh	Read Only
003Dh		TAIC2LR	Timer A Input Capture 2 Low Register	xxh	Read Only
003Eh		TAOC2HR	Timer A Output Compare 2 High Register	80h	R/W
003Fh		TAOC2LR	Timer A Output Compare 2 Low Register	00h	R/W
0040h		MISCR2	Miscellaneous Register 2	00h	R/W
0041h	TIMER B	TBCR2	Timer B Control Register 2	00h	R/W
0042h		TBCR1	Timer B Control Register 1	00h	R/W
0043h		TBSR	Timer B Status Register	xxh	Read Only
0044h		TBIC1HR	Timer B Input Capture 1 High Register	xxh	Read Only
0045h		TBIC1LR	Timer B Input Capture 1 Low Register	xxh	Read Only
0046h		TBOC1HR	Timer B Output Compare 1 High Register	80h	R/W
0047h		TBOC1LR	Timer B Output Compare 1 Low Register	00h	R/W
0048h		TBCHR	Timer B Counter High Register	FFh	Read Only
0049h		TBCLR	Timer B Counter Low Register	FCh	Read Only
004Ah		TBACHR	Timer B Alternate Counter High Register	FFh	Read Only
004Bh		TBACL	Timer B Alternate Counter Low Register	FCh	Read Only
004Ch		TBIC2HR	Timer B Input Capture 2 High Register	xxh	Read Only
004Dh		TBIC2LR	Timer B Input Capture 2 Low Register	xxh	Read Only
004Eh		TBOC2HR	Timer B Output Compare 2 High Register	80h	R/W
004Fh		TBOC2LR	Timer B Output Compare 2 Low Register	00h	R/W
0050h to 006Fh	Reserved (32 Bytes)				
0070h	ADC	ADCDR	Data Register	00h	Read Only
0071h		ADCCSR	Control/Status Register	00h	R/W
0072h to 007Fh	Reserved (14 Bytes)				

**Legend:** x=undefined, R/W=read/write

**Notes:**

1. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.
2. The bits associated with unavailable pins must always keep their reset value.

## 4 FLASH PROGRAM MEMORY

### 4.1 INTRODUCTION

FLASH devices have a single voltage non-volatile FLASH memory that may be programmed in-situ (or plugged in a programming tool) on a byte-by-byte basis.

### 4.2 MAIN FEATURES

- Remote In-Situ Programming (ISP) mode
- Up to 16 bytes programmed in the same cycle
- MTP memory (Multiple Time Programmable)
- Read-out memory protection against piracy

### 4.3 STRUCTURAL ORGANISATION

The FLASH program memory is organised in a single 8-bit wide memory block which can be used for storing both code and data constants.

The FLASH program memory is mapped in the upper part of the ST7 addressing space and includes the reset and interrupt user vector area .

### 4.4 IN-SITU PROGRAMMING (ISP) MODE

The FLASH program memory can be programmed using Remote ISP mode. This ISP mode allows the contents of the ST7 program memory to be updated using a standard ST7 programming tools after the device is mounted on the application board. This feature can be implemented with a minimum number of added components and board area impact.

An example Remote ISP hardware interface to the standard ST7 programming tool is described below. For more details on ISP programming, refer to the ST7 Programming Specification.

#### Remote ISP Overview

The Remote ISP mode is initiated by a specific sequence on the dedicated ISPSEL pin.

The Remote ISP is performed in three steps:

- Selection of the RAM execution mode
- Download of Remote ISP code in RAM
- Execution of Remote ISP code in RAM to program the user program into the FLASH

#### Remote ISP hardware configuration

In Remote ISP mode, the ST7 has to be supplied with power ( $V_{DD}$  and  $V_{SS}$ ) and a clock signal (oscillator and application crystal circuit for example).

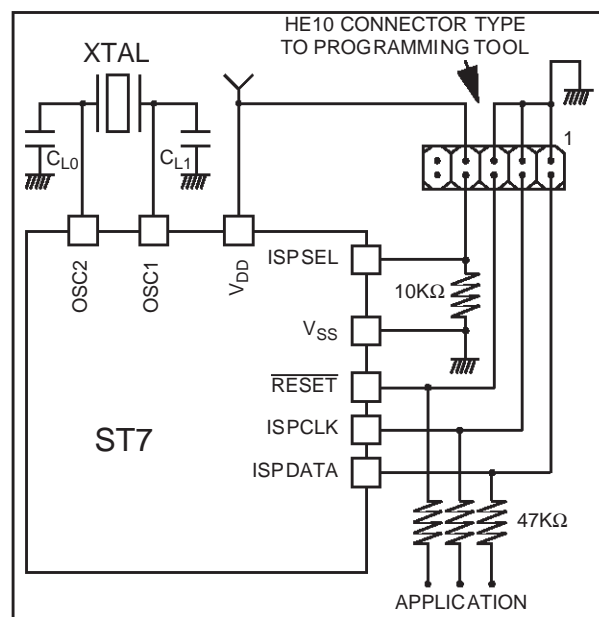
This mode needs five signals (plus the  $V_{DD}$  signal if necessary) to be connected to the programming tool. This signals are:

- $\overline{RESET}$ : device reset
- $V_{SS}$ : device ground power supply
- ISPCLK: ISP output serial clock pin
- ISPDATA: ISP input serial data pin
- ISPSEL: Remote ISP mode selection. This pin must be connected to  $V_{SS}$  on the application board through a pull-down resistor.

If any of these pins are used for other purposes on the application, a serial resistor has to be implemented to avoid a conflict if the other device forces the signal level.

Figure 5 shows a typical hardware interface to a standard ST7 programming tool. For more details on the pin locations, refer to the device pinout description.

**Figure 5. Typical Remote ISP Interface**



### 4.5 MEMORY READ-OUT PROTECTION

The read-out protection is enabled through an option bit.

For FLASH devices, when this option is selected, the program and data stored in the FLASH memory are protected against read-out piracy (including a re-write protection). When this protection option is removed the entire FLASH program memory is first automatically erased. However, the E<sup>2</sup>PROM data memory (when available) can be protected only with ROM devices.

## 5 CENTRAL PROCESSING UNIT

### 5.1 INTRODUCTION

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

### 5.2 MAIN FEATURES

- 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes
- Two 8-bit index registers
- 16-bit stack pointer
- Low power modes
- Maskable hardware interrupts
- Non-maskable software interrupt

### 5.3 CPU REGISTERS

The 6 CPU registers shown in Figure 6 are not present in the memory mapping and are accessed by specific instructions.

#### Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

#### Index Registers (X and Y)

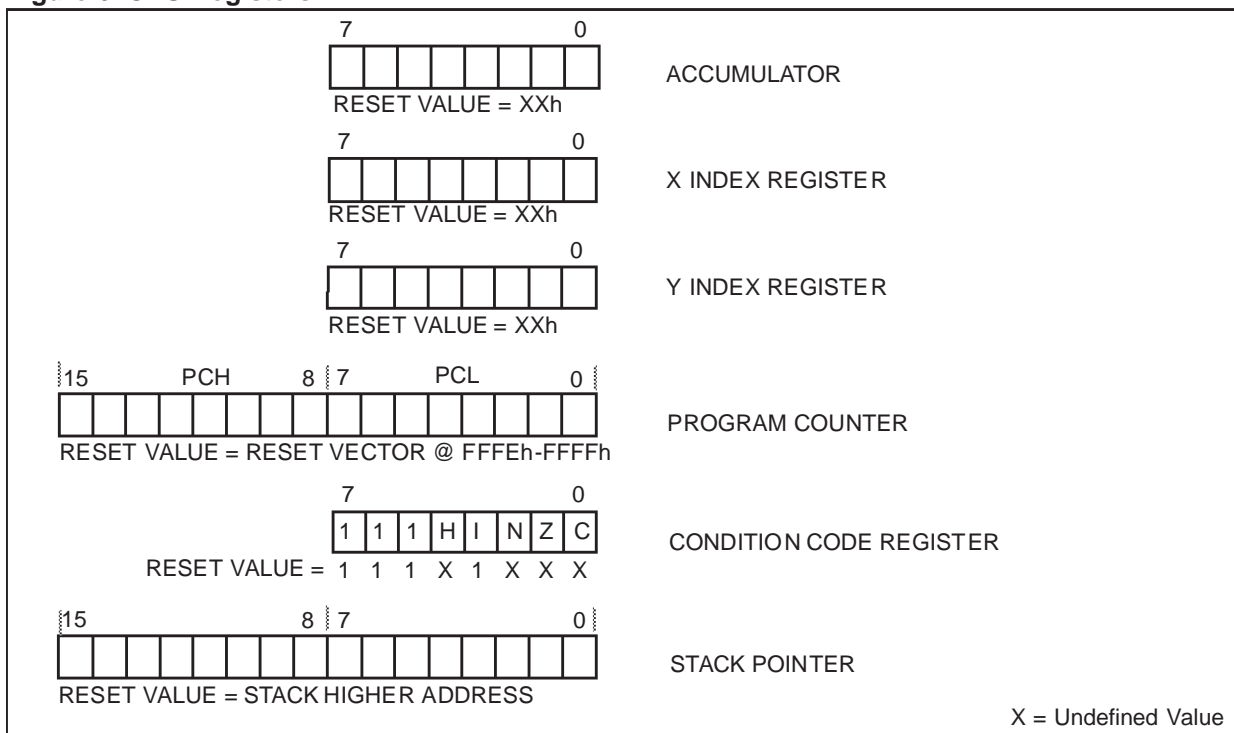
In indexed addressing modes, these 8-bit registers are used to create either effective addresses or temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures (not pushed to and popped from the stack).

#### Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 6. CPU Registers



**CPU REGISTERS (Cont'd)****CONDITION CODE REGISTER (CC)**

Read/Write

Reset Value: 111x1xxx

7							0
1	1	1	H	I	N	Z	C

The 8-bit Condition Code register contains the interrupt mask and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

**Bit 4 = H Half carry.**

This bit is set by hardware when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. It is reset by hardware during the same instructions.

0: No half carry has occurred.

1: A half carry has occurred.

This bit is tested using the JRH or JRNH instruction. The H bit is useful in BCD arithmetic subroutines.

**Bit 3 = I Interrupt mask.**

This bit is set by hardware when entering in interrupt or by software to disable all interrupts except the TRAP software interrupt. This bit is cleared by software.

0: Interrupts are enabled.

1: Interrupts are disabled.

This bit is controlled by the RIM, SIM and IRET instructions and is tested by the JRM and JRNM instructions.

**Note:** Interrupts requested while I is set are latched and can be processed when I is cleared. By default an interrupt routine is not interruptable because the I bit is set by hardware when you enter it and reset by the IRET instruction at the end of

the interrupt routine. If the I bit is cleared by software in the interrupt routine, pending interrupts are serviced regardless of the priority level of the current interrupt routine.

**Bit 2 = N Negative.**

This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It is a copy of the 7<sup>th</sup> bit of the result.

0: The result of the last operation is positive or null.

1: The result of the last operation is negative

(i.e. the most significant bit is a logic 1).

This bit is accessed by the JRMI and JRPL instructions.

**Bit 1 = Z Zero.**

This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

0: The result of the last operation is different from zero.

1: The result of the last operation is zero.

This bit is accessed by the JREQ and JRNE test instructions.

**Bit 0 = C Carry/borrow.**

This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.

0: No overflow or underflow has occurred.

1: An overflow or underflow has occurred.

This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the "bit test and branch", shift and rotate instructions.





## 6 SUPPLY, RESET AND CLOCK MANAGEMENT

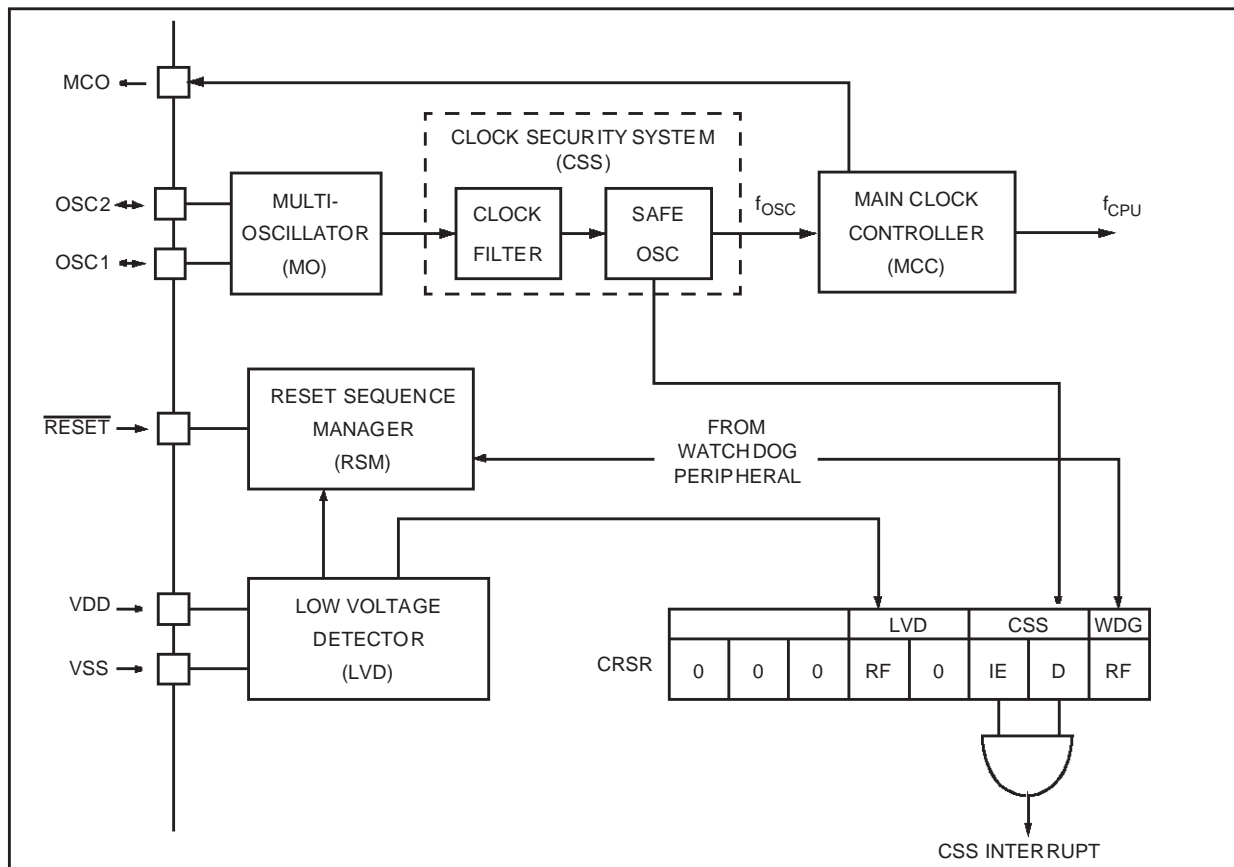
The ST72104G, ST72215G, ST72216G and ST72254G microcontrollers include a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components. An overview is shown in Figure 8.

See Section 13 "ELECTRICAL CHARACTERISTICS" on page 96 for more details.

### Main Features

- Supply Manager with main supply low voltage detection (LVD)
- Reset Sequence Manager (RSM)
- Multi-Oscillator (MO)
  - 4 Crystal/Ceramic resonator oscillators
  - 1 External RC oscillator
  - 1 Internal RC oscillator
- Clock Security System (CSS)
  - Clock Filter
  - Backup Safe Oscillator

Figure 8. Clock, Reset and Supply Block Diagram



**6.1 LOW VOLTAGE DETECTOR (LVD)**

To allow the integration of power management features in the application, the Low Voltage Detector function (LVD) generates a static reset when the  $V_{DD}$  supply voltage is below a  $V_{IT-}$  reference value. This means that it secures the power-up as well as the power-down keeping the ST7 in reset.

The  $V_{IT-}$  reference value for a voltage drop is lower than the  $V_{IT+}$  reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when  $V_{DD}$  is below:

- $V_{IT+}$  when  $V_{DD}$  is rising
- $V_{IT-}$  when  $V_{DD}$  is falling

The LVD function is illustrated in the Figure 9.

Provided the minimum  $V_{DD}$  value (guaranteed for the oscillator frequency) is below  $V_{IT-}$ , the MCU can only be in two modes:

- under full software control
- in static safe reset

In these conditions, secure operation is always ensured for the application without the need for external reset hardware.

During a Low Voltage Detector Reset, the  $\overline{RESET}$  pin is held low, thus permitting the MCU to reset other devices.

**Notes:**

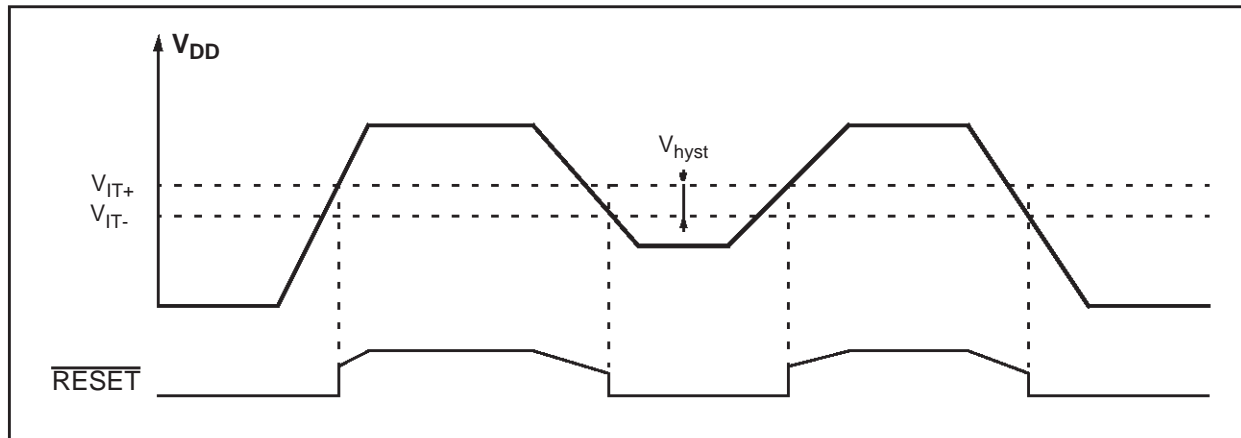
1. The LVD allows the device to be used without any external RESET circuitry.
2. Three different reference levels are selectable through the option byte according to the application requirement.

**LVD application note**

Application software can detect a reset caused by the LVD by reading the LVDRF bit in the CRSR register.

This bit is set by hardware when a LVD reset is generated and cleared by software (writing zero).

**Figure 9. Low Voltage Detector vs Reset**



## 6.2 RESET SEQUENCE MANAGER (RSM)

### 6.2.1 Introduction

The reset sequence manager includes three RESET sources as shown in Figure 11:

- External  $\overline{\text{RESET}}$  source pulse
- Internal LVD RESET (Low Voltage Detection)
- Internal WATCHDOG RESET

These sources act on the  $\overline{\text{RESET}}$  pin and it is always kept low during the delay phase.

The RESET service routine vector is fixed at addresses FFFEh-FFFFh in the ST7 memory map.

The basic RESET sequence consists of 3 phases as shown in Figure 10:

- Delay depending on the RESET source
- 4096 CPU clock cycle delay
- RESET vector fetch

The 4096 CPU clock cycle delay allows the oscillator to stabilise and ensures that recovery has taken place from the Reset state.

The RESET vector fetch phase duration is 2 clock cycles.

Figure 10. RESET Sequence Phases

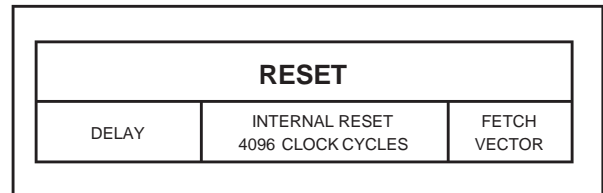
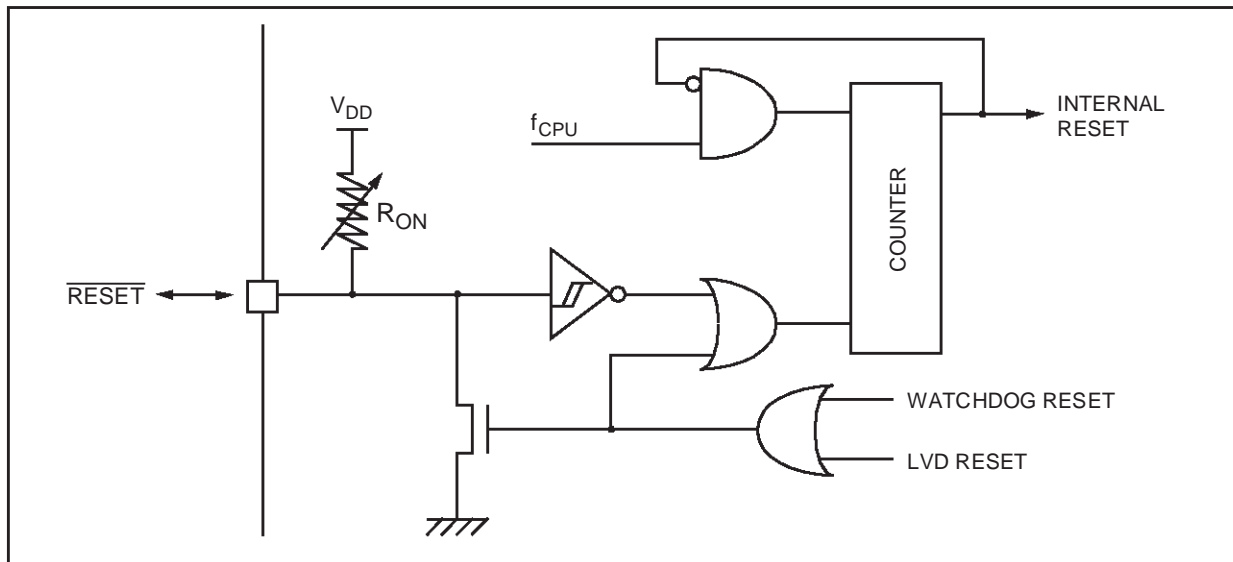


Figure 11. Reset Block Diagram



RESET SEQUENCE MANAGER (Cont'd)

6.2.2 Asynchronous External  $\overline{\text{RESET}}$  pin

The  $\overline{\text{RESET}}$  pin is both an input and an open-drain output with integrated  $R_{\text{ON}}$  weak pull-up resistor. This pull-up has no fixed value but varies in accordance with the input voltage. It can be pulled low by external circuitry to reset the device. See electrical characteristics section for more details.

A RESET signal originating from an external source must have a duration of at least  $t_{\text{h(RSTL)in}}$  in order to be recognized. This detection is asynchronous and therefore the MCU can enter reset state even in HALT mode.

The  $\overline{\text{RESET}}$  pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

Two RESET sequences can be associated with this RESET source: short or long external reset pulse (see Figure 12).

Starting from the external RESET pulse recognition, the device  $\overline{\text{RESET}}$  pin acts as an output that is pulled low during at least  $t_{\text{w(RSTL)out}}$ .

6.2.3 Internal Low Voltage Detection RESET

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-On RESET
- Voltage Drop RESET

The device  $\overline{\text{RESET}}$  pin acts as an output that is pulled low when  $V_{\text{DD}} < V_{\text{IT+}}$  (rising edge) or  $V_{\text{DD}} < V_{\text{IT-}}$  (falling edge) as shown in Figure 12.

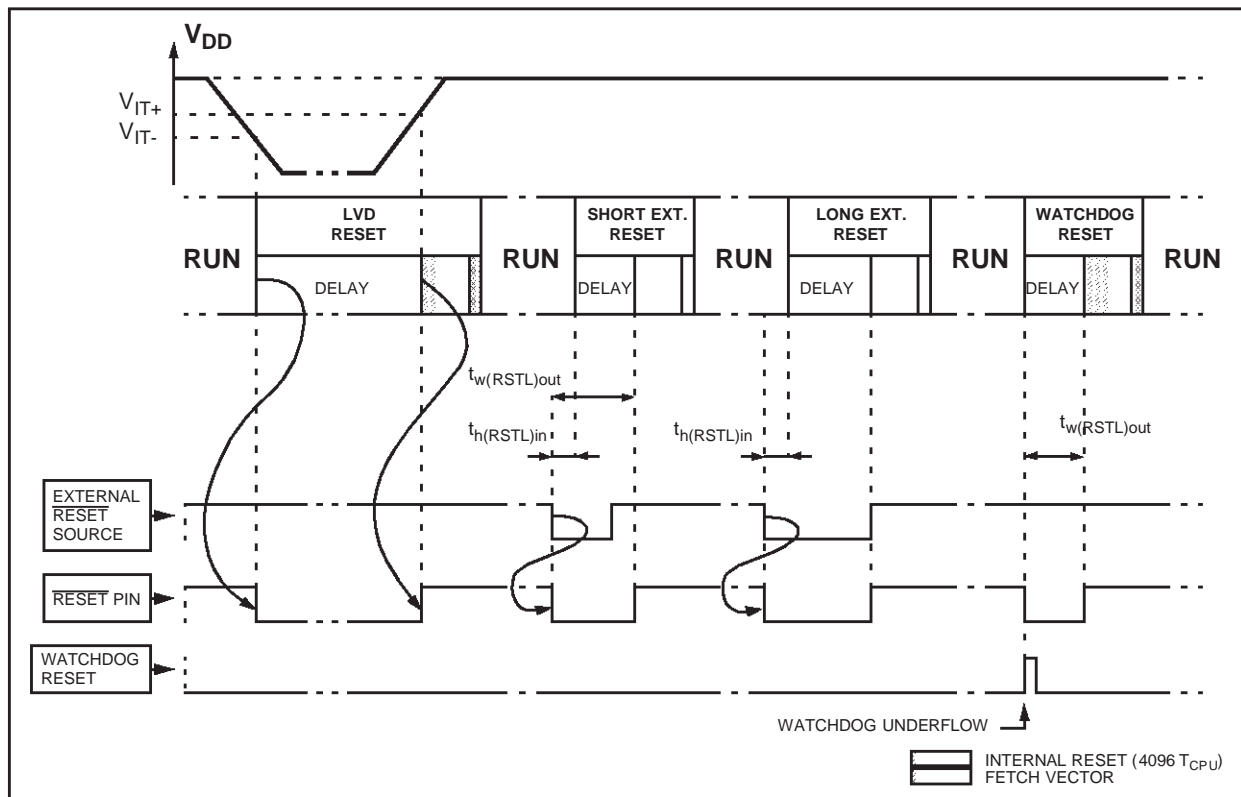
The LVD filters spikes on  $V_{\text{DD}}$  larger than  $t_{\text{g(VDD)}}$  to avoid parasitic resets.

6.2.4 Internal Watchdog RESET

The RESET sequence generated by a internal Watchdog counter overflow is shown in Figure 12.

Starting from the Watchdog counter underflow, the device  $\overline{\text{RESET}}$  pin acts as an output that is pulled low during at least  $t_{\text{w(RSTL)out}}$ .

Figure 12. RESET Sequences



### 6.3 MULTI-OSCILLATOR (MO)

The main clock of the ST7 can be generated by four different source types coming from the multi-oscillator block:

- an external source
- 4 crystal or ceramic resonator oscillators
- an external RC oscillator
- an internal high frequency RC oscillator

Each oscillator is optimized for a given frequency range in terms of consumption and is selectable through the option byte. The associated hardware configuration are shown in Table 3. Refer to the electrical characteristics section for more details.

#### External Clock Source

In this external clock mode, a clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC1 pin while the OSC2 pin is tied to ground.

#### Crystal/Ceramic Oscillators

This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. The selection within a list of 4 oscillators with different frequency ranges has to be done by option byte in order to reduce consumption. In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator start-up phase.

#### External RC Oscillator

This oscillator allows a low cost solution for the main clock of the ST7 using only an external resistor and an external capacitor. The frequency of the external RC oscillator (in the range of some MHz.) is fixed by the resistor and the capacitor values. Consequently in this MO mode, the accuracy of the clock is directly linked to the accuracy of the discrete components.

#### Internal RC Oscillator

The internal RC oscillator mode is based on the same principle as the external RC oscillator including the resistance and the capacitance of the device. This mode is the most cost effective one with the drawback of a lower frequency accuracy. Its frequency is in the range of several MHz.

In this mode, the two oscillator pins have to be tied to ground.

Table 3. ST7 Clock Sources

	Hardware Configuration
External Clock	
Crystal/Ceramic Resonators	
External RC Oscillator	
Internal RC Oscillator	

**6.4 CLOCK SECURITY SYSTEM (CSS)**

The Clock Security System (CSS) protects the ST7 against main clock problems. To allow the integration of the security features in the applications, it is based on a clock filter control and an Internal safe oscillator. The CSS can be enabled or disabled by option byte.

**6.4.1 Clock Filter Control**

The clock filter is based on a clock frequency limitation function.

This filter function is able to detect and filter high frequency spikes on the ST7 main clock.

If the oscillator is not working properly (e.g. working at a harmonic frequency of the resonator), the current active oscillator clock can be totally filtered, and then no clock signal is available for the ST7 from this oscillator anymore. If the original clock source recovers, the filtering is stopped automatically and the oscillator supplies the ST7 clock.

**6.4.2 Safe Oscillator Control**

The safe oscillator of the CSS block is a low frequency back-up clock source (see Figure 13).

If the clock signal disappears (due to a broken or disconnected resonator...) during a safe oscillator period, the safe oscillator delivers a low frequency clock signal which allows the ST7 to perform some rescue operations.

Automatically, the ST7 clock source switches back from the safe oscillator if the original clock source recovers.

**Limitation detection**

The automatic safe oscillator selection is notified by hardware setting the CSSD bit of the CRSR register. An interrupt can be generated if the CSSIE bit has been previously set.

These two bits are described in the CRSR register description.

**6.4.3 Low Power Modes**

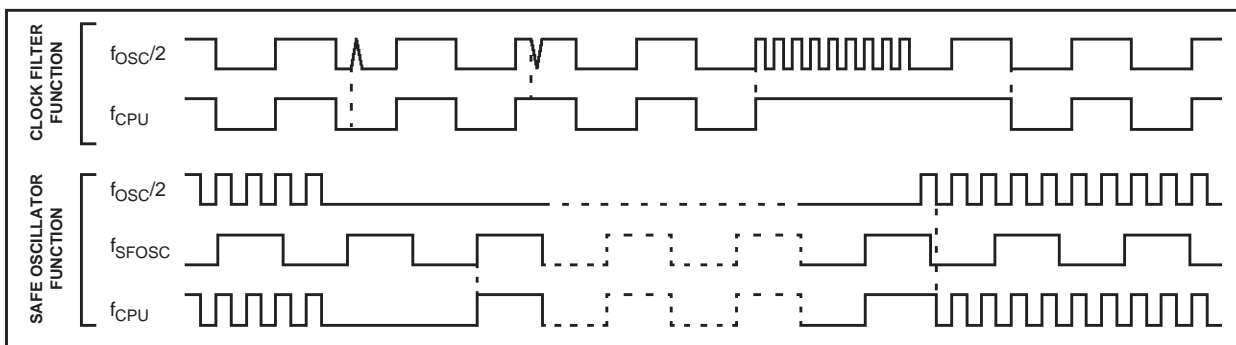
Mode	Description
WAIT	No effect on CSS. CSS interrupt cause the device to exit from Wait mode.
HALT	The CRSR register is frozen. The CSS (including the safe oscillator) is disabled until HALT mode is exited. The previous CSS configuration resumes when the MCU is woken up by an interrupt with "exit from HALT mode" capability or from the counter reset value when the MCU is woken up by a RESET.

**6.4.4 Interrupts**

The CSS interrupt event generates an interrupt if the corresponding Enable Control Bit (CSSIE) is set and the interrupt mask in the CC register is reset (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
CSS event detection (safe oscillator activated as main clock)	CSSD	CSSIE	Yes	No

**Figure 13. Clock Filter Function and Safe Oscillator Function**



**6.5 CLOCK RESET AND SUPPLY REGISTER DESCRIPTION (CRSR)**

Read/Write

Reset Value: 000x 000x (XXh)

7							0
0	0	0	LVD RF	0	CSS IE	CSS D	WDG RF

Bit 7:5 = **Reserved**, always read as 0.

Bit 4 = **LVDRF** *LVD reset flag*

This bit indicates that the last RESET was generated by the LVD block. It is set by hardware (LVD reset) and cleared by software (writing zero). See WDGRF flag description for more details. When the LVD is disabled by option byte, the LVDRF bit value is undefined.

Bit 3 = **Reserved**, always read as 0.

Bit 2 = **CSSIE** *Clock security syst interrupt enable*

This bit enables the interrupt when a disturbance is detected by the clock security system (CSSD bit set). It is set and cleared by software.

0: Clock security system interrupt disabled

1: Clock security system interrupt enabled

Refer to Table 5, "Interrupt Mapping," on page 26 for more details on the CSS interrupt vector. When the CSS is disabled by option byte, the CSSIE bit has no effect.

Bit 1 = **CSSD** *Clock security system detection*

This bit indicates that the safe oscillator of the clock security system block has been selected by hardware due to a disturbance on the main clock signal ( $f_{OSC}$ ). It is set by hardware and cleared by reading the CRSR register when the original oscillator recovers.

0: Safe oscillator is not active

1: Safe oscillator has been activated

When the CSS is disabled by option byte, the CSSD bit value is forced to 0.

Bit 0 = **WDGRF** *Watchdog reset flag*

This bit indicates that the last RESET was generated by the watchdog peripheral. It is set by hardware (Watchdog RESET) and cleared by software (writing zero) or an LVD RESET (to ensure a stable cleared state of the WDGRF flag when the CPU starts).

Combined with the LVDRF flag information, the flag description is given by the following table.

RESET Sources	LVDRF	WDGRF
External RESET pin	0	0
Watchdog	0	1
LVD	1	X

**Application notes**

The LVDRF flag is not cleared when another RESET type occurs (external or watchdog), the LVDRF flag remains set to keep trace of the original failure.

In this case, a watchdog reset can be detected by software while an external reset can not.

**Table 4. Clock, Reset and Supply Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0025h	CRSR Reset Value	0	0	0	LVDRF x	0	CSSIE 0	CSSD 0	WDGRF x

**6.6 MAIN CLOCK CONTROLLER (MCC)**

The Main Clock Controller (MCC) supplies the clock for the ST7 CPU and its internal peripherals. It allows SLOW power saving mode to be managed by the application.

All functions are managed by the Miscellaneous register 1 (MISCR1).

The MCC block consists of:

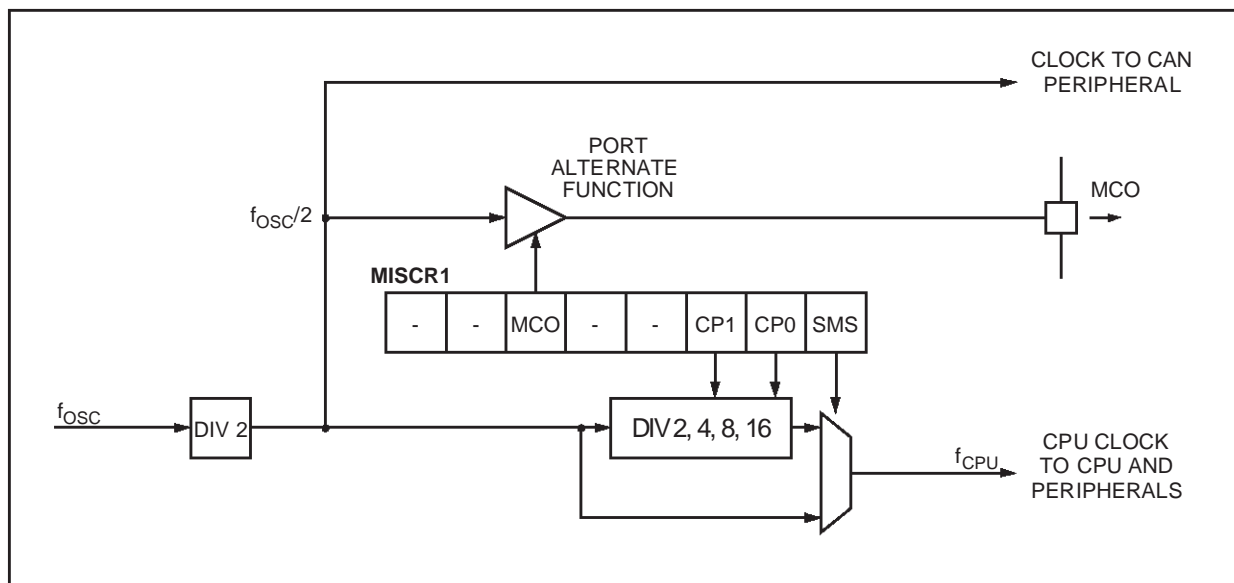
- A programmable CPU clock prescaler
- A clock-out signal to supply external devices

The prescaler allows the selection of the main clock frequency and is controlled by three bits of the MISCR1: CP1, CP0 and SMS.

The clock-out capability consists of a dedicated I/O port pin configurable as an  $f_{CPU}$  clock output to drive external devices. It is controlled by the MCO bit in the MISCR1 register.

See Section 10 "MISCELLANEOUS REGISTERS" on page 36 for more details.

**Figure 14. Main Clock Controller (MCC) Block Diagram**





## 7 INTERRUPTS

The ST7 core may be interrupted by one of two different methods: maskable hardware interrupts as listed in the Interrupt Mapping Table and a non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 15.

The maskable interrupts must be enabled clearing the I bit in order to be serviced. However, disabled interrupts may be latched and processed when they are enabled (see external interrupts subsection).

When an interrupt has to be serviced:

- Normal processing is suspended at the end of the current instruction execution.
- The PC, X, A and CC registers are saved onto the stack.
- The I bit of the CC register is set to prevent additional interrupts.
- The PC is then loaded with the interrupt vector of the interrupt to service and the first instruction of the interrupt service routine is fetched (refer to the Interrupt Mapping Table for vector addresses).

The interrupt service routine should finish with the IRET instruction which causes the contents of the saved registers to be recovered from the stack.

**Note:** As a consequence of the IRET instruction, the I bit will be cleared and the main program will resume.

### Priority management

By default, a servicing interrupt cannot be interrupted because the I bit is set by hardware entering in interrupt routine.

In the case when several interrupts are simultaneously pending, an hardware priority defines which one will be serviced first (see the Interrupt Mapping Table).

### Interrupts and Low power mode

All interrupts allow the processor to leave the WAIT low power mode. Only external and specifically mentioned interrupts allow the processor to leave the HALT low power mode (refer to the "Exit from HALT" column in the Interrupt Mapping Table).

#### 7.1 NON MASKABLE SOFTWARE INTERRUPT

This interrupt is entered when the TRAP instruction is executed regardless of the state of the I bit.

It will be serviced according to the flowchart on Figure 15.

#### 7.2 EXTERNAL INTERRUPTS

External interrupt vectors can be loaded into the PC register if the corresponding external interrupt occurred and if the I bit is cleared. These interrupts allow the processor to leave the Halt low power mode.

The external interrupt polarity is selected through the miscellaneous register or interrupt register (if available).

An external interrupt triggered on edge will be latched and the interrupt request automatically cleared upon entering the interrupt service routine.

If several input pins, connected to the same interrupt vector, are configured as interrupts, their signals are logically ANDed before entering the edge/level detection block.

**Caution:** The type of sensitivity defined in the Miscellaneous or Interrupt register (if available) applies to the ei source. In case of an ANDed source (as described on the I/O ports section), a low level on an I/O pin configured as input with interrupt, masks the interrupt request even in case of rising-edge sensitivity.

#### 7.3 PERIPHERAL INTERRUPTS

Different peripheral interrupt flags in the status register are able to cause an interrupt when they are active if both:

- The I bit of the CC register is cleared.
- The corresponding enable bit is set in the control register.

If any of these two conditions is false, the interrupt is latched and thus remains pending.

Clearing an interrupt request is done by:

- Writing "0" to the corresponding bit in the status register or
- Access to the status register while the flag is set followed by a read or write of an associated register.

**Note:** the clearing sequence resets the internal latch. A pending interrupt (i.e. waiting for being enabled) will therefore be lost if the clear sequence is executed.

INTERRUPTS (Cont'd)

Figure 15. Interrupt Processing Flowchart

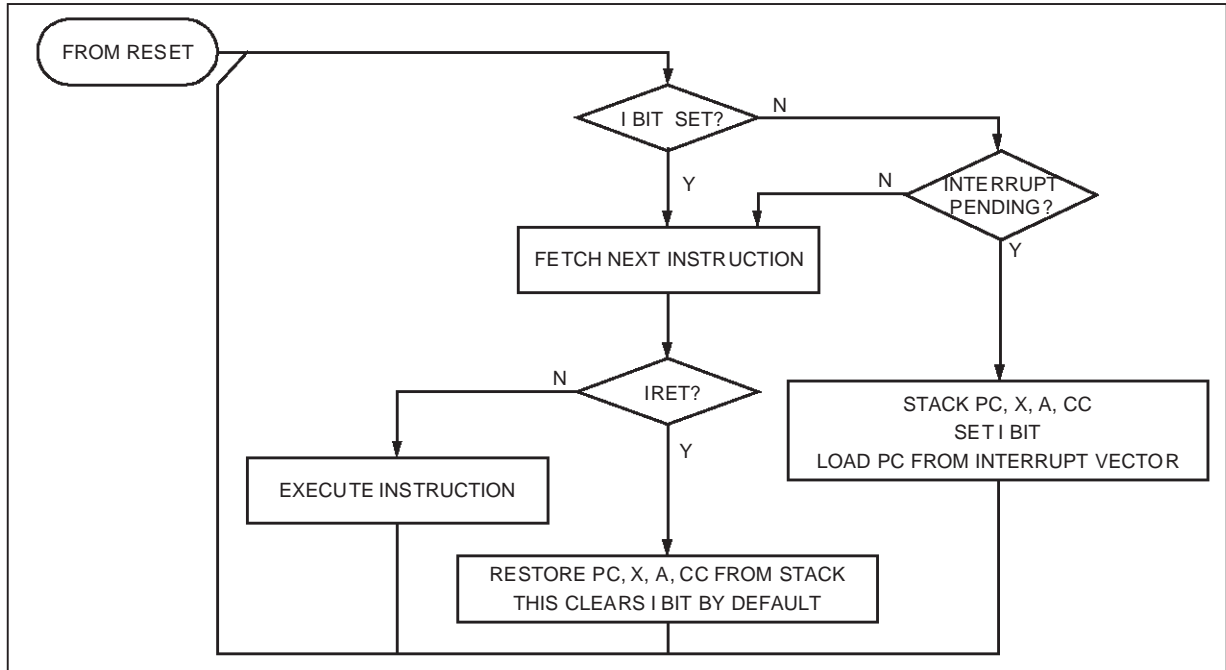


Table 5. Interrupt Mapping

N°	Source Block	Description	Register Label	Priority Order	Exit from HALT	Address Vector
	RESET	Reset	N/A	Highest Priority ↓ Lowest Priority	yes	FFFEh-FFFFh
	TRAP	Software Interrupt			no	FFFCh-FFFDh
0	ei0	External Interrupt Port A7..0 (C5..0 <sup>1</sup> )			yes	FFFAh-FFFBh
1	ei1	External Interrupt Port B7..0 (C5..0 <sup>1</sup> )			FFF8h-FFF9h	
2	CSS	Clock Filter Interrupt	CRSR			FFF6h-FFF7h
3	SPI	SPI Peripheral Interrupts	SPISR		no	FFF4h-FFF5h
4	TIMER A	TIMER A Peripheral Interrupts	TASR			FFF2h-FFF3h
5		Not used				FFF0h-FFF1h
6	TIMER B	TIMER B Peripheral Interrupts	TBSR		no	FFEEh-FFE Fh
7		Not used				FFECh-FFEDh
8		Not used				FFEAh-FFEBh
9		Not used				FFE8h-FFE9h
10		Not used				FFE6h-FFE7h
11	I C	I C Peripheral Interrupt	I2CSRx	no	FFE4h-FFE5h	
12		Not Used			FFE2h-FFE3h	
13		Not Used			FFE0h-FFE1h	

Note

1. Configurable by option byte.

## 8 POWER SAVING MODES

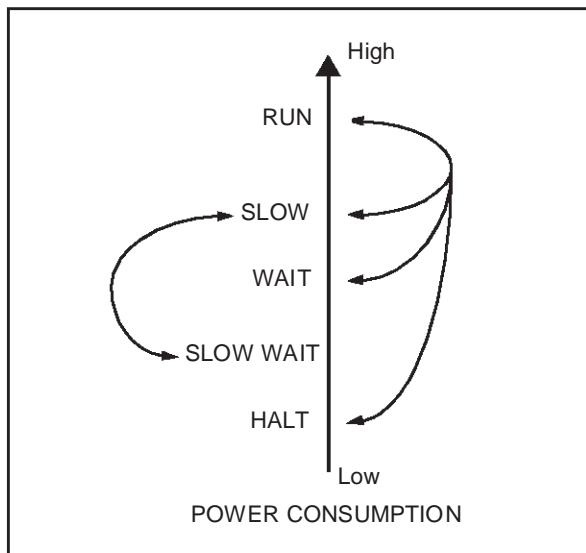
### 8.1 INTRODUCTION

To give a large measure of flexibility to the application in terms of power consumption, three main power saving modes are implemented in the ST7 (see Figure 16).

After a RESET the normal operating mode is selected by default (RUN mode). This mode drives the device (CPU and embedded peripherals) by means of a master clock which is based on the main oscillator frequency divided by 2 ( $f_{CPU}$ ).

From Run mode, the different power saving modes may be selected by setting the relevant register bits or by calling the specific ST7 software instruction whose action depends on the the oscillator status.

Figure 16. Power Saving Mode Transitions



### 8.2 SLOW MODE

This mode has two targets:

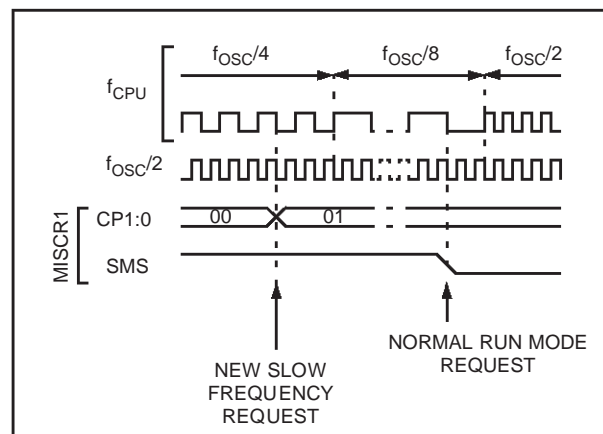
- To reduce power consumption by decreasing the internal clock in the device,
- To adapt the internal clock frequency ( $f_{CPU}$ ) to the available supply voltage.

SLOW mode is controlled by three bits in the MISCR1 register: the SMS bit which enables or disables Slow mode and two CPx bits which select the internal slow frequency ( $f_{CPU}$ ).

In this mode, the oscillator frequency can be divided by 4, 8, 16 or 32 instead of 2 in normal operating mode. The CPU and peripherals are clocked at this lower frequency.

**Note:** SLOW-WAIT mode is activated when entering the WAIT mode while the device is already in SLOW mode.

Figure 17. SLOW Mode Clock Transitions

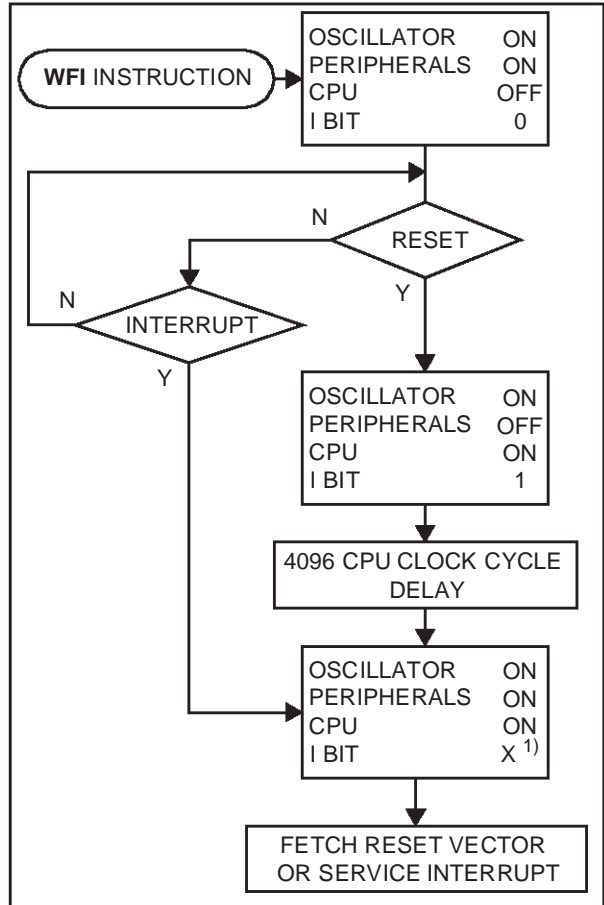


POWER SAVING MODES (Cont'd)

8.3 WAIT MODE

WAIT mode places the MCU in a low power consumption mode by stopping the CPU. This power saving mode is selected by calling the "WFI" ST7 software instruction. All peripherals remain active. During WAIT mode, the I bit of the CC register is forced to 0, to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in WAIT mode until an interrupt or Reset occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine. The MCU will remain in WAIT mode until a Reset or an Interrupt occurs, causing it to wake up. Refer to Figure 18.

Figure 18. WAIT Mode Flow-chart



Note:

1. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

**POWER SAVING MODES (Cont'd)**

**8.4 HALT MODE**

The HALT mode is the lowest power consumption mode of the MCU. It is entered by executing the ST7 HALT instruction (see Figure 20).

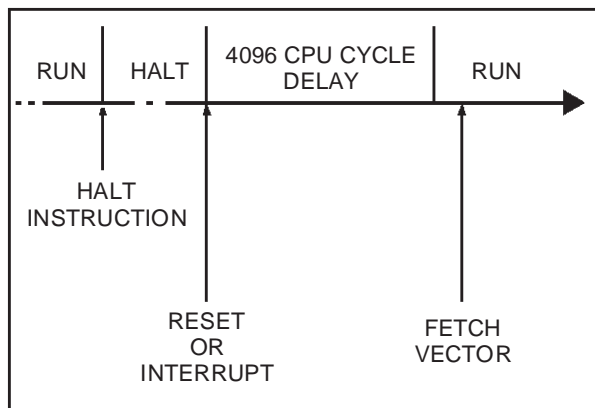
The MCU can exit HALT mode on reception of either a specific interrupt (see Table 5, "Interrupt Mapping," on page 26) or a RESET. When exiting HALT mode by means of a RESET or an interrupt, the oscillator is immediately turned on and the 4096 CPU cycle delay is used to stabilize the oscillator. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see Figure 19).

When entering HALT mode, the I bit in the CC register is forced to 0 to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes immediately.

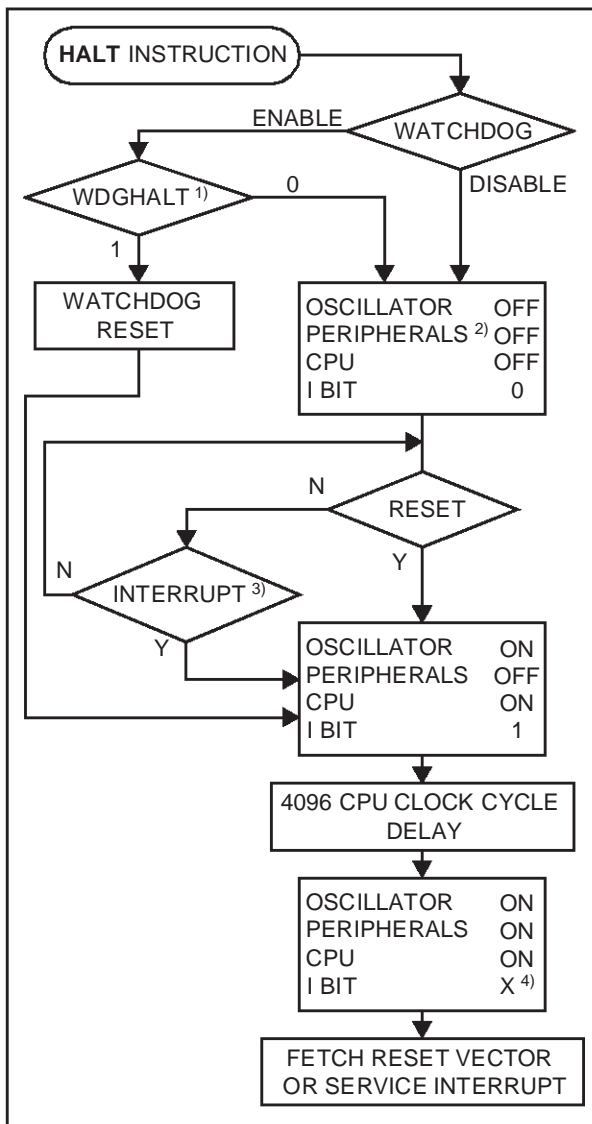
In the HALT mode the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of Watchdog operation with HALT mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the Watchdog system is enabled, can generate a Watchdog RESET (see Section 15.1 "OPTION BYTES" on page 129 for more details).

**Figure 19. HALT Mode Timing Overview**



**Figure 20. HALT Mode Flow-chart**



**Notes:**

1. WDGHALT is an option bit. See option byte section for more details.
2. Peripheral clocked with an external clock source can still be active.
3. Only some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 5, "Interrupt Mapping," on page 26 for more details.
4. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

## 9 I/O PORTS

### 9.1 INTRODUCTION

The I/O ports offer different functional modes:  
 – transfer of data through digital inputs and outputs and for specific pins:  
 – external interrupt generation  
 – alternate signal input/output for the on-chip peripherals.

An I/O port contains up to 8 pins. Each pin can be programmed independently as digital input (with or without interrupt generation) or digital output.

### 9.2 FUNCTIONAL DESCRIPTION

Each port has 2 main registers:

- Data Register (DR)
  - Data Direction Register (DDR)
- and one optional register:
- Option Register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR and OR registers: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

The following description takes into account the OR register, (for specific ports which do not provide this register refer to the I/O Port Implementation section). The generic I/O block diagram is shown in Figure 21

#### 9.2.1 Input Modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Different input modes can be selected by software through the OR register.

**Notes:**

1. Writing the DR register modifies the latch value but does not affect the pin status.
2. When switching from input to output mode, the DR register has to be written first to drive the correct level on the pin as soon as the port is configured as an output.

#### External interrupt function

When an I/O is configured as Input with Interrupt, an event on this I/O can generate an external interrupt request to the CPU.

Each pin can independently generate an interrupt request. The interrupt sensitivity is independently

programmable using the sensitivity bits in the Miscellaneous register.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see pinout description and interrupt section). If several input pins are selected simultaneously as interrupt source, these are logically ANDed. For this reason if one of the interrupt pins is tied low, it masks the other ones.

In case of a floating input with interrupt configuration, special care must be taken when changing the configuration (see Figure 22).

The external interrupts are hardware interrupts, which means that the request latch (not accessible directly by the application) is automatically cleared when the corresponding interrupt vector is fetched. To clear an unwanted pending interrupt by software, the sensitivity bits in the Miscellaneous register must be modified.

#### 9.2.2 Output Modes

The output configuration is selected by setting the corresponding DDR register bit. In this case, writing the DR register applies this digital value to the I/O pin through the latch. Then reading the DR register returns the previously stored value.

Two different output modes can be selected by software through the OR register: Output push-pull and open-drain.

DR register value and output pin status:

DR	Push-pull	Open-drain
0	V <sub>SS</sub>	V <sub>SS</sub>
1	V <sub>DD</sub>	Floating

#### 9.2.3 Alternate Functions

When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over the standard I/O programming.

When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).

When the signal is going to an on-chip peripheral, the I/O pin must be configured in input mode. In this case, the pin state is also digitally readable by addressing the DR register.

**Note:** Input pull-up configuration can cause unexpected value at the input of the alternate peripheral input. When an on-chip peripheral use a pin as input and output, this pin has to be configured in input floating mode.

I/O PORTS (Cont'd)

Figure 21. I/O Port General Block Diagram

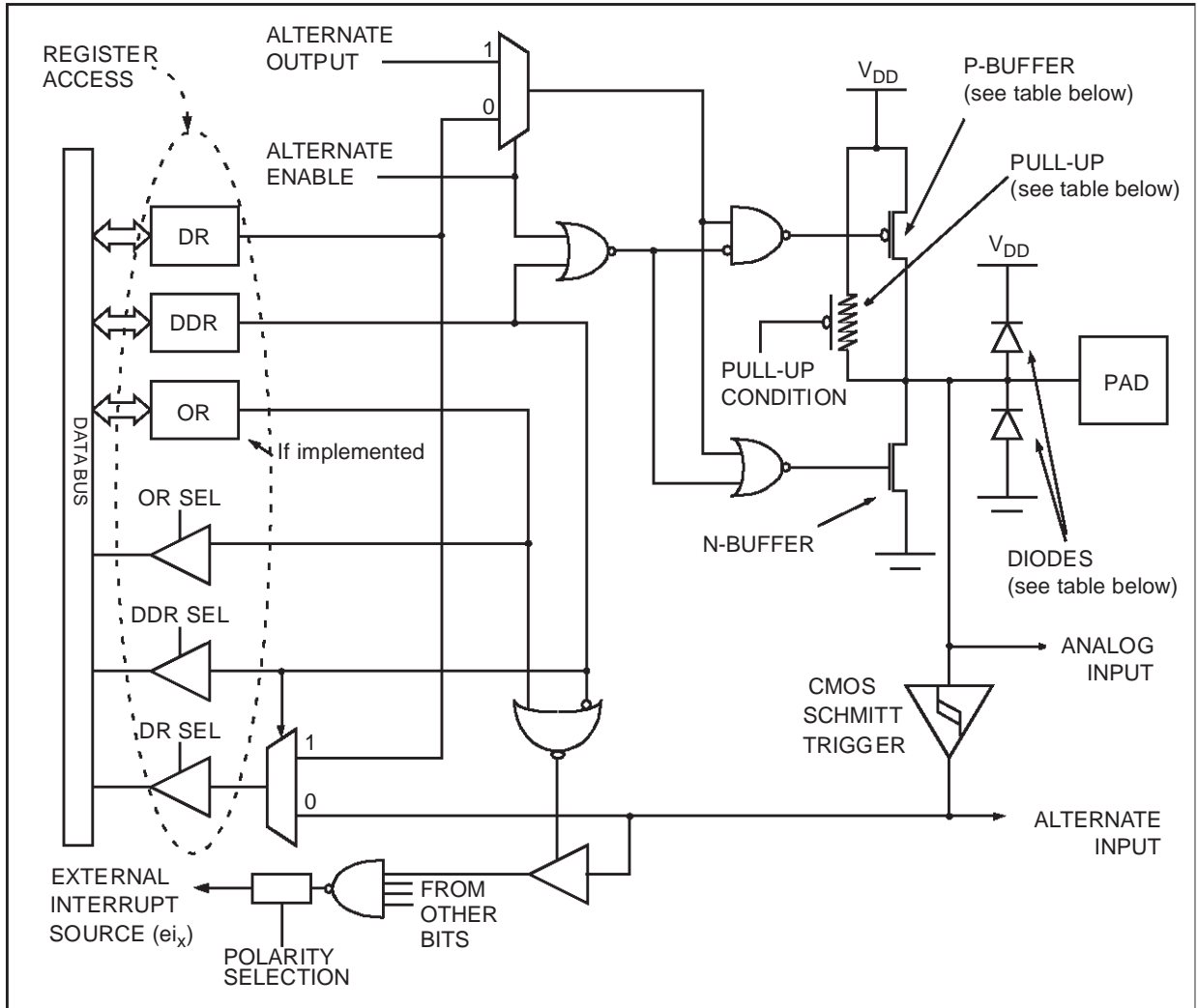


Table 6. I/O Port Mode Options

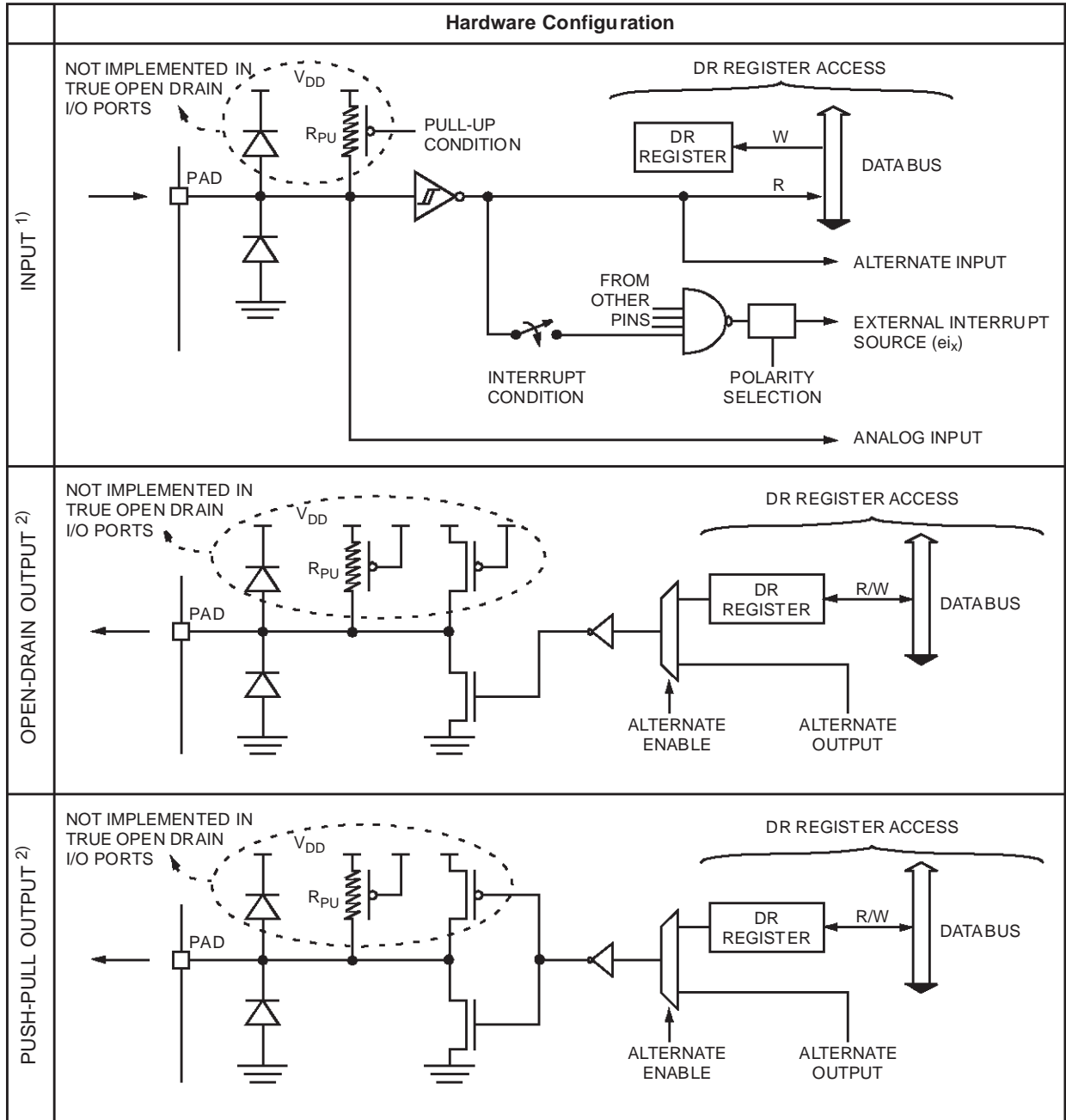
Configuration Mode		Pull-Up	P-Buffer	Diodes	
				to V <sub>DD</sub>	to V <sub>SS</sub>
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On	Off		
Output	Push-pull	Off	On	NI (see note)	On
	Open Drain (logic level)		Off		
	True Open Drain	NI	NI		

**Legend:** NI - not implemented  
 Off - implemented not activated  
 On - implemented and activated

**Note:** The diode to V<sub>DD</sub> is not implemented in the true open drain pads. A local protection between the pad and V<sub>SS</sub> is implemented to protect the device against positive stress.

I/O PORTS (Cont'd)

Table 7. I/O Port Configurations



Notes:

1. When the I/O port is in input configuration and the associated alternate function is enabled as an output, reading the DR register will read the alternate function output status.
2. When the I/O port is in output configuration and the associated alternate function is enabled as an input, the alternate function reads the pin status given by the DR register content.



**I/O PORTS** (Cont'd)

**CAUTION:** The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

**Analog alternate function**

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

It is recommended not to change the voltage level or loading on any port pin while conversion is in progress. Furthermore it is recommended not to have clocking pins located close to a selected analog pin.

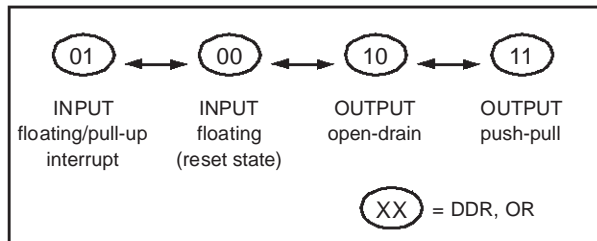
**WARNING:** The analog input voltage level must be within the limits stated in the absolute maximum ratings.

**9.3 I/O PORT IMPLEMENTATION**

The hardware implementation on each I/O port depends on the settings in the DDR and OR registers and specific feature of the I/O port such as ADC input or true open drain.

Switching these I/O ports from one state to another should be done in a sequence that prevents unwanted side effects. Recommended safe transitions are illustrated in Figure 22 Other transitions are potentially risky and should be avoided, since they are likely to present unwanted side-effects such as spurious interrupt generation.

**Figure 22. Interrupt I/O Port State Transitions**



The I/O port register configurations are summarized as follows.

**Interrupt Ports**

**PA7, PA5, PA3:0, PB7:0, PC5:0** (with pull-up)

MODE	DDR	OR
floating input	0	0
pull-up interrupt input	0	1
open drain output	1	0
push-pull output	1	1

**True Open Drain Interrupt Ports**

**PA6, PA4** (without pull-up)

MODE	DDR	OR
floating input	0	0
floating interrupt input	0	1
open drain (high sink ports)	1	X

**Table 8. Port Configuration**

Port	Pin name	Input (DDR = 0)		Output (DDR = 1)		High-Sink
		OR = 0	OR = 1	OR = 0	OR = 1	
Port A	PA7	floating	pull-up interrupt	open drain	push-pull	Yes
	PA6	floating	floating interrupt	true open-drain		
	PA5	floating	pull-up interrupt	open drain	push-pull	
	PA4	floating	floating interrupt	true open-drain		
	PA3:0	floating	pull-up interrupt	open drain	push-pull	
Port B	PB7:0	floating	pull-up interrupt	open drain	push-pull	No
Port C	PC7:0	floating	pull-up interrupt	open drain	push-pull	

I/O PORTS (Cont'd)

9.4 LOW POWER MODES

Mode	Description
WAIT	No effect on I/O ports. External interrupts cause the device to exit from WAIT mode.
HALT	No effect on I/O ports. External interrupts cause the device to exit from HALT mode.

9.5 INTERRUPTS

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and the I-bit in the CC register is reset (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
External interrupt on selected external event	-	DDR <sub>x</sub> OR <sub>x</sub>	Yes	Yes

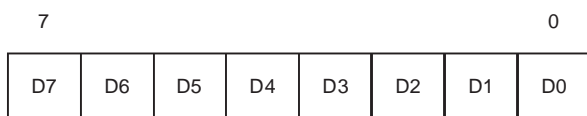
9.6 REGISTER DESCRIPTION

DATA REGISTER (DR)

Port x Data Register  
PxDR with x = A, B or C.

Read/Write

Reset Value: 0000 0000 (00h)



Bit 7:0 = **D[7:0]** Data register 8 bits.

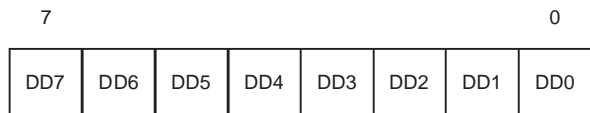
The DR register has a specific behaviour according to the selected input/output configuration. Writing the DR register is always taken into account even if the pin is configured as an input; this allows always having the expected level on the pin when toggling to output mode. Reading the DR register returns either the DR register latch content (pin configured as output) or the digital value applied to the I/O pin (pin configured as input).

DATA DIRECTION REGISTER (DDR)

Port x Data Direction Register  
PxDDR with x = A, B or C.

Read/Write

Reset Value: 0000 0000 (00h)



Bit 7:0 = **DD[7:0]** Data direction register 8 bits.

The DDR register gives the input/output direction configuration of the pins. Each bit is set and cleared by software.

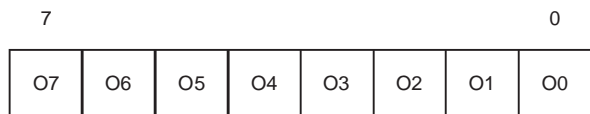
0: Input mode  
1: Output mode

OPTION REGISTER (OR)

Port x Option Register  
PxOR with x = A, B or C.

Read/Write

Reset Value: 0000 0000 (00h)



Bit 7:0 = **O[7:0]** Option register 8 bits.

For specific I/O pins, this register is not implemented. In this case the DDR register is enough to select the I/O pin configuration.

The OR register allows to distinguish: in input mode if the pull-up with interrupt capability or the basic pull-up configuration is selected, in output mode if the push-pull or open drain configuration is selected.

Each bit is set and cleared by software.

Input mode:

0: Floating input  
1: Pull-up input with or without interrupt

Output mode:

0: Output open drain (with P-Buffer unactivated)  
1: Output push-pull (when available)

## I/O PORTS (Cont'd)

Table 9. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Reset Value of all I/O port registers		0	0	0	0	0	0	0	0
0000h	PCDR	MSB							LSB
0001h	PCDDR								
0002h	PCOR								
0004h	PBDR	MSB							LSB
0005h	PBDDR								
0006h	PBOR								
0008h	PADR	MSB							LSB
0009h	PADDR								
000Ah	PAOR								

## 10 MISCELLANEOUS REGISTERS

The miscellaneous registers allow control over several different features such as the external interrupts or the I/O alternate functions.

### 10.1 I/O PORT INTERRUPT SENSITIVITY

The external interrupt sensitivity is controlled by the ISxx bits of the Miscellaneous register and the OPTION BYTE. This control allows having two fully independent external interrupt source sensitivities with configurable sources (using EXTIT option bit) as shown in Figure 23 and Figure 24.

Each external interrupt source can be generated on four different events on the pin:

- Falling edge
- Rising edge
- Falling and rising edge
- Falling edge and low level

To guarantee correct functionality, the sensitivity bits in the MISCR1 register must be modified only when the I bit of the CC register is set to 1 (interrupt masked). See I/O port register and Miscellaneous register descriptions for more details on the programming.

### 10.2 I/O PORT ALTERNATE FUNCTIONS

The MISCR registers manage four I/O port miscellaneous alternate functions:

- Main clock signal ( $f_{CPU}$ ) output on PC2
- SPI pin configuration:
  - $\overline{SS}$  pin internal control to use the PB7 I/O port function while the SPI is active.
  - Master output capability on MOSI pin (PB4) deactivated while the SPI is active.
  - Slave output capability on MISO pin (PB5) deactivated while the SPI is active.

These functions are described in detail in the Section 10.3 "MISCELLANEOUS REGISTER DESCRIPTION" on page 37.

Figure 23. Ext. Interrupt Sensitivity (EXTIT=0)

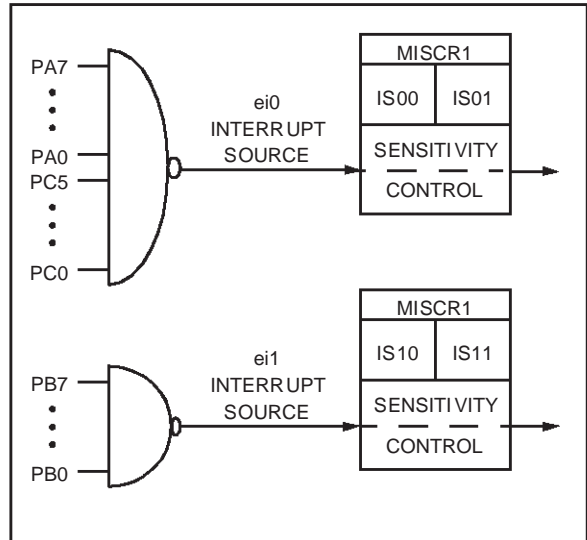
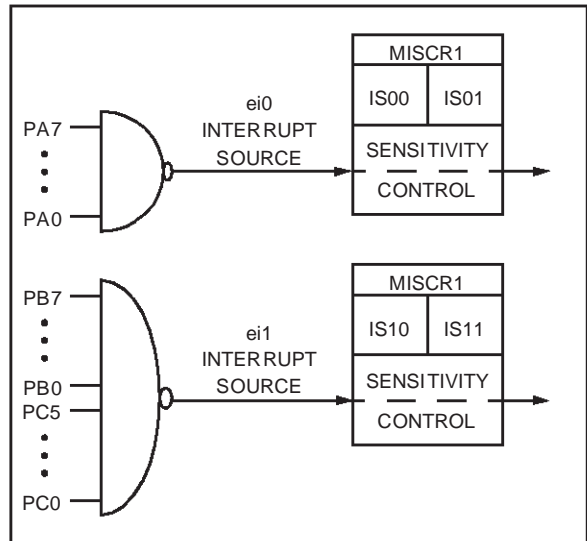


Figure 24. Ext. Interrupt Sensitivity (EXTIT=1)



MISCELLANEOUS REGISTERS (Cont'd)

10.3 MISCELLANEOUS REGISTER DESCRIPTION

MISCELLANEOUS REGISTER 1 (MISCR1)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
IS11	IS10	MCO	IS01	IS00	CP1	CP0	SMS

Bit 7:6 = **IS1[1:0]** *ei1 sensitivity*

The interrupt sensitivity, defined using the IS1[1:0] bits, is applied to the ei1 external interrupts. These two bits can be written only when the I bit of the CC register is set to 1 (interrupt masked).

ei1: Port B (C optional)

External Interrupt Sensitivity	IS11	IS10
Falling edge & low level	0	0
Rising edge only	0	1
Falling edge only	1	0
Rising and falling edge	1	1

Bit 5 = **MCO** *Main clock out selection*

This bit enables the MCO alternate function on the PC2 I/O port. It is set and cleared by software.

0: MCO alternate function disabled (I/O pin free for general-purpose I/O)

1: MCO alternate function enabled ( $f_{CPU}$  on I/O port)

Bit 4:3 = **IS0[1:0]** *ei0 sensitivity*

The interrupt sensitivity, defined using the IS0[1:0] bits, is applied to the ei0 external interrupts. These two bits can be written only when the I bit of the CC register is set to 1 (interrupt masked).

ei0: Port A (C optional)

External Interrupt Sensitivity	IS01	IS00
Falling edge & low level	0	0
Rising edge only	0	1
Falling edge only	1	0
Rising and falling edge	1	1

Bit 2:1 = **CP[1:0]** *CPU clock prescaler*

These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software

$f_{CPU}$ in SLOW mode	CP1	CP0
$f_{OSC} / 4$	0	0
$f_{OSC} / 8$	1	0
$f_{OSC} / 16$	0	1
$f_{OSC} / 32$	1	1

Bit 0 = **SMS** *Slow mode select*

This bit is set and cleared by software.

0: Normal mode.  $f_{CPU} = f_{OSC} / 2$

1: Slow mode.  $f_{CPU}$  is given by CP1, CP0

See low power consumption mode and MCC chapters for more details.

**MISCELLANEOUS REGISTERS (Cont'd)**

**MISCELLANEOUS REGISTER 2 (MISCR2)**

Read/Write

Reset Value: 0000 0000 (00h)

				MOD	SOD	SSM	SSI		
0	0	0	0						

Bit 7:4 = **Reserved** *always read as 0*

Bit 5 = **MOD SPI Master Output Disable**  
 This bit is set and cleared by software. When set, it disables the SPI Master (MOSI) output signal.  
 0: SPI Master Output enabled.  
 1: SPI Master Output disabled.

Bit 4 = **SOD SPI Slave Output Disable**  
 This bit is set and cleared by software. When set it disable the SPI Slave (MISO) output signal.  
 0: SPI Slave Output enabled.  
 1: SPI Slave Output disabled.

Bit 1 = **SSM  $\overline{SS}$  mode selection**  
 This bit is set and cleared by software.  
 0: Normal mode - the level of the SPI  $\overline{SS}$  signal is input from the external  $\overline{SS}$  pin.  
 1: I/O mode, the level of the SPI  $\overline{SS}$  signal is read from the SSI bit.

Bit 0 = **SSI  $\overline{SS}$  internal mode**  
 This bit replaces the  $\overline{SS}$  pin of the SPI when the SSM bit is set to 1. (see SPI description). It is set and cleared by software.

**Table 10. Miscellaneous Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0020h	<b>MISCR1</b> Reset Value	IS11 0	IS10 0	MCO 0	IS01 0	IS00 0	CP1 0	CP0 0	SMS 0
0040h	<b>MISCR2</b> Reset Value	0	0	0	0	MOD 0	SOD 0	SSM 0	SSI 0

## 11 ON-CHIP PERIPHERALS

### 11.1 WATCHDOG TIMER (WDG)

#### 11.1.1 Introduction

The Watchdog timer is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before the T6 bit becomes cleared.

#### 11.1.2 Main Features

- Programmable timer (64 increments of 12288 CPU cycles)
- Programmable reset
- Reset (if watchdog activated) when the T6 bit reaches zero
- Optional reset on HALT instruction (configurable by option byte)
- Hardware Watchdog selectable by option byte.

#### 11.1.3 Functional Description

The counter value stored in the CR register (bits T6:T0), is decremented every 12,288 machine cy-

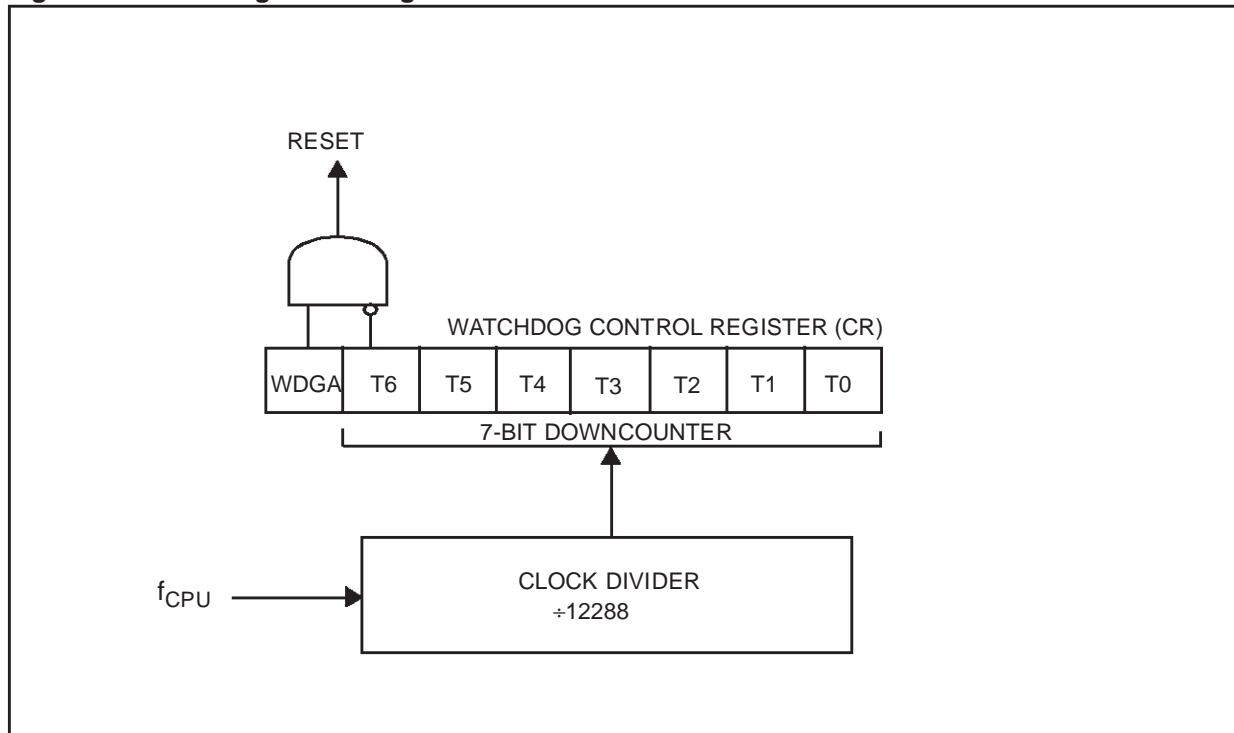
cles, and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T6:T0) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 500ns.

The application program must write in the CR register at regular intervals during normal operation to prevent an MCU reset. The value to be stored in the CR register must be between FFh and C0h (see Table 11 . Watchdog Timing (fCPU = 8 MHz)):

- The WDGA bit is set (watchdog enabled)
- The T6 bit is set to prevent generating an immediate reset
- The T5:T0 bits contain the number of increments which represents the time delay before the watchdog produces a reset.

Figure 25. Watchdog Block Diagram



WATCHDOG TIMER (Cont'd)

Table 11. Watchdog Timing (f<sub>CPU</sub> = 8 MHz)

	CR Register initial value	WDG timeout period (ms)
Max	FFh	98.304
Min	C0h	1.536

**Notes:** Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

11.1.4 Hardware Watchdog Option

If Hardware Watchdog is selected by option byte, the watchdog is always active and the WDGA bit in the CR is not used.

Refer to the device-specific Option Byte description.

11.1.5 Low Power Modes

WAIT Instruction

No effect on Watchdog.

HALT Instruction

If the Watchdog reset on HALT option is selected by option byte, a HALT instruction causes an immediate reset generation if the Watchdog is activated (WDGA bit is set).

11.1.5.1 Using Halt Mode with the WDG (option)

If the Watchdog reset on HALT option is not selected by option byte, the Halt mode can be used when the watchdog is enabled.

In this case, the HALT instruction stops the oscillator. When the oscillator is stopped, the WDG stops counting and is no longer able to generate a reset until the microcontroller receives an external interrupt or a reset.

If an external interrupt is received, the WDG restarts counting after 4096 CPU clocks. If a reset is generated, the WDG is disabled (reset state).

Recommendations

- Make sure that an external event is available to wake up the microcontroller from Halt mode.
- Before executing the HALT instruction, refresh the WDG counter, to avoid an unexpected WDG

reset immediately after waking up the microcontroller.

- When using an external interrupt to wake up the microcontroller, reinitialize the corresponding I/O as “Input Pull-up with Interrupt” before executing the HALT instruction. The main reason for this is that the I/O may be wrongly configured due to external interference or by an unforeseen logical condition.
- For the same reason, reinitialize the level sensitivity of each external interrupt as a precautionary measure.
- The opcode for the HALT instruction is 0x8E. To avoid an unexpected HALT instruction due to a program counter failure, it is advised to clear all occurrences of the data value 0x8E from memory. For example, avoid defining a constant in ROM with the value 0x8E.
- As the HALT instruction clears the I bit in the CC register to allow interrupts, the user may choose to clear all pending interrupt bits before executing the HALT instruction. This avoids entering other peripheral interrupt routines after executing the external interrupt routine corresponding to the wake-up event (reset or external interrupt).

11.1.6 Interrupts

None.

11.1.7 Register Description

CONTROL REGISTER (CR)

Read/Write

Reset Value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0

Bit 7 = **WDGA** Activation bit.

This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset.

0: Watchdog disabled

1: Watchdog enabled

Bit 6:0 = **T[6:0]** 7-bit timer (MSB to LSB).

These bits contain the decremented value. A reset is produced when it rolls over from 40h to 3Fh (T6 becomes cleared).



## WATCHDOG TIMER (Cond't)

Table 12. Watchdog Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0024h	WDGCR Reset Value	WDGA 0	T6 1	T5 1	T4 1	T3 1	T2 1	T1 1	T0 1

## 11.2 16-BIT TIMER

### 11.2.1 Introduction

The timer consists of a 16-bit free-running counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (*input capture*) or generation of up to two output waveforms (*output compare* and *PWM*).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the CPU clock prescaler.

Some ST7 devices have two on-chip 16-bit timers. They are completely independent, and do not share any resources. They are synchronized after a MCU reset as long as the timer clock frequencies are not modified.

This description covers one or two 16-bit timers. In ST7 devices with two timers, register names are prefixed with TA (Timer A) or TB (Timer B).

### 11.2.2 Main Features

- Programmable prescaler:  $f_{CPU}$  divided by 2, 4 or 8.
- Overflow status flag and maskable interrupt
- External clock input (must be at least 4 times slower than the CPU clock speed) with the choice of active edge
- Output compare functions with
  - 2 dedicated 16-bit registers
  - 2 dedicated programmable signals
  - 2 dedicated status flags
  - 1 dedicated maskable interrupt
- Input capture functions with
  - 2 dedicated 16-bit registers
  - 2 dedicated active edge selection signals
  - 2 dedicated status flags
  - 1 dedicated maskable interrupt
- Pulse width modulation mode (PWM)
- One pulse mode
- 5 alternate functions on I/O ports (ICAP1, ICAP2, OCMP1, OCMP2, EXTCLK)\*

The Block Diagram is shown in Figure 26.

**\*Note:** Some timer pins may not be available (not bonded) in some ST7 devices. Refer to the device pin out description.

When reading an input signal on a non-bonded pin, the value will always be '1'.

### 11.2.3 Functional Description

#### 11.2.3.1 Counter

The main block of the Programmable Timer is a 16-bit free running upcounter and its associated 16-bit registers. The 16-bit registers are made up of two 8-bit registers called high & low.

Counter Register (CR):

- Counter High Register (CHR) is the most significant byte (MS Byte).
- Counter Low Register (CLR) is the least significant byte (LS Byte).

Alternate Counter Register (ACR)

- Alternate Counter High Register (ACHR) is the most significant byte (MS Byte).
- Alternate Counter Low Register (ACLR) is the least significant byte (LS Byte).

These two read-only 16-bit registers contain the same value but with the difference that reading the ACLR register does not clear the TOF bit (Timer overflow flag), located in the Status register, (SR), (see note at the end of paragraph titled 16-bit read sequence).

Writing in the CLR register or ACLR register resets the free running counter to the FFFCh value.

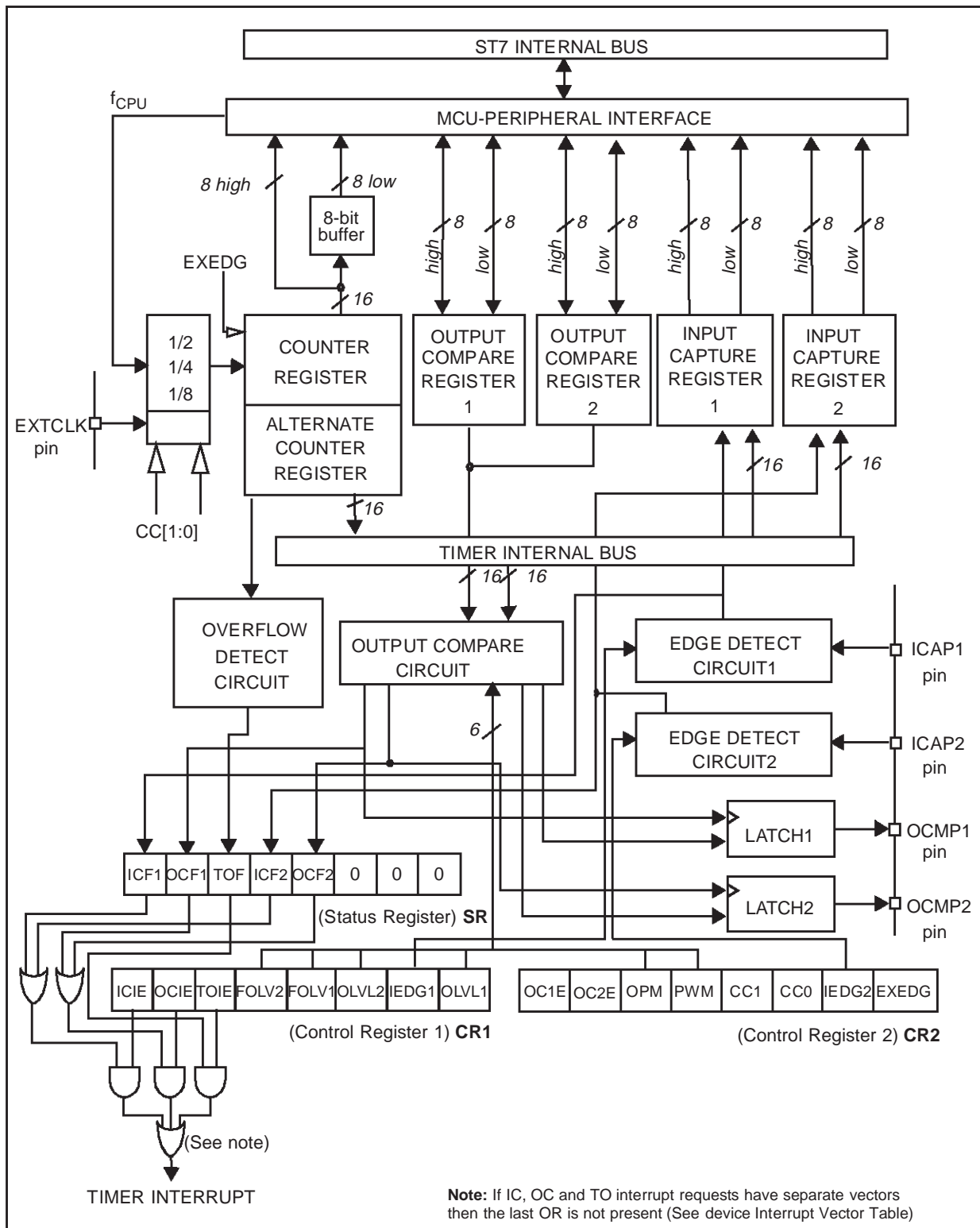
Both counters have a reset value of FFFCh (this is the only value which is reloaded in the 16-bit timer). The reset value of both counters is also FFFCh in One Pulse mode and PWM mode.

The timer clock depends on the clock control bits of the CR2 register, as illustrated in Table 13 Clock Control Bits. The value in the counter register repeats every 131.072, 262.144 or 524.288 CPU clock cycles depending on the CC[1:0] bits.

The timer frequency can be  $f_{CPU}/2$ ,  $f_{CPU}/4$ ,  $f_{CPU}/8$  or an external frequency.

16-BIT TIMER (Cont'd)

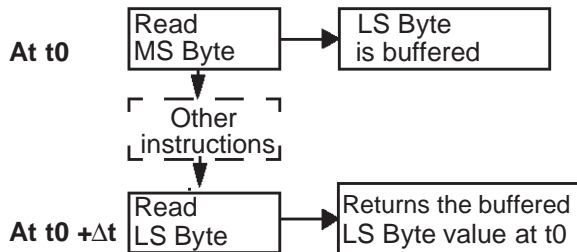
Figure 26. Timer Block Diagram



**16-BIT TIMER** (Cont'd)

**16-bit read sequence:** (from either the Counter Register or the Alternate Counter Register).

*Beginning of the sequence*



*Sequence completed*

The user must read the MS Byte first, then the LS Byte value is buffered automatically.

This buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MS Byte several times.

After a complete reading sequence, if only the CLR register or ACLR register are read, they return the LS Byte of the count value at the time of the read.

Whatever the timer mode used (input capture, output compare, one pulse mode or PWM mode) an overflow occurs when the counter rolls over from FFFFh to 0000h then:

- The TOF bit of the SR register is set.
- A timer interrupt is generated if:
  - TOIE bit of the CR1 register is set and
  - I bit of the CC register is cleared.

If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true.

Clearing the overflow interrupt request is done in two steps:

1. Reading the SR register while the TOF bit is set.
2. An access (read or write) to the CLR register.

**Notes:** The TOF bit is not cleared by accesses to ACLR register. The advantage of accessing the ACLR register rather than the CLR register is that it allows simultaneous use of the overflow function and reading the free running counter at random times (for example, to measure elapsed time) without the risk of clearing the TOF bit erroneously.

The timer is not affected by WAIT mode.

In HALT mode, the counter stops counting until the mode is exited. Counting then resumes from the previous count (MCU awakened by an interrupt) or from the reset count (MCU awakened by a Reset).

**11.2.3.2 External Clock**

The external clock (where available) is selected if CC0=1 and CC1=1 in CR2 register.

The status of the EXEDG bit in the CR2 register determines the type of level transition on the external clock pin EXTCLK that will trigger the free running counter.

The counter is synchronised with the falling edge of the internal CPU clock.

A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

16-BIT TIMER (Cont'd)

Figure 27. Counter Timing Diagram, internal clock divided by 2

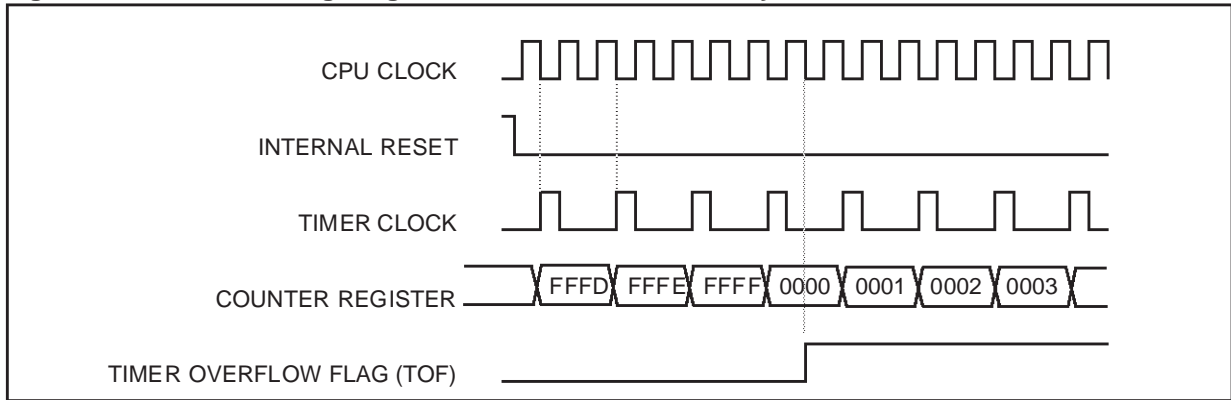


Figure 28. Counter Timing Diagram, internal clock divided by 4

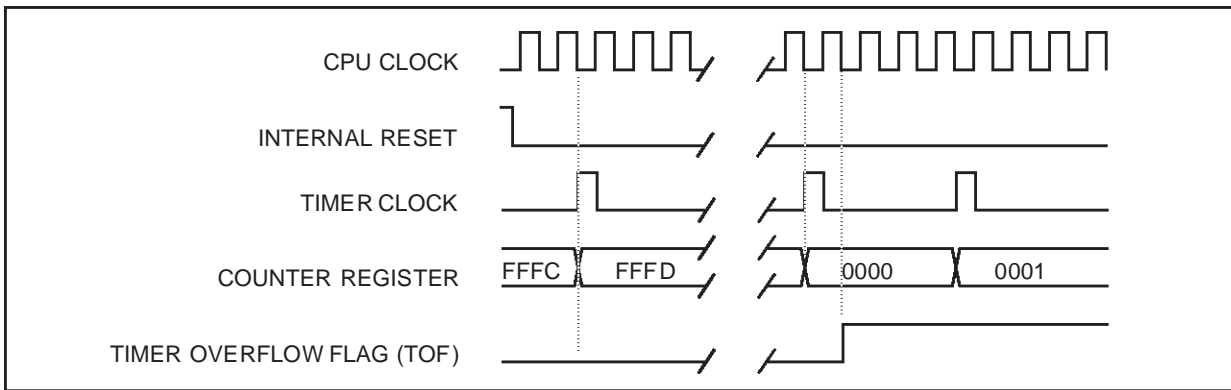
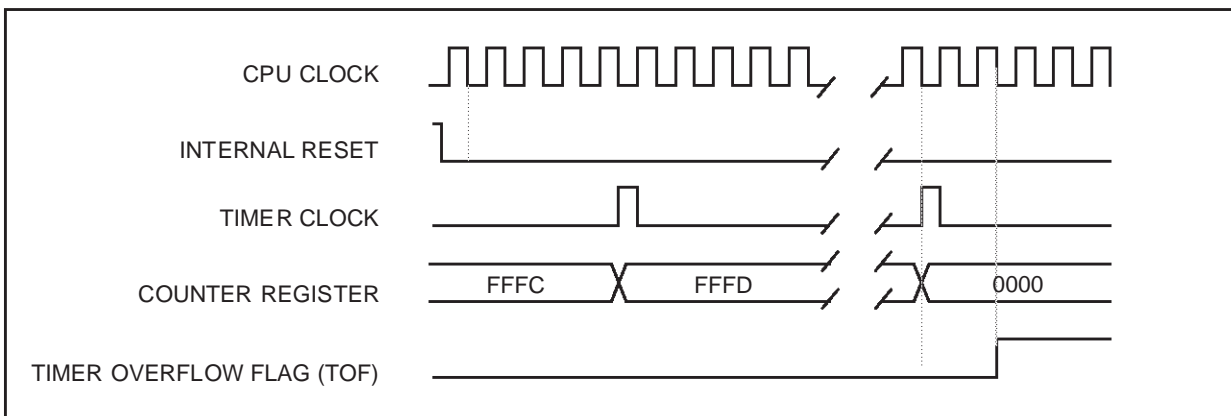


Figure 29. Counter Timing Diagram, internal clock divided by 8



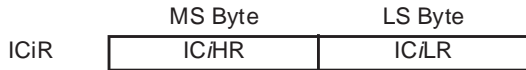
**Note:** The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

**16-BIT TIMER (Cont'd)**

**11.2.3.3 Input Capture**

In this section, the index, *i*, may be 1 or 2 because there are 2 input capture functions in the 16-bit timer.

The two input capture 16-bit registers (IC1R and IC2R) are used to latch the value of the free running counter after a transition detected by the ICAP*i* pin (see figure 5).



ICiR register is a read-only register.

The active transition is software programmable through the IEDG*i* bit of Control Registers (CR*i*).

Timing resolution is one count of the free running counter: (f<sub>CPU</sub>/CC[1:0]).

**Procedure:**

To use the input capture function select the following in the CR2 register:

- Select the timer clock (CC[1:0]) (see Table 13 Clock Control Bits).
- Select the edge of the active transition on the ICAP2 pin with the IEDG2 bit (the ICAP2 pin must be configured as floating input).

And select the following in the CR1 register:

- Set the ICIE bit to generate an interrupt after an input capture coming from either the ICAP1 pin or the ICAP2 pin
- Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).

When an input capture occurs:

- ICF*i* bit is set.
- The ICiR register contains the value of the free running counter on the active transition on the ICAP*i* pin (see Figure 31).
- A timer interrupt is generated if the ICIE bit is set and the I bit is cleared in the CC register. Otherwise, the interrupt remains pending until both conditions become true.

Clearing the Input Capture interrupt request (i.e. clearing the ICF*i* bit) is done in two steps:

1. Reading the SR register while the ICF*i* bit is set.
2. An access (read or write) to the ICiLR register.

**Notes:**

1. After reading the ICiHR register, transfer of input capture data is inhibited and ICF*i* will never be set until the ICiLR register is also read.
2. The ICiR register contains the free running counter value which corresponds to the most recent input capture.
3. The 2 input capture functions can be used together even if the timer also uses the 2 output compare functions.
4. In One pulse Mode and PWM mode only the input capture 2 can be used.
5. The alternate inputs (ICAP1 & ICAP2) are always directly connected to the timer. So any transitions on these pins activate the input capture function.  
Moreover if one of the ICAP*i* pin is configured as an input and the second one as an output, an interrupt can be generated if the user toggle the output pin and if the ICIE bit is set.  
This can be avoided if the input capture function *i* is disabled by reading the ICiHR (see note 1).
6. The TOF bit can be used with interrupt in order to measure event that go beyond the timer range (FFFFh).

16-BIT TIMER (Cont'd)

Figure 30. Input Capture Block Diagram

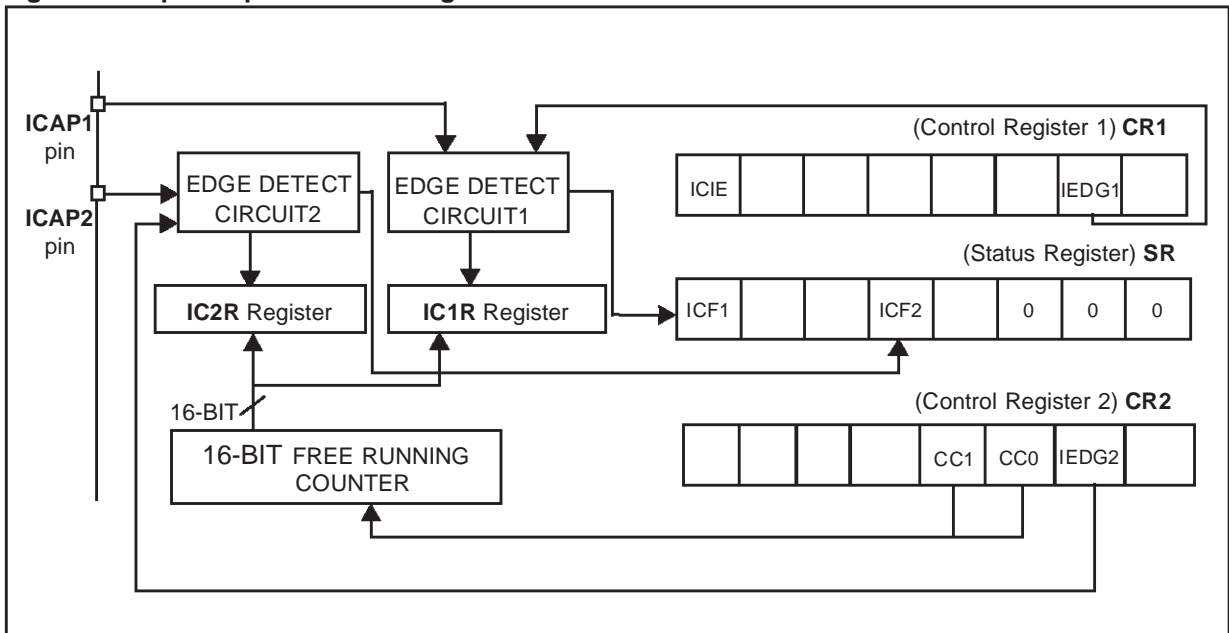
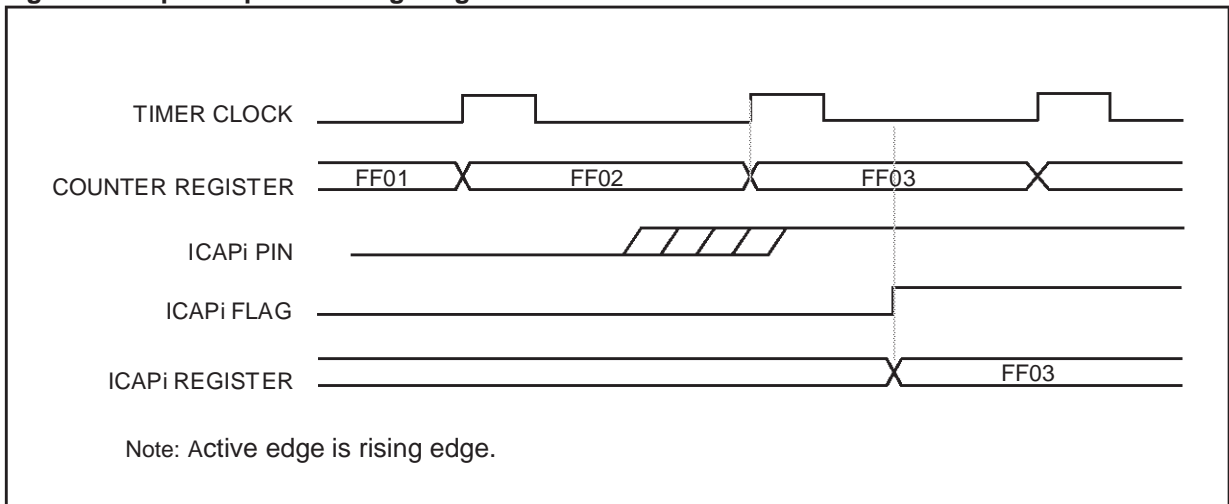


Figure 31. Input Capture Timing Diagram



**16-BIT TIMER (Cont'd)**

**11.2.3.4 Output Compare**

In this section, the index, *i*, may be 1 or 2 because there are 2 output compare functions in the 16-bit timer.

This function can be used to control an output waveform or indicate when a period of time has elapsed.

When a match is found between the Output Compare register and the free running counter, the output compare function:

- Assigns pins with a programmable value if the OCIE bit is set
- Sets a flag in the status register
- Generates an interrupt if enabled

Two 16-bit registers Output Compare Register 1 (OC1R) and Output Compare Register 2 (OC2R) contain the value to be compared to the counter register each timer clock cycle.



These registers are readable and writable and are not affected by the timer hardware. A reset event changes the OC*i*R value to 8000h.

Timing resolution is one count of the free running counter: ( $f_{CPU}/CC[1:0]$ ).

**Procedure:**

To use the output compare function, select the following in the CR2 register:

- Set the OC*i*E bit if an output is needed then the OCMP*i* pin is dedicated to the output compare *i* signal.
- Select the timer clock (CC[1:0]) (see Table 13 Clock Control Bits).

And select the following in the CR1 register:

- Select the OLVL*i* bit to applied to the OCMP*i* pins after the match occurs.
- Set the OCIE bit to generate an interrupt if it is needed.

When a match is found between OCR*i* register and CR register:

- OCF*i* bit is set.

- The OCMP*i* pin takes OLVL*i* bit value (OCMP*i* pin latch is forced low during reset).
- A timer interrupt is generated if the OCIE bit is set in the CR2 register and the I bit is cleared in the CC register (CC).

The OC*i*R register value required for a specific timing application can be calculated using the following formula:

$$\Delta OCiR = \frac{\Delta t * f_{CPU}}{PRESC}$$

Where:

- $\Delta t$  = Output compare period (in seconds)
- $f_{CPU}$  = CPU clock frequency (in hertz)
- PRESC = Timer prescaler factor (2, 4 or 8 depending on CC[1:0] bits, see Table 13 Clock Control Bits)

If the timer clock is an external clock, the formula is:

$$\Delta OCiR = \Delta t * f_{EXT}$$

Where:

- $\Delta t$  = Output compare period (in seconds)
- $f_{EXT}$  = External timer clock frequency (in hertz)

Clearing the output compare interrupt request (i.e. clearing the OCF*i* bit) is done by:

1. Reading the SR register while the OCF*i* bit is set.
2. An access (read or write) to the OC*i*LR register.

The following procedure is recommended to prevent the OCF*i* bit from being set between the time it is read and the write to the OC*i*R register:

- Write to the OC*i*HR register (further compares are inhibited).
- Read the SR register (first step of the clearance of the OCF*i* bit, which may be already set).
- Write to the OC*i*LR register (enables the output compare function and clears the OCF*i* bit).



**16-BIT TIMER (Cont'd)**

**Notes:**

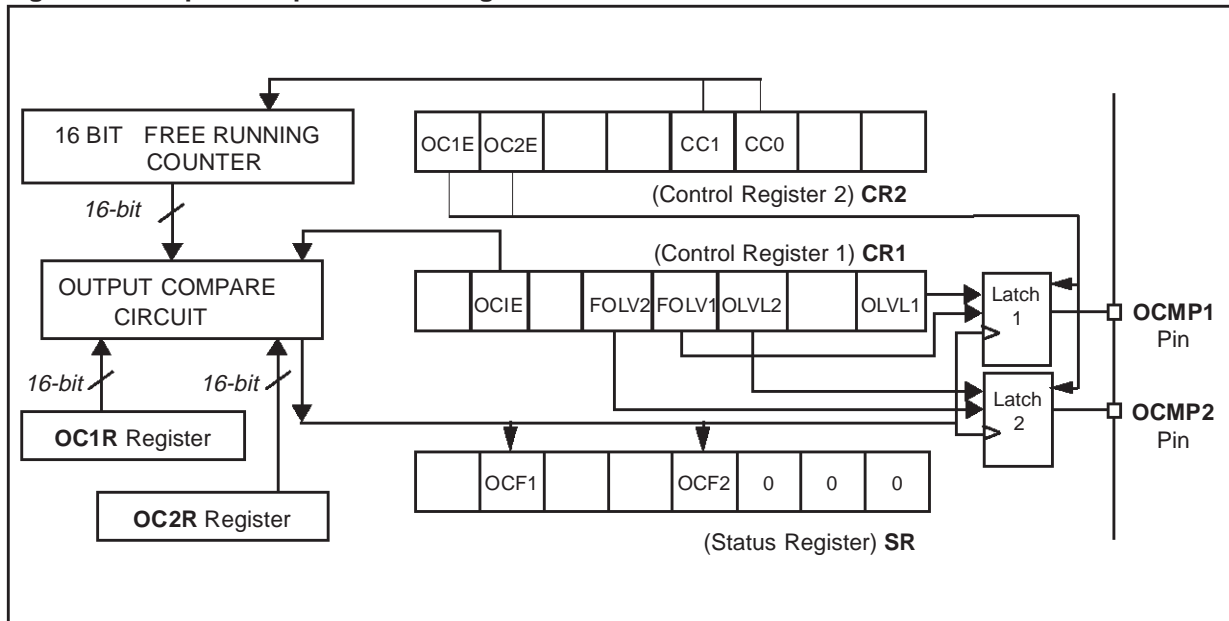
1. After a processor write cycle to the OC*i*HR register, the output compare function is inhibited until the OC*i*LR register is also written.
2. If the OC*i*E bit is not set, the OCMP*i* pin is a general I/O port and the OLV*i* bit will not appear when a match is found but an interrupt could be generated if the OCIE bit is set.
3. When the timer clock is  $f_{CPU}/2$ , OCF*i* and OCMP*i* are set while the counter value equals the OC*i*R register value (see Figure 33 on page 49). This behaviour is the same in OPM or PWM mode.  
When the timer clock is  $f_{CPU}/4$ ,  $f_{CPU}/8$  or in external clock mode, OCF*i* and OCMP*i* are set while the counter value equals the OC*i*R register value plus 1 (see Figure 34 on page 49).
4. The output compare functions can be used both for generating external events on the OCMP*i* pins even if the input capture mode is also used.
5. The value in the 16-bit OC*i*R register and the OLV*i* bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

**Forced Compare Output capability**

When the FOLV*i* bit is set by software, the OLV*i* bit is copied to the OCMP*i* pin. The OLV*i* bit has to be toggled in order to toggle the OCMP*i* pin when it is enabled (OC*i*E bit=1). The OCF*i* bit is then not set by hardware, and thus no interrupt request is generated.

FOLV*i* bits have no effect in both one pulse mode and PWM mode.

**Figure 32. Output Compare Block Diagram**



16-BIT TIMER (Cont'd)

Figure 33. Output Compare Timing Diagram,  $f_{TIMER} = f_{CPU}/2$

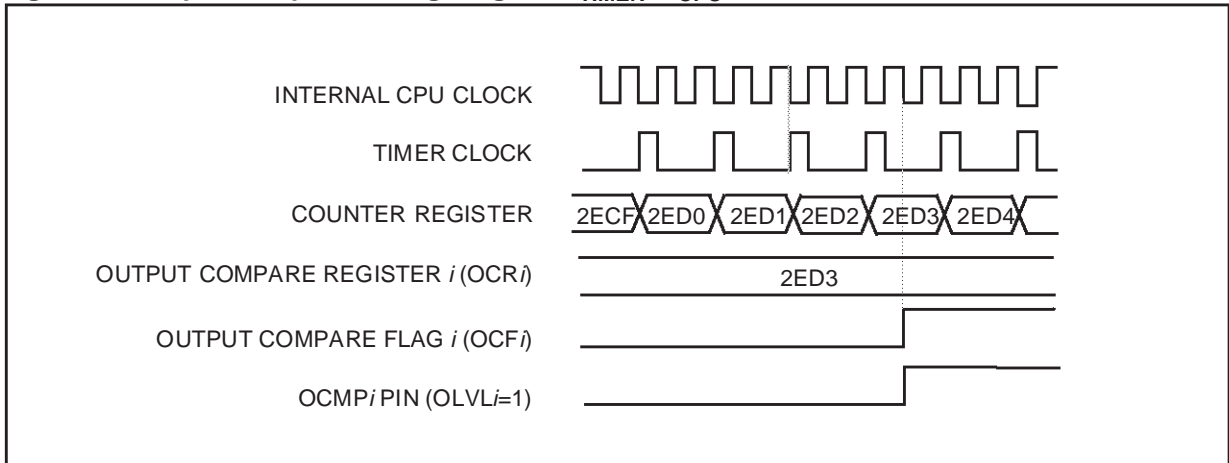
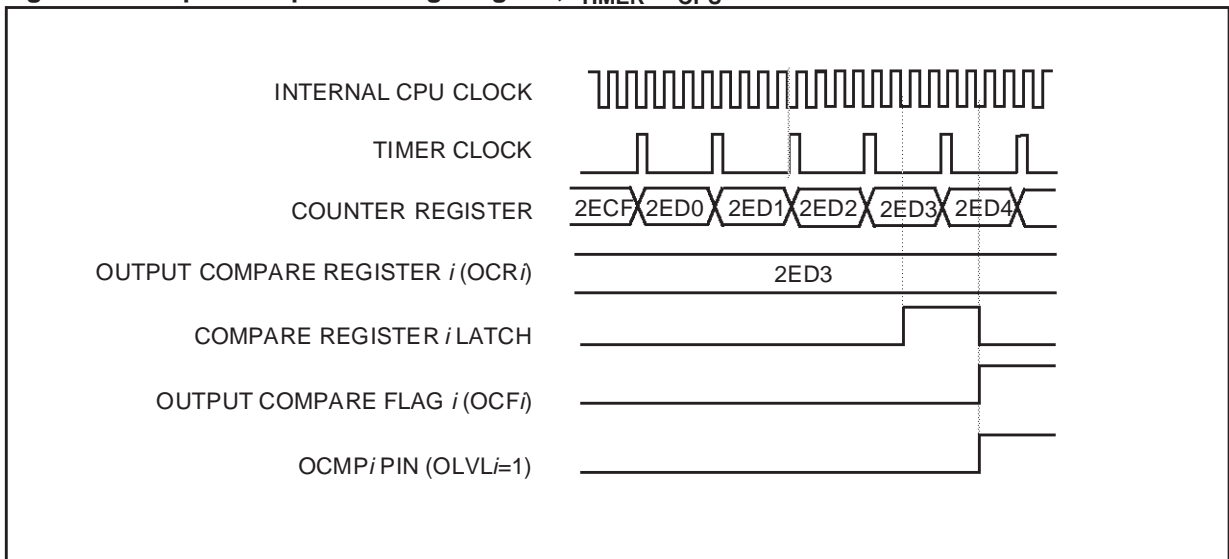


Figure 34. Output Compare Timing Diagram,  $f_{TIMER} = f_{CPU}/4$



**16-BIT TIMER (Cont'd)**

**11.2.3.5 One Pulse Mode**

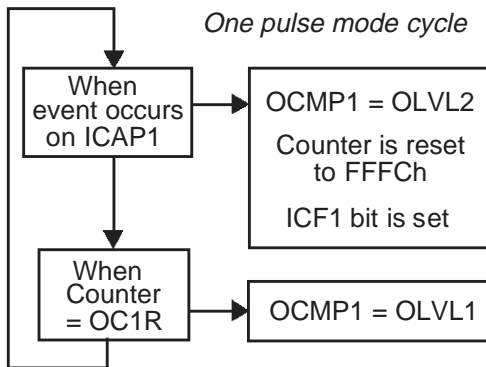
One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the Input Capture1 function and the Output Compare1 function.

**Procedure:**

To use one pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse (see the formula in the opposite column).
2. Select the following in the CR1 register:
  - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.
  - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.
  - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input).
3. Select the following in the CR2 register:
  - Set the OC1E bit, the OCMP1 pin is then dedicated to the Output Compare 1 function.
  - Set the OPM bit.
  - Select the timer clock CC[1:0] (see Table 13 Clock Control Bits).



Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OLVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the Input Capture interrupt request (i.e. clearing the ICFi bit) is done in two steps:

1. Reading the SR register while the ICFi bit is set.
2. An access (read or write) to the ICiLR register.

The OC1R register value required for a specific timing application can be calculated using the following formula:

$$OC1R \text{ Value} = \frac{t * f_{CPU}}{PRESC} - 5$$

Where:

- t = Pulse period (in seconds)
- f<sub>CPU</sub> = CPU clock frequency (in hertz)
- PRESC = Timer prescaler factor (2, 4 or 8 depending on the CC[1:0] bits, see Table 13 Clock Control Bits)

If the timer clock is an external clock the formula is:

$$OC1R = t * f_{EXT} - 5$$

Where:

- t = Pulse period (in seconds)
- f<sub>EXT</sub> = External timer clock frequency (in hertz)

When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (See Figure 35).

**Notes:**

1. The OCF1 bit cannot be set by hardware in one pulse mode but the OCF2 bit can generate an Output Compare interrupt.
2. When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.
3. If OLVL1=OLVL2 a continuous signal will be seen on the OCMP1 pin.
4. The ICAP1 pin can not be used to perform input capture. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each time a valid edge occurs on the ICAP1 pin and ICF1 can also generates interrupt if ICIE is set.
5. When one pulse mode is used OC1R is dedicated to this mode. Nevertheless OC2R and OCF2 can be used to indicate a period of time has been elapsed but cannot generate an output waveform because the level OLVL2 is dedicated to the one pulse mode.

16-BIT TIMER (Cont'd)

Figure 35. One Pulse Mode Timing Example

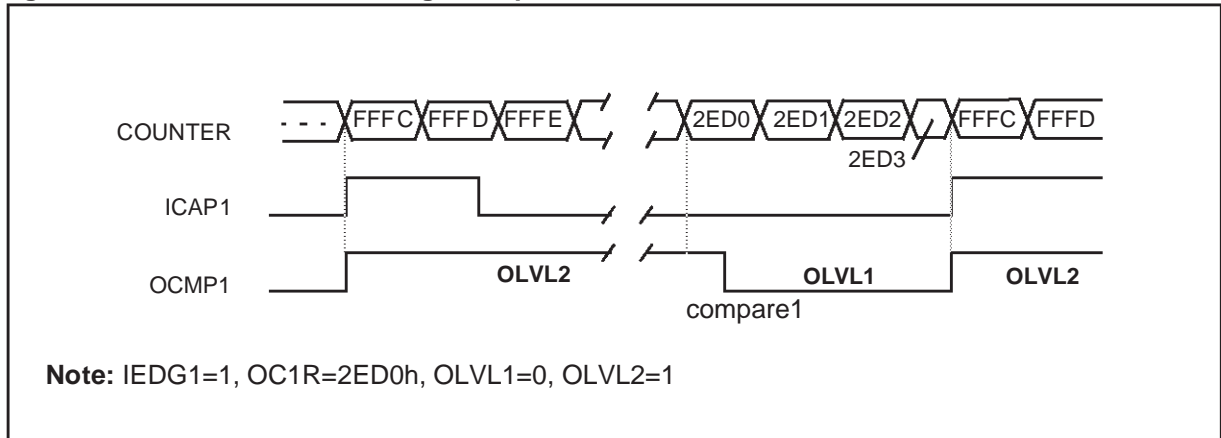
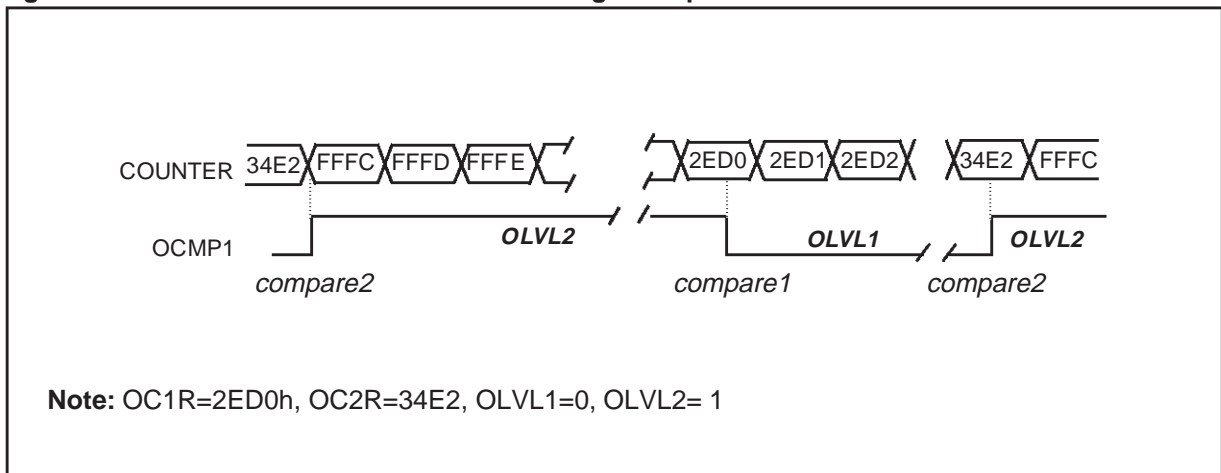


Figure 36. Pulse Width Modulation Mode Timing Example



**16-BIT TIMER (Cont'd)**

**11.2.3.6 Pulse Width Modulation Mode**

Pulse Width Modulation (PWM) mode enables the generation of a signal with a frequency and pulse length determined by the value of the OC1R and OC2R registers.

The pulse width modulation mode uses the complete Output Compare 1 function plus the OC2R register, and so these functionality can not be used when the PWM mode is activated.

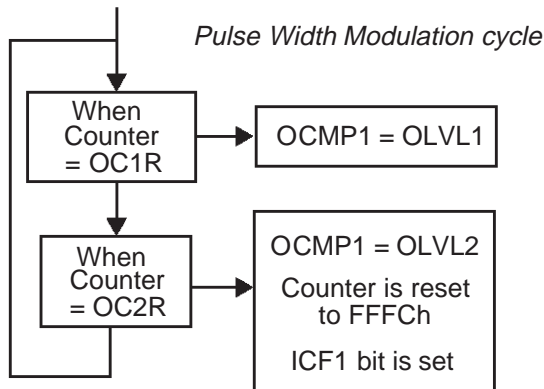
**Procedure**

To use pulse width modulation mode:

1. Load the OC2R register with the value corresponding to the period of the signal using the formula in the opposite column.
2. Load the OC1R register with the value corresponding to the period of the pulse if (OLVL1=0 and OLVL2=1) using the formula in the opposite column.
3. Select the following in the CR1 register:
  - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after a successful comparison with OC1R register.
  - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin after a successful comparison with OC2R register.
4. Select the following in the CR2 register:
  - Set OC1E bit: the OCMP1 pin is then dedicated to the output compare 1 function.
  - Set the PWM bit.
  - Select the timer clock (CC[1:0]) (see Table 13 Clock Control Bits).

If OLVL1=1 and OLVL2=0 the length of the positive pulse is the difference between the OC2R and OC1R registers.

If OLVL1=OLVL2 a continuous signal will be seen on the OCMP1 pin.



The OC*i*R register value required for a specific timing application can be calculated using the following formula:

$$OCiR \text{ Value} = \frac{t * f_{CPU}}{PRESC} - 5$$

Where:

- t = Signal or pulse period (in seconds)
- f<sub>CPU</sub> = CPU clock frequency (in hertz)
- PRESC = Timer prescaler factor (2, 4 or 8 depending on CC[1:0] bits, see Table 13 Clock Control Bits)

If the timer clock is an external clock the formula is:

$$OCiR = t * f_{EXT} - 5$$

Where:

- t = Signal or pulse period (in seconds)
- f<sub>EXT</sub> = External timer clock frequency (in hertz)

The Output Compare 2 event causes the counter to be initialized to FFFCh (See Figure 36)

**Notes:**

1. After a write instruction to the OC*i*HR register, the output compare function is inhibited until the OC*i*LR register is also written.
2. The OCF1 and OCF2 bits cannot be set by hardware in PWM mode therefore the Output Compare interrupt is inhibited.
3. The ICF1 bit is set by hardware when the counter reaches the OC2R value and can produce a timer interrupt if the ICIE bit is set and the I bit is cleared.
4. In PWM mode the ICAP1 pin can not be used to perform input capture because it is disconnected to the timer. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each period and ICF1 can also generates interrupt if ICIE is set.
5. When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.

16-BIT TIMER (Cont'd)

11.2.4 Low Power Modes

Mode	Description
WAIT	No effect on 16-bit Timer. Timer interrupts cause the device to exit from WAIT mode.
HALT	16-bit Timer registers are frozen. In HALT mode, the counter stops counting until Halt mode is exited. Counting resumes from the previous count when the MCU is woken up by an interrupt with "exit from HALT mode" capability or from the counter reset value when the MCU is woken up by a RESET. If an input capture event occurs on the ICAP <sub>i</sub> pin, the input capture detection circuitry is armed. Consequently, when the MCU is woken up by an interrupt with "exit from HALT mode" capability, the ICF <sub>i</sub> bit is set, and the counter value present when exiting from HALT mode is captured into the IC <sub>i</sub> R register.

11.2.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Input Capture 1 event/Counter reset in PWM mode	ICF1	ICIE	Yes	No
Input Capture 2 event	ICF2		Yes	No
Output Compare 1 event (not available in PWM mode)	OCF1	OCIE	Yes	No
Output Compare 2 event (not available in PWM mode)	OCF2		Yes	No
Timer Overflow event	TOF	TOIE	Yes	No

**Note:** The 16-bit Timer interrupt events are connected to the same interrupt vector (see Interrupts chapter). These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

11.2.6 Summary of Timer modes

MODES	AVAILABLE RESOURCES			
	Input Capture 1	Input Capture 2	Output Compare 1	Output Compare 2
Input Capture (1 and/or 2)	Yes	Yes	Yes	Yes
Output Compare (1 and/or 2)	Yes	Yes	Yes	Yes
One Pulse Mode	No	Not Recommended <sup>1)</sup>	No	Partially <sup>2)</sup>
PWM Mode	No	Not Recommended <sup>3)</sup>	No	No

<sup>1)</sup> See note 4 in Section 11.2.3.5 "One Pulse Mode" on page 50

<sup>2)</sup> See note 5 in Section 11.2.3.5 "One Pulse Mode" on page 50

<sup>3)</sup> See note 4 in Section 11.2.3.6 "Pulse Width Modulation Mode" on page 52

**16-BIT TIMER (Cont'd)**

**11.2.7 Register Description**

Each Timer is associated with three control and status registers, and with six pairs of data registers (16-bit values) relating to the two input captures, the two output compares, the counter and the alternate counter.

**CONTROL REGISTER 1 (CR1)**

Read/Write

Reset Value: 0000 0000 (00h)

7	0						
ICIE	OCIE	TOIE	FOLV2	FOLV1	OLVL2	IEDG1	OLVL1

Bit 7 = **ICIE** *Input Capture Interrupt Enable*.  
 0: Interrupt is inhibited.  
 1: A timer interrupt is generated whenever the ICF1 or ICF2 bit of the SR register is set.

Bit 6 = **OCIE** *Output Compare Interrupt Enable*.  
 0: Interrupt is inhibited.  
 1: A timer interrupt is generated whenever the OCF1 or OCF2 bit of the SR register is set.

Bit 5 = **TOIE** *Timer Overflow Interrupt Enable*.  
 0: Interrupt is inhibited.  
 1: A timer interrupt is enabled whenever the TOF bit of the SR register is set.

Bit 4 = **FOLV2** *Forced Output Compare 2*.  
 This bit is set and cleared by software.  
 0: No effect on the OCMP2 pin.  
 1: Forces the OLVL2 bit to be copied to the OCMP2 pin, if the OC2E bit is set and even if there is no successful comparison.

Bit 3 = **FOLV1** *Forced Output Compare 1*.  
 This bit is set and cleared by software.  
 0: No effect on the OCMP1 pin.  
 1: Forces OLVL1 to be copied to the OCMP1 pin, if the OC1E bit is set and even if there is no successful comparison.

Bit 2 = **OLVL2** *Output Level 2*.  
 This bit is copied to the OCMP2 pin whenever a successful comparison occurs with the OC2R register and OCxE is set in the CR2 register. This value is copied to the OCMP1 pin in One Pulse Mode and Pulse Width Modulation mode.

Bit 1 = **IEDG1** *Input Edge 1*.  
 This bit determines which type of level transition on the ICAP1 pin will trigger the capture.  
 0: A falling edge triggers the capture.  
 1: A rising edge triggers the capture.

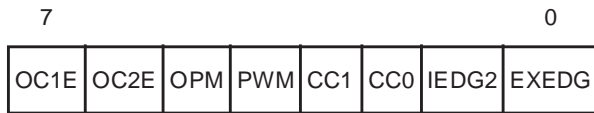
Bit 0 = **OLVL1** *Output Level 1*.  
 The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs with the OC1R register and the OC1E bit is set in the CR2 register.

16-BIT TIMER (Cont'd)

CONTROL REGISTER 2 (CR2)

Read/Write

Reset Value: 0000 0000 (00h)



Bit 7 = **OC1E** *Output Compare 1 Pin Enable*.  
 This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in Output Compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the Output Compare 1 function of the timer remains active.  
 0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O).  
 1: OCMP1 pin alternate function enabled.

Bit 6 = **OC2E** *Output Compare 2 Pin Enable*.  
 This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in Output Compare mode). Whatever the value of the OC2E bit, the Output Compare 2 function of the timer remains active.  
 0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O).  
 1: OCMP2 pin alternate function enabled.

Bit 5 = **OPM** *One Pulse Mode*.  
 0: One Pulse Mode is not active.  
 1: One Pulse Mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.

Bit 4 = **PWM** *Pulse Width Modulation*.  
 0: PWM mode is not active.  
 1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.

Bit 3, 2 = **CC[1:0]** *Clock Control*.  
 The timer clock mode depends on these bits:

Table 13. Clock Control Bits

Timer Clock	CC1	CC0
$f_{CPU} / 4$	0	0
$f_{CPU} / 2$	0	1
$f_{CPU} / 8$	1	0
External Clock (where available)	1	1

**Note:** If the external clock pin is not available, programming the external clock configuration stops the counter.

Bit 1 = **IEDG2** *Input Edge 2*.  
 This bit determines which type of level transition on the ICAP2 pin will trigger the capture.  
 0: A falling edge triggers the capture.  
 1: A rising edge triggers the capture.

Bit 0 = **EXEDG** *External Clock Edge*.  
 This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register.  
 0: A falling edge triggers the counter register.  
 1: A rising edge triggers the counter register.





**16-BIT TIMER (Cont'd)**

**OUTPUT COMPARE 2 HIGH REGISTER (OC2HR)**

Read/Write  
Reset Value: 1000 0000 (80h)

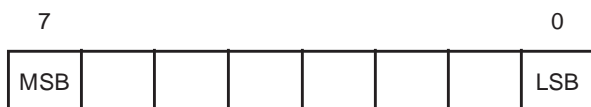
This is an 8-bit register that contains the high part of the value to be compared to the CHR register.



**OUTPUT COMPARE 2 LOW REGISTER (OC2LR)**

Read/Write  
Reset Value: 0000 0000 (00h)

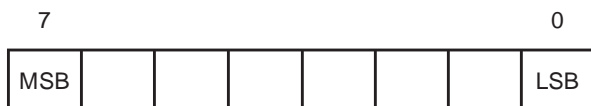
This is an 8-bit register that contains the low part of the value to be compared to the CLR register.



**COUNTER HIGH REGISTER (CHR)**

Read Only  
Reset Value: 1111 1111 (FFh)

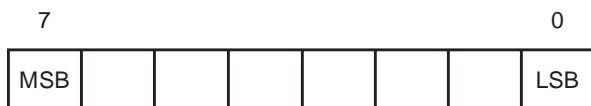
This is an 8-bit register that contains the high part of the counter value.



**COUNTER LOW REGISTER (CLR)**

Read Only  
Reset Value: 1111 1100 (FCh)

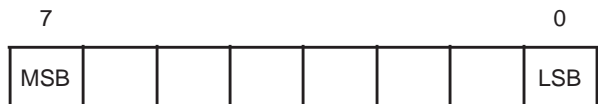
This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after accessing the SR register clears the TOF bit.



**ALTERNATE COUNTER HIGH REGISTER (ACHR)**

Read Only  
Reset Value: 1111 1111 (FFh)

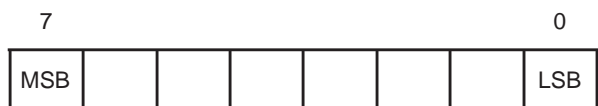
This is an 8-bit register that contains the high part of the counter value.



**ALTERNATE COUNTER LOW REGISTER (ACLRL)**

Read Only  
Reset Value: 1111 1100 (FCh)

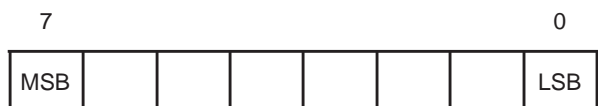
This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to SR register does not clear the TOF bit in SR register.



**INPUT CAPTURE 2 HIGH REGISTER (IC2HR)**

Read Only  
Reset Value: Undefined

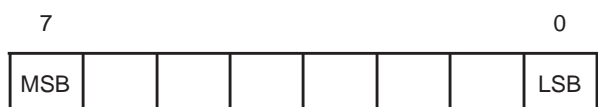
This is an 8-bit read only register that contains the high part of the counter value (transferred by the Input Capture 2 event).



**INPUT CAPTURE 2 LOW REGISTER (IC2LR)**

Read Only  
Reset Value: Undefined

This is an 8-bit read only register that contains the low part of the counter value (transferred by the Input Capture 2 event).



16-BIT TIMER (Cont'd)

Table 14. 16-Bit Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Timer A: 32 Timer B: 42	<b>CR1</b> Reset Value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
Timer A: 31 Timer B: 41	<b>CR2</b> Reset Value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
Timer A: 33 Timer B: 43	<b>SR</b> Reset Value	ICF1 0	OCF1 0	TOF 0	ICF2 0	OCF2 0	- 0	- 0	- 0
Timer A: 34 Timer B: 44	<b>ICHR1</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 35 Timer B: 45	<b>ICLR1</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 36 Timer B: 46	<b>OCHR1</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 37 Timer B: 47	<b>OCLR1</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 3E Timer B: 4E	<b>OCHR2</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 3F Timer B: 4F	<b>OCLR2</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 38 Timer B: 48	<b>CHR</b> Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 39 Timer B: 49	<b>CLR</b> Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3A Timer B: 4A	<b>ACHR</b> Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 3B Timer B: 4B	<b>ACLR</b> Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3C Timer B: 4C	<b>ICHR2</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer A: 3D Timer B: 4D	<b>ICLR2</b> Reset Value	MSB -	-	-	-	-	-	-	LSB -

**11.3 SERIAL PERIPHERAL INTERFACE (SPI)**

**11.3.1 Introduction**

The Serial Peripheral Interface (SPI) allows full-duplex, synchronous, serial communication with external devices. An SPI system may consist of a master and one or more slaves or a system in which devices may be either masters or slaves.

The SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Refer to the Pin Description chapter for the device-specific pin-out.

**11.3.2 Main Features**

- Full duplex, three-wire synchronous transfers
- Master or slave operation
- Four master mode frequencies
- Maximum slave mode frequency = fCPU/2.
- Four programmable master bit rates
- Programmable clock polarity and phase
- End of transfer interrupt flag
- Write collision flag protection
- Master mode fault protection capability.

**11.3.3 General description**

The SPI is connected to external devices through 4 alternate pins:

- MISO: Master In Slave Out pin
- MOSI: Master Out Slave In pin
- SCK: Serial Clock pin
- $\overline{SS}$ : Slave select pin

A basic example of interconnections between a single master and a single slave is illustrated on Figure 37.

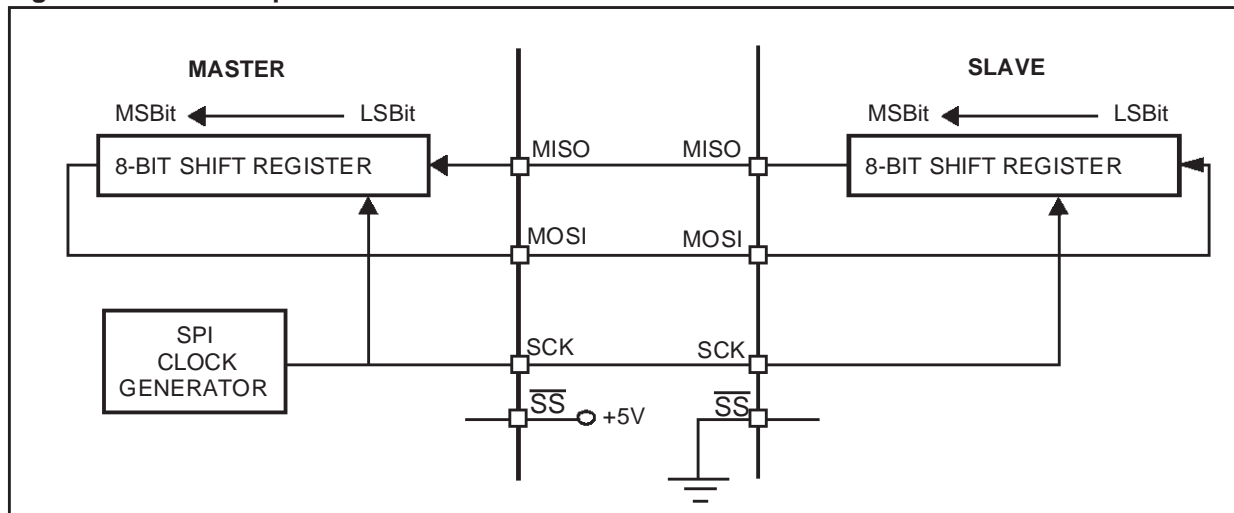
The MOSI pins are connected together as are MISO pins. In this way data is transferred serially between master and slave (most significant bit first).

When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex transmission with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full bits. A status flag is used to indicate that the I/O operation is complete.

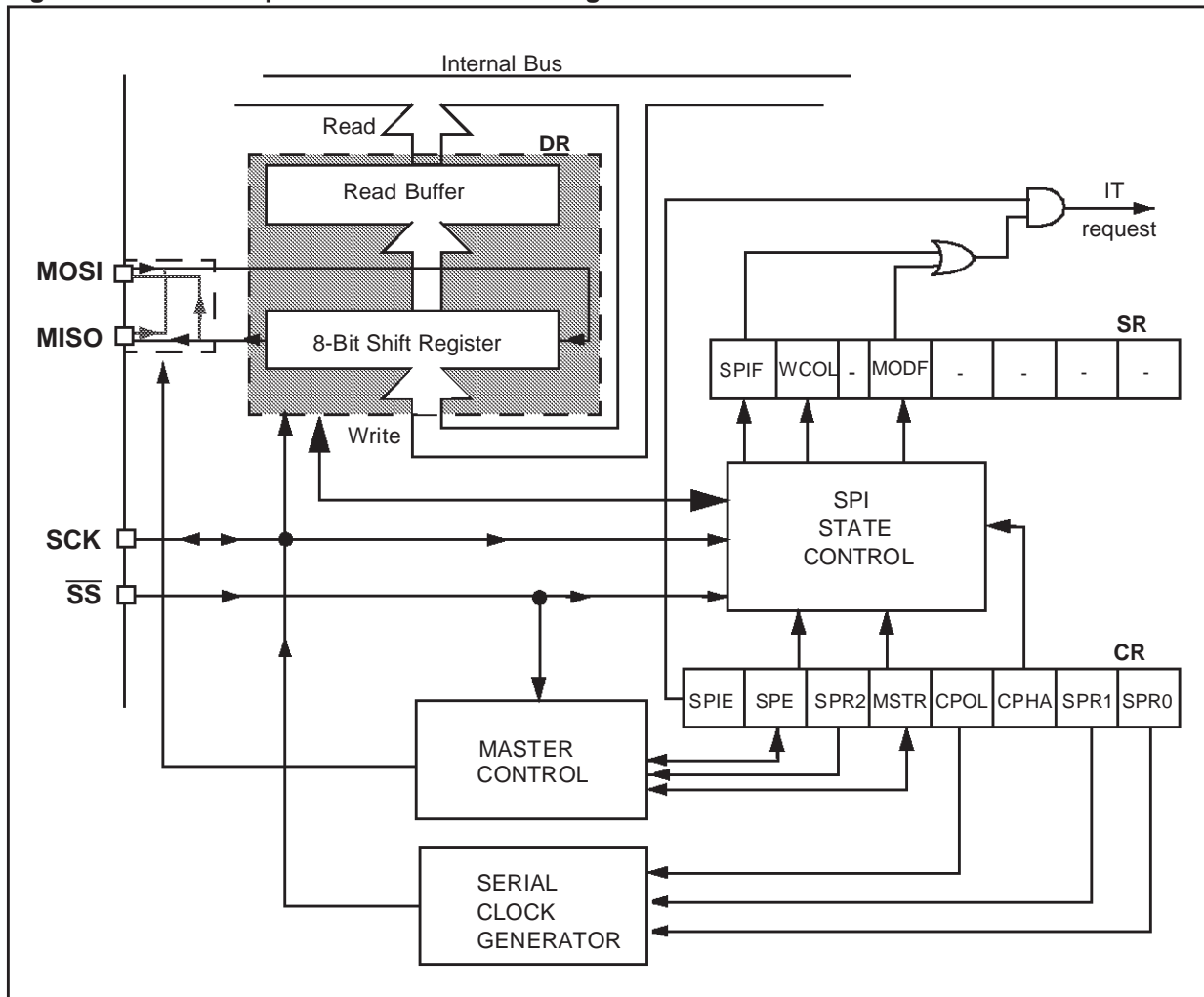
Four possible data/clock timing relationships may be chosen (see Figure 40) but master and slave must be programmed with the same timing mode.

**Figure 37. Serial Peripheral Interface Master/Slave**



SERIAL PERIPHERAL INTERFACE (Cont'd)

Figure 38. Serial Peripheral Interface Block Diagram



## SERIAL PERIPHERAL INTERFACE (Cont'd)

### 11.3.4 Functional Description

Figure 37 shows the serial peripheral interface (SPI) block diagram.

This interface contains 3 dedicated registers:

- A Control Register (CR)
- A Status Register (SR)
- A Data Register (DR)

Refer to the CR, SR and DR registers in Section 11.3.7 for the bit definitions.

#### 11.3.4.1 Master Configuration

In a master configuration, the serial clock is generated on the SCK pin.

##### Procedure

- Select the SPR0 & SPR1 bits to define the serial clock baud rate (see CR register).
- Select the CPOL and CPHA bits to define one of the four relationships between the data transfer and the serial clock (see Figure 40).
- The  $\overline{SS}$  pin must be connected to a high level signal during the complete byte transmit sequence.
- The MSTR and SPE bits must be set (they remain set only if the  $\overline{SS}$  pin is connected to a high level signal).

In this configuration the MOSI pin is a data output and to the MISO pin is a data input.

##### Transmit sequence

The transmit sequence begins when a byte is written to the DR register.

The data byte is parallel loaded into the 8-bit shift register (from the internal bus) during a write cycle and then shifted out serially to the MOSI pin most significant bit first.

When data transfer is complete:

- The SPIF bit is set by hardware
- An interrupt is generated if the SPIE bit is set and the I bit in the CCR register is cleared.

During the last clock cycle the SPIF bit is set, a copy of the data byte received in the shift register is moved to a buffer. When the DR register is read, the SPI peripheral returns this buffered value.

Clearing the SPIF bit is performed by the following software sequence:

1. An access to the SR register while the SPIF bit is set
2. A write or a read of the DR register.

**Note:** While the SPIF bit is set, all writes to the DR register are inhibited until the SR register is read.

**SERIAL PERIPHERAL INTERFACE (Cont'd)****11.3.4.2 Slave Configuration**

In slave configuration, the serial clock is received on the SCK pin from the master device.

The value of the SPR0 & SPR1 bits is not used for the data transfer.

**Procedure**

- For correct data transfer, the slave device must be in the same timing mode as the master device (CPOL and CPHA bits). See Figure 40.
- The  $\overline{SS}$  pin must be connected to a low level signal during the complete byte transmit sequence.
- Clear the MSTR bit and set the SPE bit to assign the pins to alternate function.

In this configuration the MOSI pin is a data input and the MISO pin is a data output.

**Transmit Sequence**

The data byte is parallel loaded into the 8-bit shift register (from the internal bus) during a write cycle and then shifted out serially to the MISO pin most significant bit first.

The transmit sequence begins when the slave device receives the clock signal and the most significant bit of the data on its MOSI pin.

When data transfer is complete:

- The SPIF bit is set by hardware
- An interrupt is generated if SPIE bit is set and I bit in CCR register is cleared.

During the last clock cycle the SPIF bit is set, a copy of the data byte received in the shift register is moved to a buffer. When the DR register is read, the SPI peripheral returns this buffered value.

Clearing the SPIF bit is performed by the following software sequence:

1. An access to the SR register while the SPIF bit is set.
2. A write or a read of the DR register.

**Notes:** While the SPIF bit is set, all writes to the DR register are inhibited until the SR register is read.

The SPIF bit can be cleared during a second transmission; however, it must be cleared before the second SPIF bit in order to prevent an overrun condition (see Section 11.3.4.6).

Depending on the CPHA bit, the  $\overline{SS}$  pin has to be set to write to the DR register between each data byte transfer to avoid a write collision (see Section 11.3.4.4).

**SERIAL PERIPHERAL INTERFACE (Cont'd)**

**11.3.4.3 Data Transfer Format**

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The serial clock is used to synchronize the data transfer during a sequence of eight clock pulses.

The  $\overline{SS}$  pin allows individual selection of a slave device; the other slave devices that are not selected do not interfere with the SPI transfer.

**Clock Phase and Clock Polarity**

Four possible timing relationships may be chosen by software, using the CPOL and CPHA bits.

The CPOL (clock polarity) bit controls the steady state value of the clock when no data is being transferred. This bit affects both master and slave modes.

The combination between the CPOL and CPHA (clock phase) bits selects the data capture clock edge.

Figure 40, shows an SPI transfer with the four combinations of the CPHA and CPOL bits. The diagram may be interpreted as a master or slave timing diagram where the SCK pin, the MISO pin, the MOSI pin are directly connected between the master and the slave device.

The  $\overline{SS}$  pin is the slave device select input and can be driven by the master device.

The master device applies data to its MOSI pin-clock edge before the capture clock edge.

**CPHA bit is set**

The second edge on the SCK pin (falling edge if the CPOL bit is reset, rising edge if the CPOL bit is set) is the MSBit capture strobe. Data is latched on the occurrence of the second clock transition.

No write collision should occur even if the  $\overline{SS}$  pin stays low during a transfer of several bytes (see Figure 39).

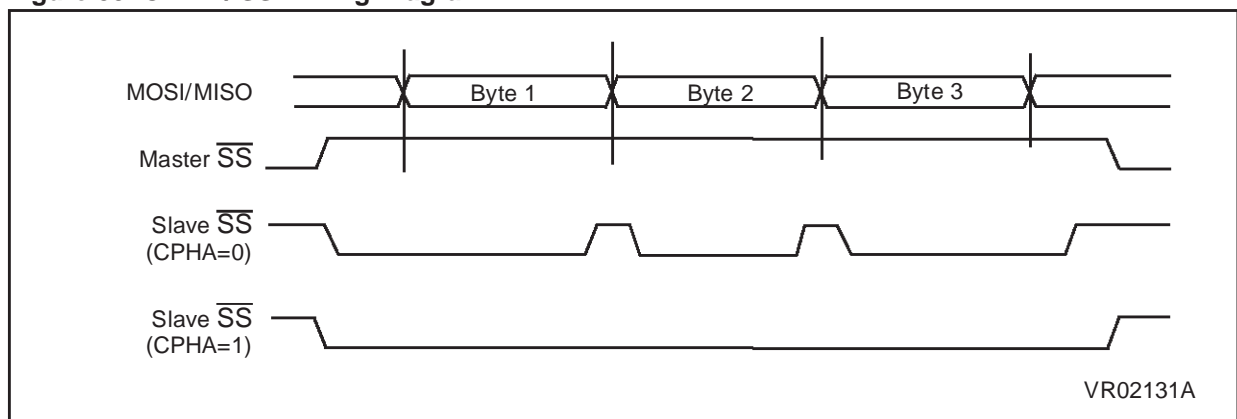
**CPHA bit is reset**

The first edge on the SCK pin (falling edge if CPOL bit is set, rising edge if CPOL bit is reset) is the MSBit capture strobe. Data is latched on the occurrence of the first clock transition.

The  $\overline{SS}$  pin must be toggled high and low between each byte transmitted (see Figure 39).

To protect the transmission from a write collision a low value on the  $\overline{SS}$  pin of a slave device freezes the data in its DR register and does not allow it to be altered. Therefore the  $\overline{SS}$  pin must be high to write a new data byte in the DR without producing a write collision.

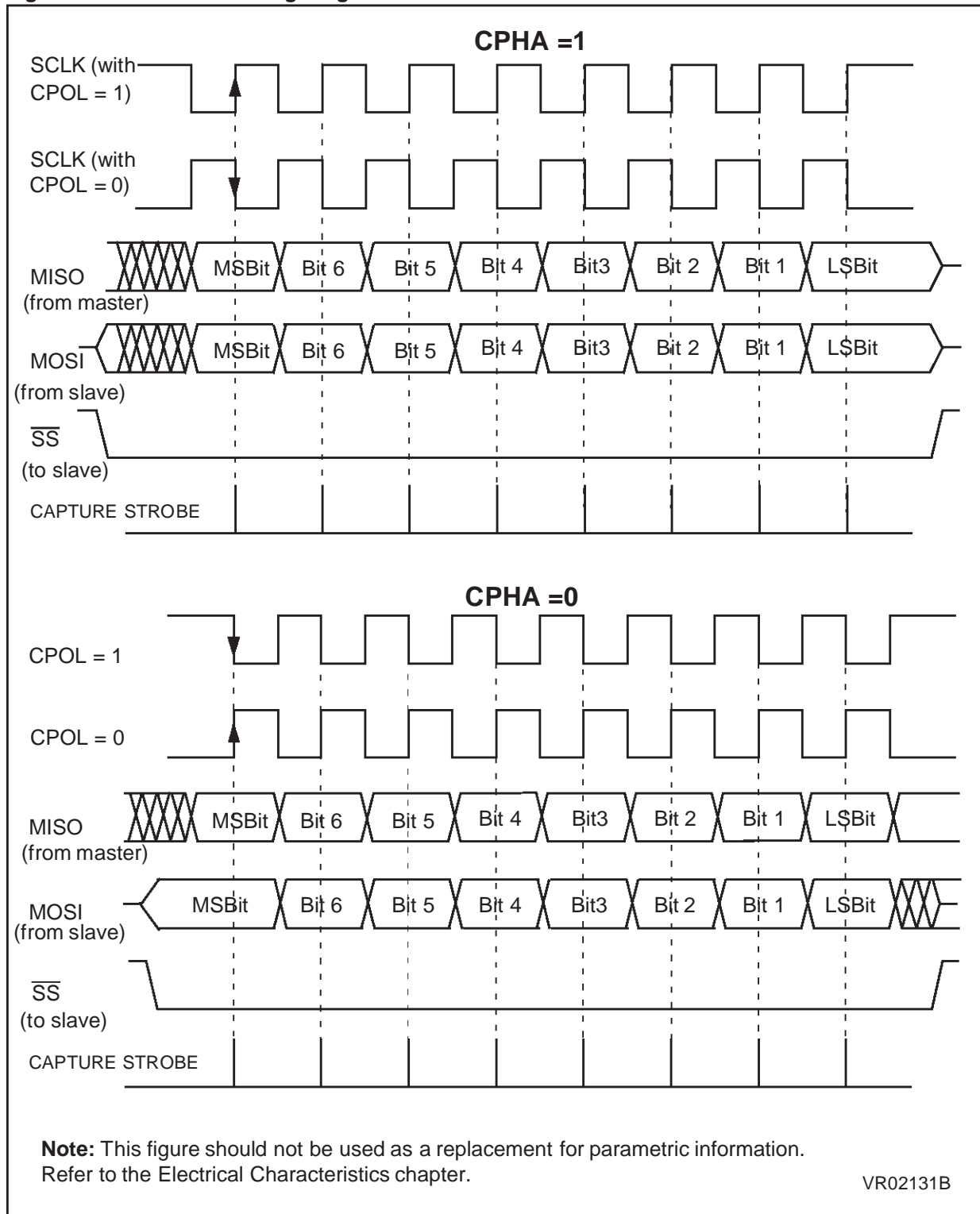
**Figure 39. CPHA /  $\overline{SS}$  Timing Diagram**





SERIAL PERIPHERAL INTERFACE (Cont'd)

Figure 40. Data Clock Timing Diagram



**SERIAL PERIPHERAL INTERFACE (Cont'd)**

**11.3.4.4 Write Collision Error**

A write collision occurs when the software tries to write to the DR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted; and the software write will be unsuccessful.

Write collisions can occur both in master and slave mode.

**Note:** a "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation.

**In Slave mode**

When the CPHA bit is set:

The slave device will receive a clock (SCK) edge prior to the latch of the first data transfer. This first clock edge will freeze the data in the slave device DR register and output the MSBit on to the external MISO pin of the slave device.

The  $\overline{SS}$  pin low state enables the slave device but the output of the MSBit onto the MISO pin does not take place until the first data transfer clock edge.

When the CPHA bit is reset:

Data is latched on the occurrence of the first clock transition. The slave device does not have any way of knowing when that transition will occur; therefore, the slave device collision occurs when software attempts to write the DR register after its  $\overline{SS}$  pin has been pulled low.

For this reason, the  $\overline{SS}$  pin must be high, between each data byte transfer, to allow the CPU to write in the DR register without generating a write collision.

**In Master mode**

Collision in the master device is defined as a write of the DR register while the internal serial clock (SCK) is in the process of transfer.

The  $\overline{SS}$  pin signal must be always high on the master device.

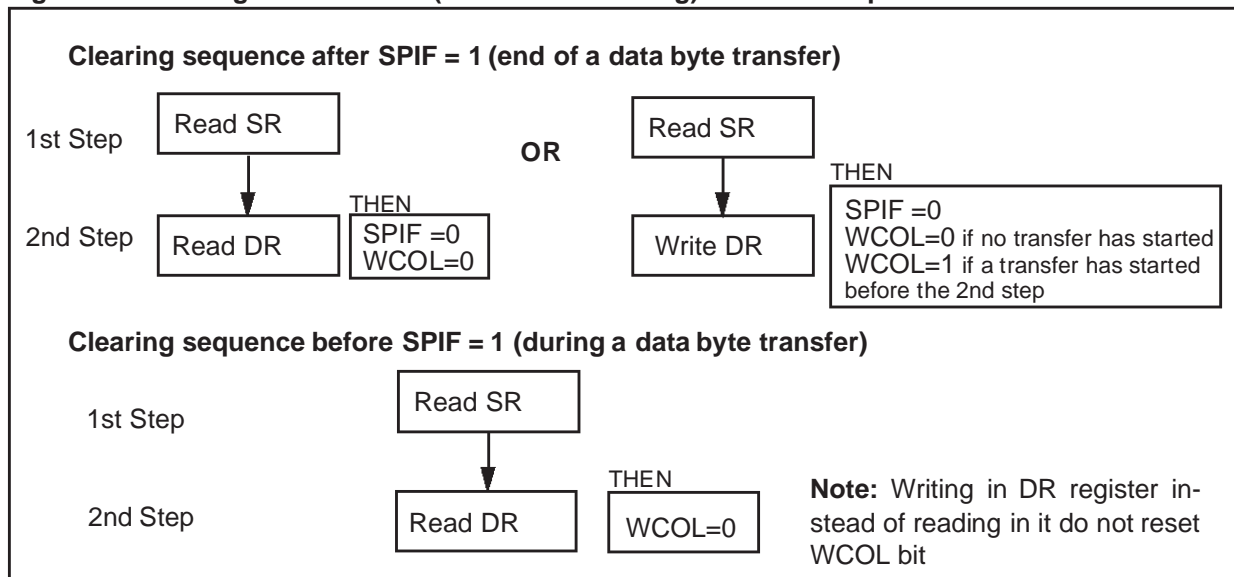
**WCOL bit**

The WCOL bit in the SR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

Clearing the WCOL bit is done through a software sequence (see Figure 41).

**Figure 41. Clearing the WCOL bit (Write Collision Flag) Software Sequence**



## SERIAL PERIPHERAL INTERFACE (Cont'd)

### 11.3.4.5 Master Mode Fault

Master mode fault occurs when the master device has its  $\overline{SS}$  pin pulled low, then the MODF bit is set.

Master mode fault affects the SPI peripheral in the following ways:

- The MODF bit is set and an SPI interrupt is generated if the SPIE bit is set.
- The SPE bit is reset. This blocks all output from the device and disables the SPI peripheral.
- The MSTR bit is reset, thus forcing the device into slave mode.

Clearing the MODF bit is done through a software sequence:

1. A read or write access to the SR register while the MODF bit is set.
2. A write to the CR register.

**Notes:** To avoid any multiple slave conflicts in the case of a system comprising several MCUs, the  $\overline{SS}$  pin must be pulled high during the clearing sequence of the MODF bit. The SPE and MSTR bits

may be restored to their original state during or after this clearing sequence.

Hardware does not allow the user to set the SPE and MSTR bits while the MODF bit is set except in the MODF bit clearing sequence.

In a slave device the MODF bit can not be set, but in a multi master configuration the device can be in slave mode with this MODF bit set.

The MODF bit indicates that there might have been a multi-master conflict for system control and allows a proper exit from system operation to a reset or default system state using an interrupt routine.

### 11.3.4.6 Overrun Condition

An overrun condition occurs when the master device has sent several data bytes and the slave device has not cleared the SPIF bit issuing from the previous data byte transmitted.

In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read to the DR register returns this byte. All other bytes are lost.

This condition is not detected by the SPI peripheral.

**SERIAL PERIPHERAL INTERFACE (Cont'd)**

**11.3.4.7 Single Master and Multimaster Configurations**

There are two types of SPI systems:

- Single Master System
- Multimaster System

**Single Master System**

A typical single master system may be configured, using an MCU as the master and four MCUs as slaves (see Figure 42).

The master device selects the individual slave devices by using four pins of a parallel port to control the four  $\overline{SS}$  pins of the slave devices.

The  $\overline{SS}$  pins are pulled high during reset since the master device ports will be forced to be inputs at that time, thus disabling the slave devices.

**Note:** To prevent a bus conflict on the MISO line the master allows only one active slave device during a transmission.

For more security, the slave device may respond to the master with the received data byte. Then the master will receive the previous byte back from the slave device if all MISO and MOSI pins are connected and the slave has not written its DR register.

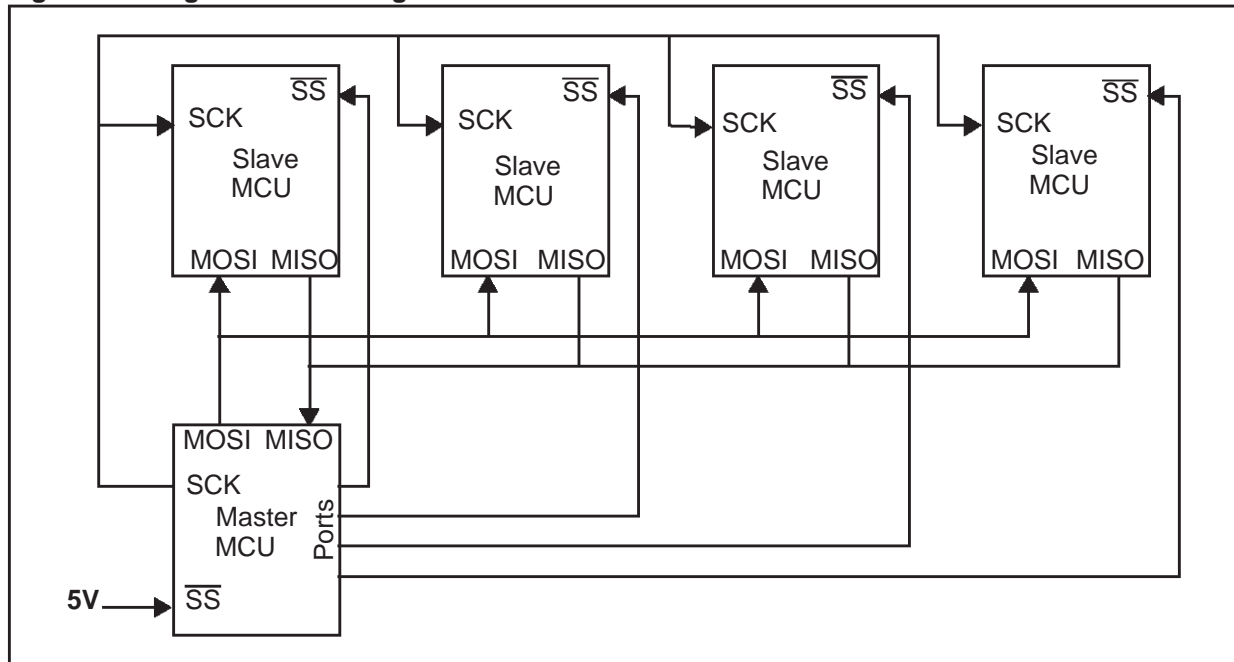
Other transmission security methods can use ports for handshake lines or data bytes with command fields.

**Multi-master System**

A multi-master system may also be configured by the user. Transfer of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system.

The multi-master system is principally handled by the MSTR bit in the CR register and the MODF bit in the SR register.

**Figure 42. Single Master Configuration**



**SERIAL PERIPHERAL INTERFACE (Cont'd)****11.3.5 Low Power Modes**

Mode	Description
WAIT	No effect on SPI. SPI interrupt events cause the device to exit from WAIT mode.
HALT	SPI registers are frozen. In HALT mode, the SPI is inactive. SPI operation resumes when the MCU is woken up by an interrupt with "exit from HALT mode" capability.

**11.3.6 Interrupts**

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
SPI End of Transfer Event	SPIF	SPIE	Yes	No
Master Mode Fault Event	MODF		Yes	No

**Note:** The SPI interrupt events are connected to the same interrupt vector (see Interrupts chapter). They generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

**SERIAL PERIPHERAL INTERFACE (Cont'd)**

**11.3.7 Register Description**

**CONTROL REGISTER (CR)**

Read/Write

Reset Value: 0000xxxx (0xh)

7							0
SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0

Bit 7 = **SPIE** *Serial peripheral interrupt enable.*

This bit is set and cleared by software.

0: Interrupt is inhibited

1: An SPI interrupt is generated whenever SPIF=1 or MODF=1 in the SR register

Bit 6 = **SPE** *Serial peripheral output enable.*

This bit is set and cleared by software. It is also cleared by hardware when, in master mode,  $\overline{SS}=0$  (see Section 11.3.4.5 "Master Mode Fault" on page 66).

0: I/O port connected to pins

1: SPI alternate functions connected to pins

The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins.

Bit 5 = **SPR2** *Divider Enable.*

this bit is set and cleared by software and it is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate. Refer to Table 15.

0: Divider by 2 enabled

1: Divider by 2 disabled

Bit 4 = **MSTR** *Master.*

This bit is set and cleared by software. It is also cleared by hardware when, in master mode,  $\overline{SS}=0$  (see Section 11.3.4.5 "Master Mode Fault" on page 66).

0: Slave mode is selected

1: Master mode is selected, the function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.

Bit 3 = **CPOL** *Clock polarity.*

This bit is set and cleared by software. This bit determines the steady state of the serial Clock. The CPOL bit affects both the master and slave modes.

0: The steady state is a low value at the SCK pin.

1: The steady state is a high value at the SCK pin.

Bit 2 = **CPHA** *Clock phase.*

This bit is set and cleared by software.

0: The first clock transition is the first data capture edge.

1: The second clock transition is the first capture edge.

Bit 1:0 = **SPR[1:0]** *Serial peripheral rate.*

These bits are set and cleared by software. Used with the SPR2 bit, they select one of six baud rates to be used as the serial clock when the device is a master.

These 2 bits have no effect in slave mode.

**Table 15. Serial Peripheral Baud Rate**

Serial Clock	SPR2	SPR1	SPR0
$f_{CPU}/2$	1	0	0
$f_{CPU}/8$	0	0	0
$f_{CPU}/16$	0	0	1
$f_{CPU}/32$	1	1	0
$f_{CPU}/64$	0	1	0
$f_{CPU}/128$	0	1	1

**SERIAL PERIPHERAL INTERFACE (Cont'd)**

**STATUS REGISTER (SR)**

Read Only

Reset Value: 0000 0000 (00h)

7							0
SPIF	WCOL	-	MODF	-	-	-	-

Bit 7 = **SPIF** *Serial Peripheral data transfer flag*.  
 This bit is set by hardware when a transfer has been completed. An interrupt is generated if SPIE=1 in the CR register. It is cleared by a software sequence (an access to the SR register followed by a read or write to the DR register).

0: Data transfer is in progress or has been approved by a clearing sequence.

1: Data transfer between the device and an external device has been completed.

**Note:** While the SPIF bit is set, all writes to the DR register are inhibited.

Bit 6 = **WCOL** *Write Collision status*.

This bit is set by hardware when a write to the DR register is done during a transmit sequence. It is cleared by a software sequence (see Figure 41).

0: No write collision occurred

1: A write collision has been detected

Bit 5 = Unused.

Bit 4 = **MODF** *Mode Fault flag*.

This bit is set by hardware when the  $\overline{SS}$  pin is pulled low in master mode (see Section 11.3.4.5 "Master Mode Fault" on page 66). An SPI interrupt can be generated if SPIE=1 in the CR register. This bit is cleared by a software sequence (An access to the SR register while MODF=1 followed by a write to the CR register).

0: No master mode fault detected

1: A fault in master mode has been detected

Bits 3-0 = Unused.

**DATA I/O REGISTER (DR)**

Read/Write

Reset Value: Undefined

7							0
D7	D6	D5	D4	D3	D2	D1	D0

The DR register is used to transmit and receive data on the serial bus. In the master device only a write to this register will initiate transmission/reception of another byte.

**Notes:** During the last clock cycle the SPIF bit is set, a copy of the received data byte in the shift register is moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read.

**Warning:**

A write to the DR register places data directly into the shift register for transmission.

A write to the the DR register returns the value located in the buffer and not the contents of the shift register (See Figure 38 ).

SERIAL PERIPHERAL INTERFACE (Cont'd)

Table 16. SPI Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0021h	<b>SPIDR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x
0022h	<b>SPICR</b> Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0023h	<b>SPISR</b> Reset Value	SPIF 0	WCOL 0	0	MODF 0	0	0	0	0



## 11.4 I<sup>2</sup>C BUS INTERFACE (I2C)

### 11.4.1 Introduction

The I<sup>2</sup>C Bus Interface serves as an interface between the microcontroller and the serial I<sup>2</sup>C bus. It provides both multimaster and slave functions, and controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing. It supports fast I<sup>2</sup>C mode (400kHz).

### 11.4.2 Main Features

- Parallel-bus/I<sup>2</sup>C protocol converter
- Multi-master capability
- 7-bit/10-bit Addressing
- Transmitter/Receiver flag
- End-of-byte transmission flag
- Transfer problem detection

#### I<sup>2</sup>C Master Features:

- Clock generation
- I<sup>2</sup>C bus busy flag
- Arbitration Lost Flag
- End of byte transmission flag
- Transmitter/Receiver Flag
- Start bit detection flag
- Start and Stop generation

#### I<sup>2</sup>C Slave Features:

- Stop bit detection
- I<sup>2</sup>C bus busy flag
- Detection of misplaced start or stop condition
- Programmable I<sup>2</sup>C Address detection
- Transfer problem detection
- End-of-byte transmission flag
- Transmitter/Receiver flag

### 11.4.3 General Description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa, using either an interrupt or polled

handshake. The interrupts are enabled or disabled by software. The interface is connected to the I<sup>2</sup>C bus by a data pin (SDA) and by a clock pin (SCL). It can be connected both with a standard I<sup>2</sup>C bus and a Fast I<sup>2</sup>C bus. This selection is made by software.

#### Mode Selection

The interface can operate in the four following modes:

- Slave transmitter/receiver
- Master transmitter/receiver

By default, it operates in slave mode.

The interface automatically switches from slave to master after it generates a START condition and from master to slave in case of arbitration loss or a STOP generation, allowing then Multi-Master capability.

#### Communication Flow

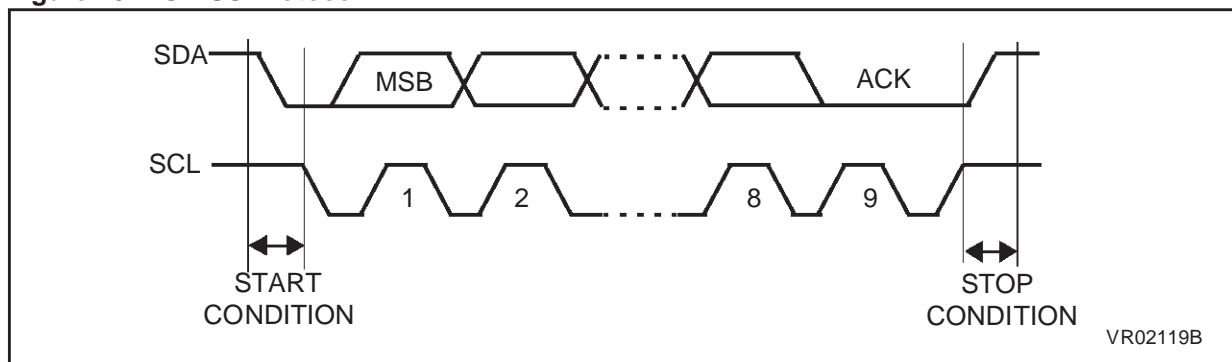
In Master mode, it initiates a data transfer and generates the clock signal. A serial data transfer always begins with a start condition and ends with a stop condition. Both start and stop conditions are generated in master mode by software.

In Slave mode, the interface is capable of recognising its own address (7 or 10-bit), and the General Call address. The General Call address detection may be enabled or disabled by software.

Data and addresses are transferred as 8-bit bytes, MSB first. The first byte(s) following the start condition contain the address (one in 7-bit mode, two in 10-bit mode). The address is always transmitted in Master mode.

A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter. Refer to Figure 43.

Figure 43. I<sup>2</sup>C BUS Protocol



**I<sup>2</sup>C BUS INTERFACE (Cont'd)**

Acknowledge may be enabled and disabled by software.

The I<sup>2</sup>C interface address and/or general call address can be selected by software.

The speed of the I<sup>2</sup>C interface may be selected between Standard (0-100KHz) and Fast I<sup>2</sup>C (100-400KHz).

The SCL frequency ( $F_{SCL}$ ) is controlled by a programmable clock divider which depends on the I<sup>2</sup>C bus mode.

When the I<sup>2</sup>C cell is enabled, the SDA and SCL ports must be configured as floating inputs. In this case, the value of the external pull-up resistor used depends on the application.

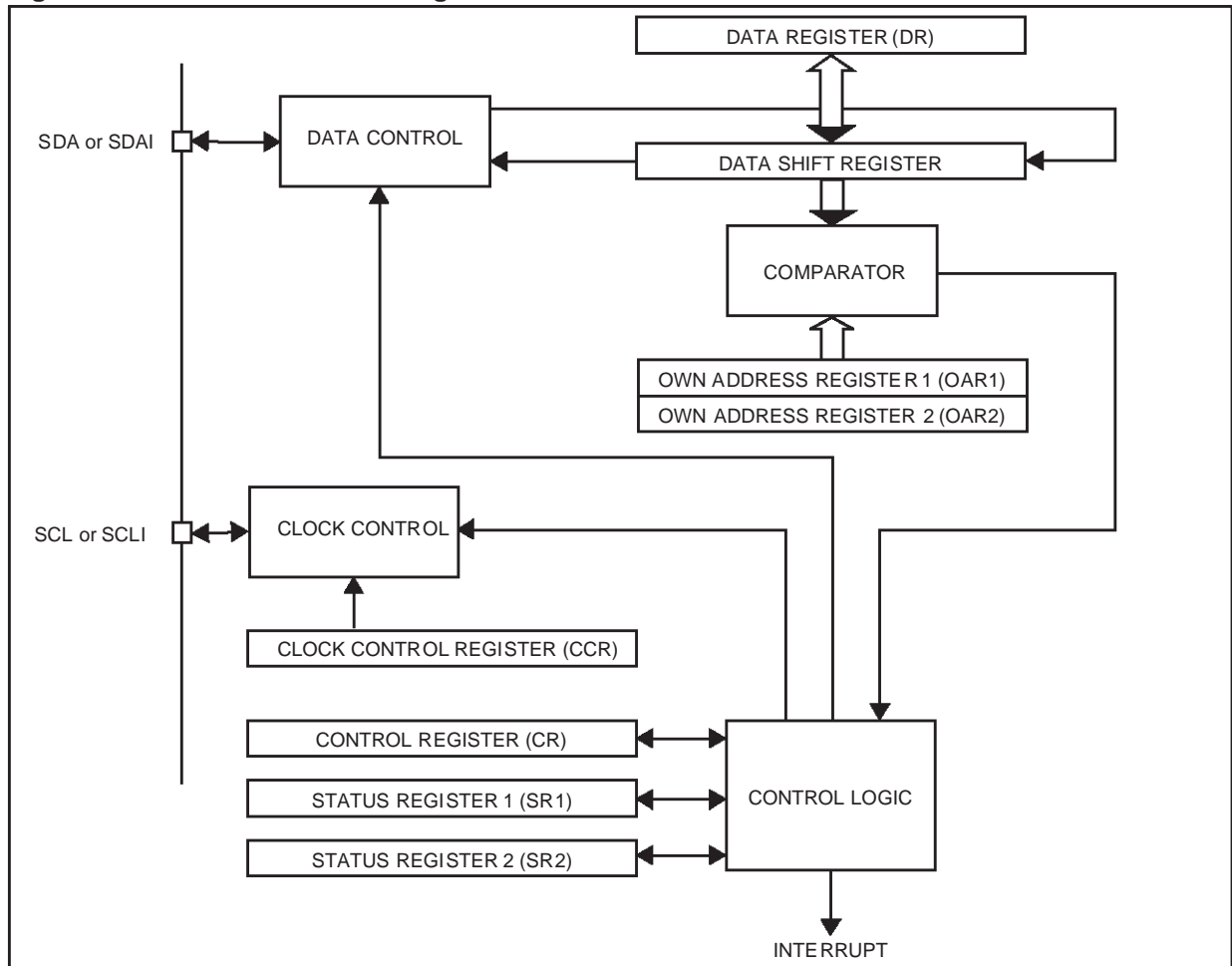
When the I<sup>2</sup>C cell is disabled, the SDA and SCL ports revert to being standard I/O port pins.

**SDA/SCL Line Control**

Transmitter mode: the interface holds the clock line low before transmission to wait for the microcontroller to write the byte in the Data Register.

Receiver mode: the interface holds the clock line low after reception to wait for the microcontroller to read the byte in the Data Register.

**Figure 44. I<sup>2</sup>C Interface Block Diagram**



## I<sup>2</sup>C BUS INTERFACE (Cont'd)

### 11.4.4 Functional Description

Refer to the CR, SR1 and SR2 registers in Section 11.4.7. for the bit definitions.

By default the I<sup>2</sup>C interface operates in Slave mode (M/SL bit is cleared) except when it initiates a transmit or receive sequence.

First the interface frequency must be configured using the FRi bits in the OAR2 register.

#### 11.4.4.1 Slave Mode

As soon as a start condition is detected, the address is received from the SDA line and sent to the shift register; then it is compared with the address of the interface or the General Call address (if selected by software).

**Note:** In 10-bit addressing mode, the comparison includes the header sequence (11110xx0) and the two most significant bits of the address.

**Header matched** (10-bit mode only): the interface generates an acknowledge pulse if the ACK bit is set.

**Address not matched:** the interface ignores it and waits for another Start condition.

**Address matched:** the interface generates in sequence:

- Acknowledge pulse if the ACK bit is set.
- EVF and ADSL bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register, **holding the SCL line low** (see Figure 45 Transfer sequencing EV1).

Next, in 7-bit mode read the DR register to determine from the least significant bit (Data Direction Bit) if the slave must enter Receiver or Transmitter mode.

In 10-bit mode, after receiving the address sequence the slave is always in receive mode. It will enter transmit mode on receiving a repeated Start condition followed by the header sequence with matching address bits and the least significant bit set (11110xx1) .

#### Slave Receiver

Following the address reception and after SR1 register has been read, the slave receives bytes from the SDA line into the DR register via the internal shift register. After each byte the interface generates in sequence:

- Acknowledge pulse if the ACK bit is set

- EVF and BTF bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, **holding the SCL line low** (see Figure 45 Transfer sequencing EV2).

#### Slave Transmitter

Following the address reception and after SR1 register has been read, the slave sends bytes from the DR register to the SDA line via the internal shift register.

The slave waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see Figure 45 Transfer sequencing EV3).

When the acknowledge pulse is received:

- The EVF and BTF bits are set by hardware with an interrupt if the ITE bit is set.

#### Closing slave communication

After the last data byte is transferred a Stop Condition is generated by the master. The interface detects this condition and sets:

- EVF and STOPF bits with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR2 register (see Figure 45 Transfer sequencing EV4).

#### Error Cases

- **BERR:** Detection of a Stop or a Start condition during a byte transfer. In this case, the EVF and the BERR bits are set with an interrupt if the ITE bit is set.

If it is a Stop then the interface discards the data, released the lines and waits for another Start condition.

If it is a Start then the interface discards the data and waits for the next slave address on the bus.

- **AF:** Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set with an interrupt if the ITE bit is set.

**Note:** In both cases, SCL line is not held low; however, SDA line can remain low due to possible «0» bits transmitted last. It is then necessary to release both lines by software.

## I<sup>2</sup>C BUS INTERFACE (Cont'd)

### How to release the SDA / SCL lines

Set and subsequently clear the STOP bit while BTF is set. The SDA/SCL lines are released after the transfer of the current byte.

#### 11.4.4.2 Master Mode

To switch from default Slave mode to Master mode a Start condition generation is needed.

#### Start condition

Setting the START bit while the BUSY bit is cleared causes the interface to switch to Master mode (M/SL bit set) and generates a Start condition.

Once the Start condition is sent:

- The EVF and SB bits are set by hardware with an interrupt if the ITE bit is set.

Then the master waits for a read of the SR1 register followed by a write in the DR register with the Slave address, **holding the SCL line low** (see Figure 45 Transfer sequencing EV5).

#### Slave address transmission

Then the slave address is sent to the SDA line via the internal shift register.

In 7-bit addressing mode, one address byte is sent.

In 10-bit addressing mode, sending the first byte including the header sequence causes the following event:

- The EVF bit is set by hardware with interrupt generation if the ITE bit is set.

Then the master waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see Figure 45 Transfer sequencing EV9).

Then the second address byte is sent by the interface.

After completion of this transfer (and acknowledge from the slave if the ACK bit is set):

- The EVF bit is set by hardware with interrupt generation if the ITE bit is set.

Then the master waits for a read of the SR1 register followed by a write in the CR register (for example set PE bit), **holding the SCL line low** (see Figure 45 Transfer sequencing EV6).

Next the master must enter Receiver or Transmitter mode.

**Note:** In 10-bit addressing mode, to switch the master to Receiver mode, software must generate a repeated Start condition and resend the header sequence with the least significant bit set (11110xx1).

#### Master Receiver

Following the address transmission and after SR1 and CR registers have been accessed, the master receives bytes from the SDA line into the DR register via the internal shift register. After each byte the interface generates in sequence:

- Acknowledge pulse if the ACK bit is set
- EVF and BTF bits are set by hardware with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, **holding the SCL line low** (see Figure 45 Transfer sequencing EV7).

To close the communication: before reading the last byte from the DR register, set the STOP bit to generate the Stop condition. The interface goes automatically back to slave mode (M/SL bit cleared).

**Note:** In order to generate the non-acknowledge pulse after the last received data byte, the ACK bit must be cleared just before reading the second last data byte.

**I<sup>2</sup>C BUS INTERFACE** (Cont'd)**Master Transmitter**

Following the address transmission and after SR1 register has been read, the master sends bytes from the DR register to the SDA line via the internal shift register.

The master waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see Figure 45 Transfer sequencing EV8).

When the acknowledge bit is received, the interface sets:

- EVF and BTF bits with an interrupt if the ITE bit is set.

To close the communication: after writing the last byte to the DR register, set the STOP bit to generate the Stop condition. The interface goes automatically back to slave mode (M/SL bit cleared).

**Error Cases**

- **BERR**: Detection of a Stop or a Start condition during a byte transfer. In this case, the EVF and

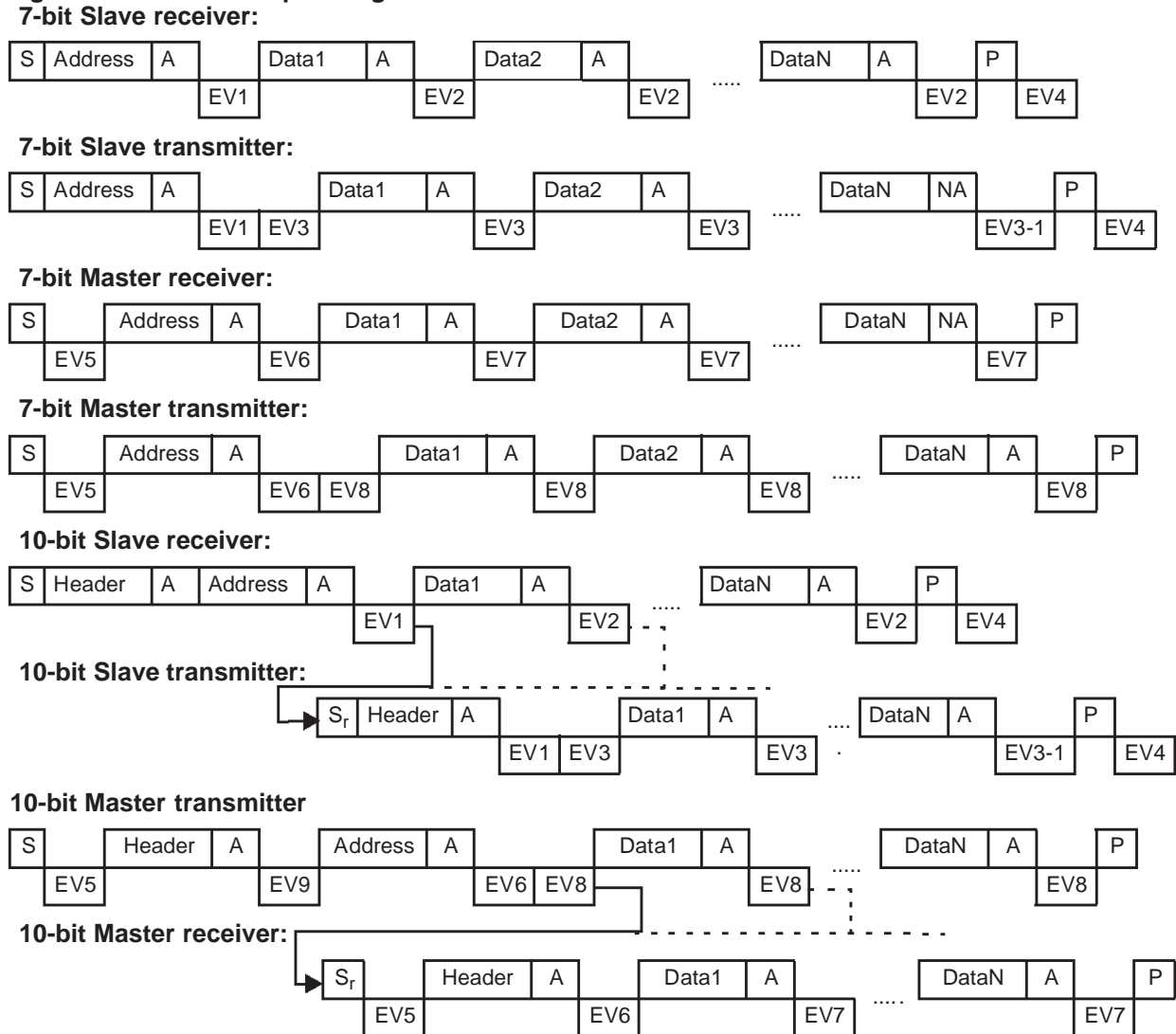
BERR bits are set by hardware with an interrupt if ITE is set.

- **AF**: Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set by hardware with an interrupt if the ITE bit is set. To resume, set the START or STOP bit.
- **ARLO**: Detection of an arbitration lost condition. In this case the ARLO bit is set by hardware (with an interrupt if the ITE bit is set and the interface goes automatically back to slave mode (the M/SL bit is cleared)).

**Note:** In all these cases, the SCL line is not held low; however, the SDA line can remain low due to possible «0» bits transmitted last. It is then necessary to release both lines by software.

I<sup>2</sup>C BUS INTERFACE (Cont'd)

Figure 45. Transfer Sequencing



**Legend:** S=Start, S<sub>r</sub> = Repeated Start, P=Stop, A=Acknowledge, NA=Non-acknowledge, EVx=Event (with interrupt if ITE=1)

- EV1:** EVF=1, ADSL=1, cleared by reading SR1 register.
- EV2:** EVF=1, BTF=1, cleared by reading SR1 register followed by reading DR register.
- EV3:** EVF=1, BTF=1, cleared by reading SR1 register followed by writing DR register.
- EV3-1:** EVF=1, AF=1, BTF=1; AF is cleared by reading SR1 register. BTF is cleared by releasing the lines (STOP=1, STOP=0) or by writing DR register (DR=FFh). **Note:** If lines are released by STOP=1, STOP=0, the subsequent EV4 is not seen.
- EV4:** EVF=1, STOPF=1, cleared by reading SR2 register.
- EV5:** EVF=1, SB=1, cleared by reading SR1 register followed by writing DR register.
- EV6:** EVF=1, cleared by reading SR1 register followed by writing CR register (for example PE=1).
- EV7:** EVF=1, BTF=1, cleared by reading SR1 register followed by reading DR register.
- EV8:** EVF=1, BTF=1, cleared by reading SR1 register followed by writing DR register.
- EV9:** EVF=1, ADD10=1, cleared by reading SR1 register followed by writing DR register.

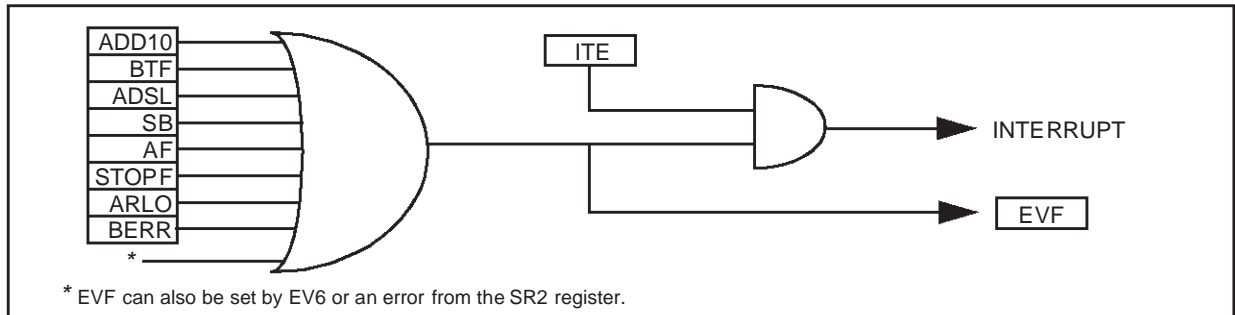
I<sup>2</sup>C BUS INTERFACE (Cont'd)

11.4.5 Low Power Modes

Mode	Description
WAIT	No effect on I <sup>2</sup> C interface. I <sup>2</sup> C interrupts cause the device to exit from WAIT mode.
HALT	I <sup>2</sup> C registers are frozen. In HALT mode, the I <sup>2</sup> C interface is inactive and does not acknowledge data on the bus. The I <sup>2</sup> C interface resumes operation when the MCU is woken up by an interrupt with "exit from HALT mode" capability.

11.4.6 Interrupts

Figure 46. Event Flags and Interrupt Generation



Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
10-bit Address Sent Event (Master mode)	ADD10	ITE	Yes	No
End of Byte Transfer Event	BTF		Yes	No
Address Matched Event (Slave mode)	ADSEL		Yes	No
Start Bit Generation Event (Master mode)	SB		Yes	No
Acknowledge Failure Event	AF		Yes	No
Stop Detection Event (Slave mode)	STOPF		Yes	No
Arbitration Lost Event (Multimaster configuration)	ARLO		Yes	No
Bus Error Event	BERR		Yes	No

**Note:** The I<sup>2</sup>C interrupt events are connected to the same interrupt vector (see Interrupts chapter). They generate an interrupt if the corresponding Enable Control Bit is set and the I-bit in the CC register is reset (RIM instruction).

**I<sup>2</sup>C BUS INTERFACE** (Cont'd)

**11.4.7 Register Description**

**I<sup>2</sup>C CONTROL REGISTER (CR)**

Read / Write

Reset Value: 0000 0000 (00h)

7							0
0	0	PE	ENGC	START	ACK	STOP	ITE

Bit 7:6 = Reserved. Forced to 0 by hardware.

Bit 5 = **PE** *Peripheral enable*.

This bit is set and cleared by software.

0: Peripheral disabled

1: Master/Slave capability

Notes:

- When PE=0, all the bits of the CR register and the SR register except the Stop bit are reset. All outputs are released while PE=0
- When PE=1, the corresponding I/O pins are selected by hardware as alternate functions.
- To enable the I<sup>2</sup>C interface, write the CR register **TWICE** with PE=1 as the first write only activates the interface (only PE is set).

Bit 4 = **ENGC** *Enable General Call*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0). The 00h General Call address is acknowledged (01h ignored).

0: General Call disabled

1: General Call enabled

Bit 3 = **START** *Generation of a Start condition*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0) or when the Start condition is sent (with interrupt generation if ITE=1).

- In master mode:
  - 0: No start generation
  - 1: Repeated start generation
- In slave mode:
  - 0: No start generation
  - 1: Start generation when the bus is free

Bit 2 = **ACK** *Acknowledge enable*.

This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0).

0: No acknowledge returned

1: Acknowledge returned after an address byte or a data byte is received

Bit 1 = **STOP** *Generation of a Stop condition*.

This bit is set and cleared by software. It is also cleared by hardware in master mode. Note: This bit is not cleared when the interface is disabled (PE=0).

- In master mode:

0: No stop generation

1: Stop generation after the current byte transfer or after the current Start condition is sent. The STOP bit is cleared by hardware when the Stop condition is sent.

- In slave mode:

0: No stop generation

1: Release the SCL and SDA lines after the current byte transfer (BTF=1). In this mode the STOP bit has to be cleared by software.

Bit 0 = **ITE** *Interrupt enable*.

This bit is set and cleared by software and cleared by hardware when the interface is disabled (PE=0).

0: Interrupts disabled

1: Interrupts enabled

Refer to Figure 46 for the relationship between the events and the interrupt.

SCL is held low when the ADD10, SB, BTF or ADSL flags or an EV6 event (See Figure 45) is detected.



**I<sup>2</sup>C BUS INTERFACE** (Cont'd)

**I<sup>2</sup>C STATUS REGISTER 1 (SR1)**

Read Only

Reset Value: 0000 0000 (00h)

7							0
EVF	ADD10	TRA	BUSY	BTF	ADSL	M/SL	SB

**Bit 7 = EVF Event flag.**

This bit is set by hardware as soon as an event occurs. It is cleared by software reading SR2 register in case of error event or as described in Figure 45. It is also cleared by hardware when the interface is disabled (PE=0).

0: No event

1: One of the following events has occurred:

- BTF=1 (Byte received or transmitted)
- ADSL=1 (Address matched in Slave mode while ACK=1)
- SB=1 (Start condition generated in Master mode)
- AF=1 (No acknowledge received after byte transmission)
- STOPF=1 (Stop condition detected in Slave mode)
- ARLO=1 (Arbitration lost in Master mode)
- BERR=1 (Bus error, misplaced Start or Stop condition detected)
- ADD10=1 (Master has sent header byte)
- Address byte successfully transmitted in Master mode.

**Bit 6 = ADD10 10-bit addressing in Master mode.**

This bit is set by hardware when the master has sent the first byte in 10-bit address mode. It is cleared by software reading SR2 register followed by a write in the DR register of the second address byte. It is also cleared by hardware when the peripheral is disabled (PE=0).

0: No ADD10 event occurred.

1: Master has sent first address byte (header)

**Bit 5 = TRA Transmitter/Receiver.**

When BTF is set, TRA=1 if a data byte has been transmitted. It is cleared automatically when BTF is cleared. It is also cleared by hardware after detection of Stop condition (STOPF=1), loss of bus

arbitration (ARLO=1) or when the interface is disabled (PE=0).

0: Data byte received (if BTF=1)

1: Data byte transmitted

**Bit 4 = BUSY Bus busy.**

This bit is set by hardware on detection of a Start condition and cleared by hardware on detection of a Stop condition. It indicates a communication in progress on the bus. This information is still updated when the interface is disabled (PE=0).

0: No communication on the bus

1: Communication ongoing on the bus

**Bit 3 = BTF Byte transfer finished.**

This bit is set by hardware as soon as a byte is correctly received or transmitted with interrupt generation if ITE=1. It is cleared by software reading SR1 register followed by a read or write of DR register. It is also cleared by hardware when the interface is disabled (PE=0).

- Following a byte transmission, this bit is set after reception of the acknowledge clock pulse. In case an address byte is sent, this bit is set only after the EV6 event (See Figure 45). BTF is cleared by reading SR1 register followed by writing the next byte in DR register.

- Following a byte reception, this bit is set after transmission of the acknowledge clock pulse if ACK=1. BTF is cleared by reading SR1 register followed by reading the byte from DR register.

The SCL line is held low while BTF=1.

0: Byte transfer not done

1: Byte transfer succeeded

**Bit 2 = ADSL Address matched (Slave mode).**

This bit is set by hardware as soon as the received slave address matched with the OAR register content or a general call is recognized. An interrupt is generated if ITE=1. It is cleared by software reading SR1 register or by hardware when the interface is disabled (PE=0).

The SCL line is held low while ADSL=1.

0: Address mismatched or not received

1: Received address matched

**I<sup>2</sup>C BUS INTERFACE** (Cont'd)

Bit 1 = **M/SL Master/Slave**.

This bit is set by hardware as soon as the interface is in Master mode (writing START=1). It is cleared by hardware after detecting a Stop condition on the bus or a loss of arbitration (ARLO=1). It is also cleared when the interface is disabled (PE=0).

0: Slave mode  
1: Master mode

Bit 0 = **SB Start bit (Master mode)**.

This bit is set by hardware as soon as the Start condition is generated (following a write START=1). An interrupt is generated if ITE=1. It is cleared by software reading SR1 register followed by writing the address byte in DR register. It is also cleared by hardware when the interface is disabled (PE=0).

0: No Start condition  
1: Start condition generated

**I<sup>2</sup>C STATUS REGISTER 2 (SR2)**

Read Only

Reset Value: 0000 0000 (00h)

7							0
0	0	0	AF	STOPF	ARLO	BERR	GCAL

Bit 7:5 = Reserved. Forced to 0 by hardware.

Bit 4 = **AF Acknowledge failure**.

This bit is set by hardware when no acknowledge is returned. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while AF=1.

0: No acknowledge failure  
1: Acknowledge failure

Bit 3 = **STOPF Stop detection (Slave mode)**.

This bit is set by hardware when a Stop condition is detected on the bus after an acknowledge (if ACK=1). An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while STOPF=1.

0: No Stop condition detected  
1: Stop condition detected

Bit 2 = **ARLO Arbitration lost**.

This bit is set by hardware when the interface loses the arbitration of the bus to another master. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

After an ARLO event the interface switches back automatically to Slave mode (M/SL=0).

The SCL line is not held low while ARLO=1.

0: No arbitration lost detected  
1: Arbitration lost detected

Bit 1 = **BERR Bus error**.

This bit is set by hardware when the interface detects a misplaced Start or Stop condition. An interrupt is generated if ITE=1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE=0).

The SCL line is not held low while BERR=1.

0: No misplaced Start or Stop condition  
1: Misplaced Start or Stop condition

Bit 0 = **GCAL General Call (Slave mode)**.

This bit is set by hardware when a general call address is detected on the bus while ENGC=1. It is cleared by hardware detecting a Stop condition (STOPF=1) or when the interface is disabled (PE=0).

0: No general call address detected on bus  
1: general call address detected on bus



**I<sup>2</sup>C BUS INTERFACE (Cont'd)**

**I<sup>2</sup>C OWN ADDRESS REGISTER (OAR1)**

Read / Write  
Reset Value: 0000 0000 (00h)

7								0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	

**7-bit Addressing Mode**

Bit 7:1 = **ADD7-ADD1** *Interface address.*  
These bits define the I<sup>2</sup>C bus address of the interface. They are not cleared when the interface is disabled (PE=0).

Bit 0 = **ADD0** *Address direction bit.*  
This bit is don't care, the interface acknowledges either 0 or 1. It is not cleared when the interface is disabled (PE=0).

Note: Address 01h is always ignored.

**10-bit Addressing Mode**

Bit 7:0 = **ADD7-ADD0** *Interface address.*  
These are the least significant bits of the I<sup>2</sup>C bus address of the interface. They are not cleared when the interface is disabled (PE=0).

**I<sup>2</sup>C OWN ADDRESS REGISTER (OAR2)**

Read / Write  
Reset Value: 0100 0000 (40h)

7								0
FR1	FR0	0	0	0	ADD9	ADD8	0	

Bit 7:6 = **FR1-FR0** *Frequency bits.*

These bits are set by software only when the interface is disabled (PE=0). To configure the interface to I<sup>2</sup>C specified delays select the value corresponding to the microcontroller frequency F<sub>CPU</sub>.

F <sub>CPU</sub> Range (MHz)	FR1	FR0
2.5 - 6	0	0
6 - 10	0	1
10 - 14	1	0
14 - 24	1	1

Bit 5:3 = Reserved

Bit 2:1 = **ADD9-ADD8** *Interface address.*  
These are the most significant bits of the I<sup>2</sup>C bus address of the interface (10-bit mode only). They are not cleared when the interface is disabled (PE=0).

Bit 0 = Reserved.

I<sup>2</sup>C BUS INTERFACE (Cont'd)Table 17. I<sup>2</sup>C Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0028h	<b>I2CCR</b> Reset Value	0	0	PE 0	ENGC 0	START 0	ACK 0	STOP 0	ITE 0
0029h	<b>I2CSR1</b> Reset Value	EVF 0	ADD10 0	TRA 0	BUSY 0	BTF 0	ADSL 0	M/SL 0	SB 0
002Ah	<b>I2CSR2</b> Reset Value	0	0	0	AF 0	STOPF 0	ARLO 0	BERR 0	GCAL 0
02Bh	<b>I2CCCR</b> Reset Value	FM/SM 0	CC6 0	CC5 0	CC4 0	CC3 0	CC2 0	CC1 0	CC0 0
02Ch	<b>I2COAR1</b> Reset Value	ADD7 0	ADD6 0	ADD5 0	ADD4 0	ADD3 0	ADD2 0	ADD1 0	ADD0 0
002Dh	<b>I2COAR2</b> Reset Value	FR1 0	FR0 1	0	0	0	ADD9 0	ADD8 0	0
002Eh	<b>I2CDR</b> Reset Value	MSB 0	0	0	0	0	0	0	LSB 0

11.5 8-BIT A/D CONVERTER (ADC)

11.5.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 8-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

The result of the conversion is stored in a 8-bit Data Register. The A/D converter is controlled through a Control/Status Register.

11.5.2 Main Features

- 8-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in Figure 47.

11.5.3 Functional Description

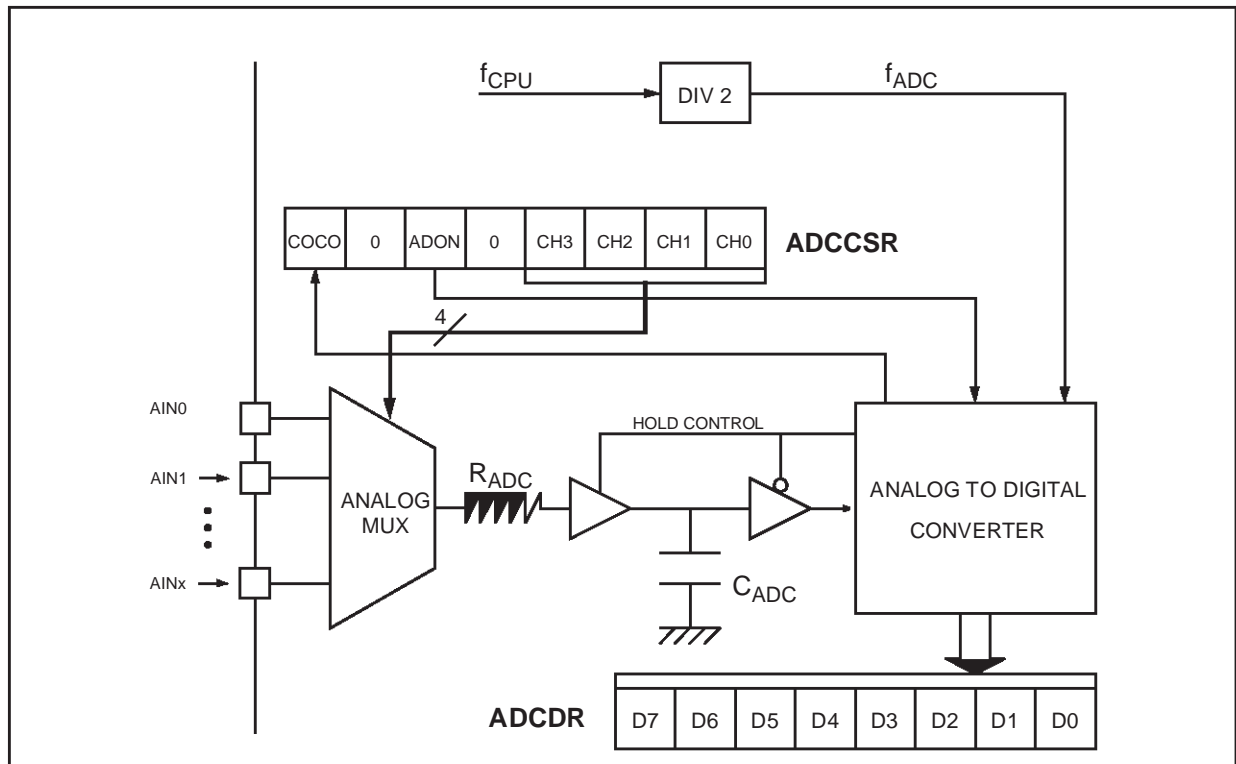
11.5.3.1 Analog Power Supply

$V_{DDA}$  and  $V_{SSA}$  are the high and low level reference voltage pins. In some devices (refer to device pin out description) they are internally connected to the  $V_{DD}$  and  $V_{SS}$  pins.

Conversion accuracy may therefore be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines.

See electrical characteristics section for more details.

Figure 47. ADC Block Diagram



**8-BIT A/D CONVERTER (ADC) (Cont'd)**

**11.5.3.2 Digital A/D Conversion Result**

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage ( $V_{AIN}$ ) is greater than or equal to  $V_{DDA}$  (high-level voltage reference) then the conversion result in the DR register is FFh (full scale) without overflow indication.

If input voltage ( $V_{AIN}$ ) is lower than or equal to  $V_{SSA}$  (low-level voltage reference) then the conversion result in the DR register is 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDR register. The accuracy of the conversion is described in the parametric section.

$R_{AIN}$  is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allotted time.

**11.5.3.3 A/D Conversion Phases**

The A/D conversion is based on two conversion phases as shown in Figure 48:

- Sample capacitor loading [duration:  $t_{LOAD}$ ]  
During this phase, the  $V_{AIN}$  input voltage to be measured is loaded into the  $C_{ADC}$  sample capacitor.
- A/D conversion [duration:  $t_{CONV}$ ]  
During this phase, the A/D conversion is computed (8 successive approximations cycles) and the  $C_{ADC}$  sample capacitor is disconnected from the analog input pin to get the optimum analog to digital conversion accuracy.

While the ADC is on, these two phases are continuously repeated.

At the end of each conversion, the sample capacitor is kept loaded with the previous measurement load. The advantage of this behaviour is that it minimizes the current consumption on the analog pin in case of single input channel measurement.

**11.5.3.4 Software Procedure**

Refer to the control/status register (CSR) and data register (DR) in Section 11.5.6 for the bit definitions and to Figure 48 for the timings.

**ADC Configuration**

The total duration of the A/D conversion is 12 ADC clock periods ( $1/f_{ADC}=2/f_{CPU}$ ).

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the CSR register:

- Select the CH[3:0] bits to assign the analog channel to be converted.

**ADC Conversion**

In the CSR register:

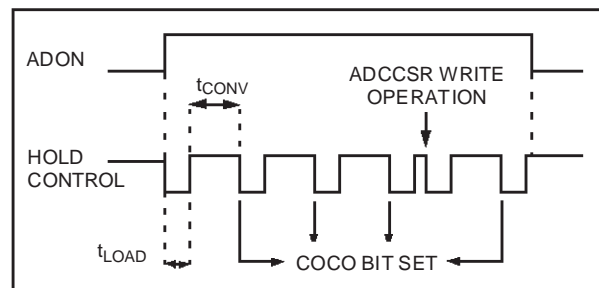
- Set the ADON bit to enable the A/D converter and to start the first conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete

- The COCO bit is set by hardware.
- No interrupt is generated.
- The result is in the DR register and remains valid until the next conversion has ended.

A write to the CSR register (with ADON set) aborts the current conversion, resets the COCO bit and starts a new conversion.

**Figure 48. ADC Conversion Timings**



**11.5.4 Low Power Modes**

Mode	Description
WAIT	No effect on A/D Converter
HALT	A/D Converter disabled. After wakeup from Halt mode, the A/D Converter requires a stabilisation time before accurate conversions can be performed.

**Note:** The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

**11.5.5 Interrupts**

None

**8-BIT A/D CONVERTER (ADC) (Cont'd)**

**11.5.6 Register Description**

**CONTROL/STATUS REGISTER (CSR)**

Read/Write

Reset Value: 0000 0000 (00h)

7							0
COCO	0	ADON	0	CH3	CH2	CH1	CH0

Bit 7 = **COCO** *Conversion Complete*  
 This bit is set by hardware. It is cleared by software reading the result in the DR register or writing to the CSR register.  
 0: Conversion is not complete  
 1: Conversion can be read from the DR register

Bit 6 = **Reserved.** *must always be cleared.*

Bit 5 = **ADON** *A/D Converter On*  
 This bit is set and cleared by software.  
 0: A/D converter is switched off  
 1: A/D converter is switched on

Bit 4 = **Reserved.** *must always be cleared.*

Bit 3:0 = **CH[3:0]** *Channel Selection*  
 These bits are set and cleared by software. They select the analog input to convert.

Channel Pin*	CH3	CH2	CH1	CH0
AIN0	0	0	0	0
AIN1	0	0	0	1
AIN2	0	0	1	0
AIN3	0	0	1	1
AIN4	0	1	0	0
AIN5	0	1	0	1
AIN6	0	1	1	0
AIN7	0	1	1	1
AIN8	1	0	0	0
AIN9	1	0	0	1
AIN10	1	0	1	0
AIN11	1	0	1	1
AIN12	1	1	0	0
AIN13	1	1	0	1
AIN14	1	1	1	0
AIN15	1	1	1	1

**\*Note:** The number of pins AND the channel selection varies according to the device. Refer to the device pinout.

**DATA REGISTER (DR)**

Read Only

Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7:0 = **D[7:0]** *Analog Converted Value*  
 This register contains the converted analog value in the range 00h to FFh.

**Note:** Reading this register reset the COCO flag.



## 8-BIT A/D CONVERTER (ADC) (Cont'd)

Table 18. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0070h	<b>ADCDR</b> Reset Value	D7 0	D6 0	D5 0	D4 0	D3 0	D2 0	D1 0	D0 0
0071h	<b>ADCCSR</b> Reset Value	COCO 0	0	ADON 0	0	CH3 0	CH2 0	CH1 0	CH0 0

## 12 INSTRUCTION SET

### 12.1 ST7 ADDRESSING MODES

The ST7 Core features 17 different addressing modes which can be classified in 7 main groups:

Addressing Mode	Example
Inherent	nop
Immediate	ld A,#\$55
Direct	ld A,\$55
Indexed	ld A,(\$55,X)
Indirect	ld A,([\$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 Instruction set is designed to minimize the number of bytes required per instruction: To do

so, most of the addressing modes may be subdivided in two sub-modes called long and short:

- Long addressing mode is more powerful because it can use the full 64 Kbyte address space, however it uses more bytes and more CPU cycles.
- Short addressing mode is less powerful because it can generally only access page zero (0000h - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 Assembler optimizes the use of long and short addressing modes.

**Table 19. ST7 Addressing Mode Overview**

Mode		Syntax	Destination/Source	Pointer Address (Hex.)	Pointer Size (Hex.)	Length (Bytes)
Inherent		nop				+ 0
Immediate		ld A,#\$55				+ 1
Short	Direct	ld A,\$10	00..FF			+ 1
Long	Direct	ld A,\$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF		+ 0 (with X register) + 1 (with Y register)
Short	Direct	Indexed	ld A,(\$10,X)	00..1FE		+ 1
Long	Direct	Indexed	ld A,(\$1000,X)	0000..FFFF		+ 2
Short	Indirect		ld A,[\$10]	00..FF	00..FF	byte + 2
Long	Indirect		ld A,[\$10.w]	0000..FFFF	00..FF	word + 2
Short	Indirect	Indexed	ld A,([\$10],X)	00..1FE	00..FF	byte + 2
Long	Indirect	Indexed	ld A,([\$10.w],X)	0000..FFFF	00..FF	word + 2
Relative	Direct		jrne loop	PC-128/PC+127 <sup>1)</sup>		+ 1
Relative	Indirect		jrne [\$10]	PC-128/PC+127 <sup>1)</sup>	00..FF	byte + 2
Bit	Direct		bset \$10,#7	00..FF		+ 1
Bit	Indirect		bset [\$10],#7	00..FF	00..FF	byte + 2
Bit	Direct	Relative	btjt \$10,#7,skip	00..FF		+ 2
Bit	Indirect	Relative	btjt [\$10],#7,skip	00..FF	00..FF	byte + 3

Note 1. At the time the instruction is executed, the Program Counter (PC) points to the instruction following JRxx.

**ST7 ADDRESSING MODES (Cont'd)****12.1.1 Inherent**

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

**12.1.2 Immediate**

Immediate instructions have two bytes, the first byte contains the opcode, the second byte contains the operand value.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

**12.1.3 Direct**

In Direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two sub-modes:

**Direct (short)**

The address is a byte, thus requires only one byte after the opcode, but only allows 00 - FF addressing space.

**Direct (long)**

The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

**12.1.4 Indexed (No Offset, Short, Long)**

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indirect addressing mode consists of three sub-modes:

**Indexed (No Offset)**

There is no offset, (no extra byte after the opcode), and allows 00 - FF addressing space.

**Indexed (Short)**

The offset is a byte, thus requires only one byte after the opcode and allows 00 - 1FE addressing space.

**Indexed (long)**

The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

**12.1.5 Indirect (Short, Long)**

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two sub-modes:

**Indirect (short)**

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

**Indirect (long)**

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

**ST7 ADDRESSING MODES (Cont'd)**

**12.1.6 Indirect Indexed (Short, Long)**

This is a combination of indirect and short indexed addressing modes. The operand is referenced by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the opcode.

The indirect indexed addressing mode consists of two sub-modes:

**Indirect Indexed (Short)**

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - 1FE addressing space, and requires 1 byte after the opcode.

**Indirect Indexed (Long)**

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

**Table 20. Instructions Supporting Direct, Indexed, Indirect and Indirect Indexed Addressing Modes**

Long and Short Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Addition/subtraction operations
BCP	Bit Compare

Short Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

**12.1.7 Relative mode (Direct, Indirect)**

This addressing mode is used to modify the PC register value, by adding an 8-bit signed offset to it.

Available Relative Direct/Indirect Instructions	Function
JRxx	Conditional Jump
CALLR	Call Relative

The relative addressing mode consists of two sub-modes:

**Relative (Direct)**

The offset follows the opcode.

**Relative (Indirect)**

The offset is defined in memory, of which the address follows the opcode.

## 12.2 INSTRUCTION GROUPS

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may

be subdivided into 13 main groups as illustrated in the following table:

Load and Transfer	LD	CLR						
Stack operation	PUSH	POP	RSP					
Increment/Decrement	INC	DEC						
Compare and Tests	CP	TNZ	BCP					
Logical operations	AND	OR	XOR	CPL	NEG			
Bit Operation	BSET	BRES						
Conditional Bit Test and Branch	BTJT	BTJF						
Arithmetic operations	ADC	ADD	SUB	SBC	MUL			
Shift and Rotates	SLL	SRL	SRA	RLC	RRC	SWAP	SLA	
Unconditional Jump or Call	JRA	JRT	JRF	JP	CALL	CALLR	NOP	RET
Conditional Branch	JRxx							
Interrupt management	TRAP	WFI	HALT	IRET				
Code Condition Flag modification	SIM	RIM	SCF	RCF				

### Using a pre-byte

The instructions are described with one to four bytes.

In order to extend the number of available opcodes for an 8-bit CPU (256 opcodes), three different prebyte opcodes are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

PC-2            End of previous instruction  
 PC-1            Prebyte  
 PC               opcode  
 PC+1           Additional word (0 to 2) according to the number of bytes required to compute the effective address

These prebytes enable instruction in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or the instruction using direct addressing mode. The prebytes are:

PDY 90            Replace an X based instruction using immediate, direct, indexed, or inherent addressing mode by a Y one.

PIX 92            Replace an instruction using direct, direct bit, or direct relative addressing mode to an instruction using the corresponding indirect addressing mode.

It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

PIY 91            Replace an instruction using X indirect indexed addressing mode by a Y one.

INSTRUCTION GROUPS (Cont'd)

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M	H		N	Z	C
ADD	Addition	A = A + M	A	M	H		N	Z	C
AND	Logical And	A = A . M	A	M			N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M			N	Z	
BRES	Bit Reset	bres Byte, #3	M						
BSET	Bit Set	bset Byte, #3	M						
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M						C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M						C
CALL	Call subroutine								
CALLR	Call subroutine relative								
CLR	Clear		reg, M				0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M			N	Z	C
CPL	One Complement	A = FFH-A	reg, M				N	Z	1
DEC	Decrement	dec Y	reg, M				N	Z	
HALT	Halt					0			
IRET	Interrupt routine return	Pop CC, A, X, PC			H	I	N	Z	C
INC	Increment	inc X	reg, M				N	Z	
JP	Absolute Jump	jp [TBL.w]							
JRA	Jump relative always								
JRT	Jump relative								
JRF	Never jump	jrf *							
JRIH	Jump if ext. interrupt = 1								
JRIL	Jump if ext. interrupt = 0								
JRH	Jump if H = 1	H = 1 ?							
JRNH	Jump if H = 0	H = 0 ?							
JRM	Jump if I = 1	I = 1 ?							
JRNM	Jump if I = 0	I = 0 ?							
JRMI	Jump if N = 1 (minus)	N = 1 ?							
JRPL	Jump if N = 0 (plus)	N = 0 ?							
JREQ	Jump if Z = 1 (equal)	Z = 1 ?							
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?							
JRC	Jump if C = 1	C = 1 ?							
JRNC	Jump if C = 0	C = 0 ?							
JRULT	Jump if C = 1	Unsigned <							
JRUGE	Jump if C = 0	Jmp if unsigned >=							
JRUGT	Jump if (C + Z = 0)	Unsigned >							

**INSTRUCTION GROUPS (Cont'd)**

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
JRULE	Jump if (C + Z = 1)	Unsigned <=							
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg \$10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg pop CC	reg CC	M M					
					H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC					
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= Dst <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => Dst => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Subtract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= Dst <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= Dst <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => Dst => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	Dst7 => Dst => C	reg, M				N	Z	C
SUB	Subtraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	Dst[7..4] <=> Dst[3..0]	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

## 13 ELECTRICAL CHARACTERISTICS

### 13.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to  $V_{SS}$ .

#### 13.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A=25^\circ\text{C}$  and  $T_A=T_{Amax}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\Sigma$ ).

#### 13.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A=25^\circ\text{C}$ ,  $V_{DD}=5\text{V}$  (for the  $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$  voltage range) and  $V_{DD}=3.3\text{V}$  (for the  $3\text{V} \leq V_{DD} \leq 4\text{V}$  voltage range). They are given only as design guidelines and are not tested.

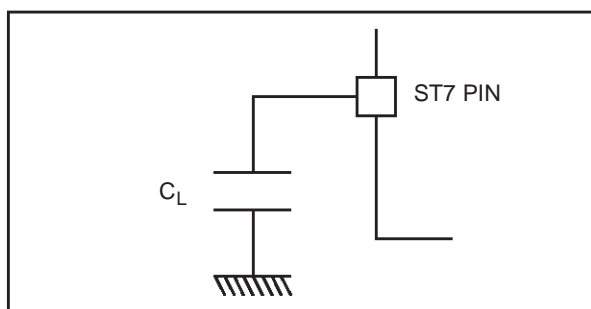
#### 13.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 13.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 49.

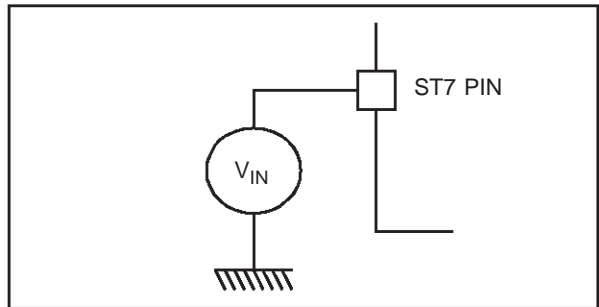
Figure 49. Pin loading conditions



#### 13.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 50.

Figure 50. Pin input voltage





**13.2 ABSOLUTE MAXIMUM RATINGS**

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these condi-

tions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**13.2.1 Voltage Characteristics**

Symbol	Ratings	Maximum value	Unit
$V_{DD} - V_{SS}$	Supply voltage	6.5	V
$V_{IN}$	Input voltage on any pin <sup>1) &amp; 2)</sup>	$V_{SS}-0.3$ to $V_{DD}+0.3$	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see Section 13.7.2 “Absolute Electrical Sensitivity” on page 110	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		

**13.2.2 Current Characteristics**

Symbol	Ratings	Maximum value	Unit
$I_{VDD}$	Total current into $V_{DD}$ power lines (source) <sup>3)</sup>	80	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>3)</sup>	80	
$I_{IO}$	Output current sunk by any standard I/O and control pin	25	
	Output current sunk by any high sink I/O pin	50	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ <sup>2) &amp; 4)</sup>	Injected current on $\overline{ISPSEL}$ pin	$\pm 5$	
	Injected current on $\overline{RESET}$ pin	$\pm 5$	
	Injected current on OSC1 and OSC2 pins	$\pm 5$	
	Injected current on any other pin <sup>5) &amp; 6)</sup>	$\pm 5$	
$\Sigma I_{INJ(PIN)}$ <sup>2)</sup>	Total injected current (sum of all I/O and control pins) <sup>5)</sup>	$\pm 20$	

**13.2.3 Thermal Characteristics**

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature (see Section 14.2 “THERMAL CHARACTERISTICS” on page 127 )		

**Notes:**

1. Directly connecting the  $\overline{RESET}$  and I/O pins to  $V_{DD}$  or  $V_{SS}$  could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for  $\overline{RESET}$ , 10kΩ for I/Os). Unused I/O pins must be tied in the same way to  $V_{DD}$  or  $V_{SS}$  according to their reset configuration.
2. When the current limitation is not possible, the  $V_{IN}$  absolute maximum rating must be respected, otherwise refer to  $I_{INJ(PIN)}$  specification. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .
3. All power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) lines must always be connected to the external supply.
4. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
  - Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
  - Pure digital pins must have a negative injection less than 1.6mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.
5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterisation with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.
6. True open drain I/O port pins do not accept positive injection.

13.3 OPERATING CONDITIONS

13.3.1 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	Supply voltage	see Figure 51 and Figure 52	3.0	5.5	V
f <sub>OSC</sub>	External clock frequency	V <sub>DD</sub> ≥3.5V for ROM devices V <sub>DD</sub> ≥4.5V for FLASH devices	0 <sup>1)</sup>	16	MHz
		V <sub>DD</sub> ≥3.0V	0 <sup>1)</sup>	8	
T <sub>A</sub>	Ambient temperature range	1 Suffix Version	0	70	°C
		6 Suffix Version	-40	85	
		7 Suffix Version	-40	105	
		3 Suffix Version	-40	125	

Figure 51. f<sub>OSC</sub> Maximum Operating Frequency Versus V<sub>DD</sub> Supply Voltage for ROM devices<sup>2)</sup>

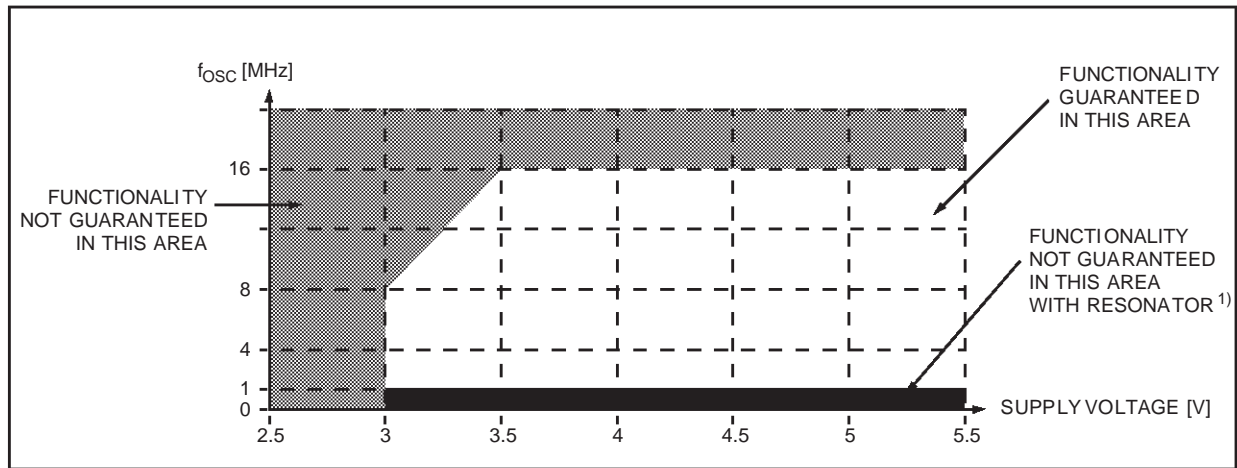
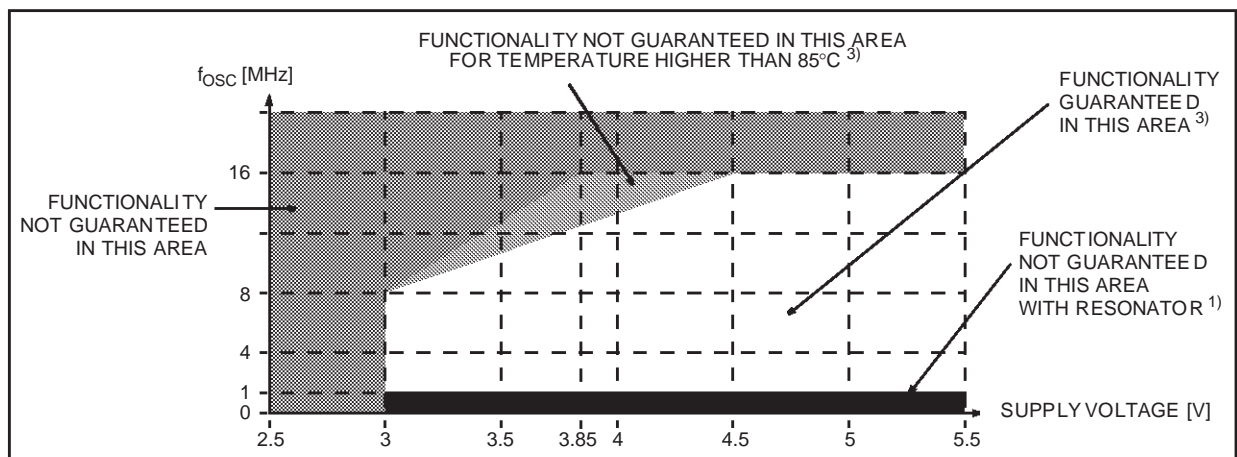


Figure 52. f<sub>OSC</sub> Maximum Operating Frequency Versus V<sub>DD</sub> Supply Voltage for FLASH devices<sup>2)</sup>



Notes:

1. Guaranteed by construction. A/D operation and resonator oscillator start-up are not guaranteed below 1MHz.
2. Operating conditions with T<sub>A</sub>=-40 to +125°C.
3. FLASH programming tested in production at maximum T<sub>A</sub> with two different conditions: V<sub>DD</sub>=5.5V, f<sub>CPU</sub>=8MHz and V<sub>DD</sub>=3V, f<sub>CPU</sub>=4MHz.

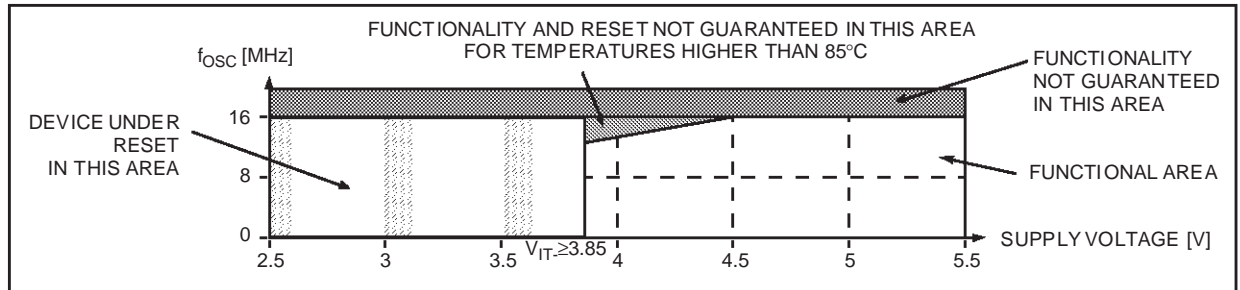
**OPERATING CONDITIONS (Cont'd)**

**13.3.2 Operating Conditions with Low Voltage Detector (LVD)**

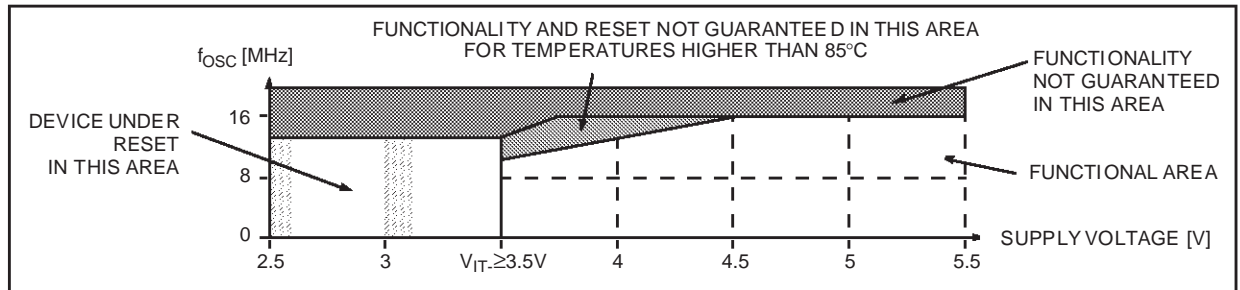
Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$ .

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit
$V_{IT+}$	Reset release threshold ( $V_{DD}$ rise)	High Threshold	4.10 <sup>2)</sup>	4.30	4.50	V
		Med. Threshold	3.75 <sup>2)</sup>	3.90	4.05	
		Low Threshold	3.25 <sup>2)</sup>	3.35	3.45	
$V_{IT-}$	Reset generation threshold ( $V_{DD}$ fall)	High Threshold	3.85	4.05	4.25	V
		Med. Threshold	3.50	3.65	3.80	
		Low Threshold	3.00	3.10	3.20	
$V_{hyst}$	LVD voltage threshold hysteresis	$V_{IT+}-V_{IT-}$	200	250	300	mV
$V_{tPOR}$	$V_{DD}$ rise time rate <sup>3)</sup>		0.2		50	V/ms
$t_g(V_{DD})$	Filtered glitch delay on $V_{DD}$ <sup>2)</sup>	Not detected by the LVD			40	ns

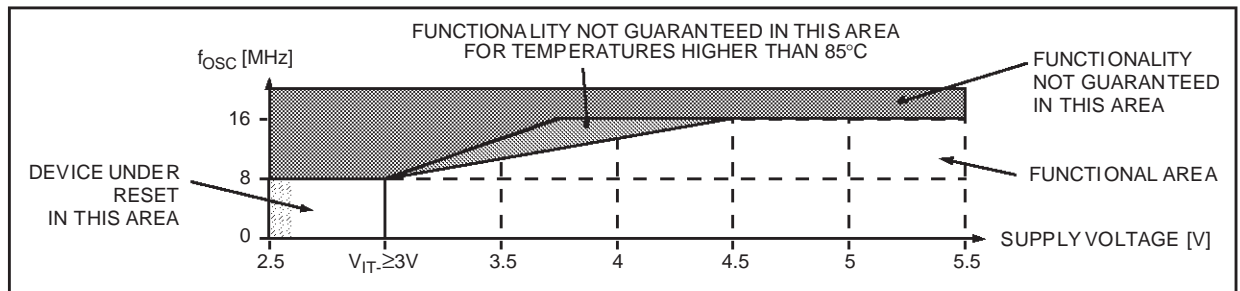
**Figure 53. High LVD Threshold Versus  $V_{DD}$  and  $f_{OSC}$  for FLASH devices<sup>3)</sup>**



**Figure 54. Medium LVD Threshold Versus  $V_{DD}$  and  $f_{OSC}$  for FLASH devices<sup>3)</sup>**



**Figure 55. Low LVD Threshold Versus  $V_{DD}$  and  $f_{OSC}$  for FLASH devices<sup>2)</sup>**



**Notes:**

1. LVD typical data are based on  $T_A=25^\circ\text{C}$ . They are given only as design guidelines and are not tested.
2. Data based on characterization results, not tested in production.
3. The  $V_{DD}$  rise time rate condition is needed to insure a correct device power-on and LVD reset. Not tested in production.

FUNCTIONAL OPERATING CONDITIONS (Cont'd)

Figure 56. High LVD Threshold Versus  $V_{DD}$  and  $f_{OSC}$  for ROM devices <sup>2)</sup>

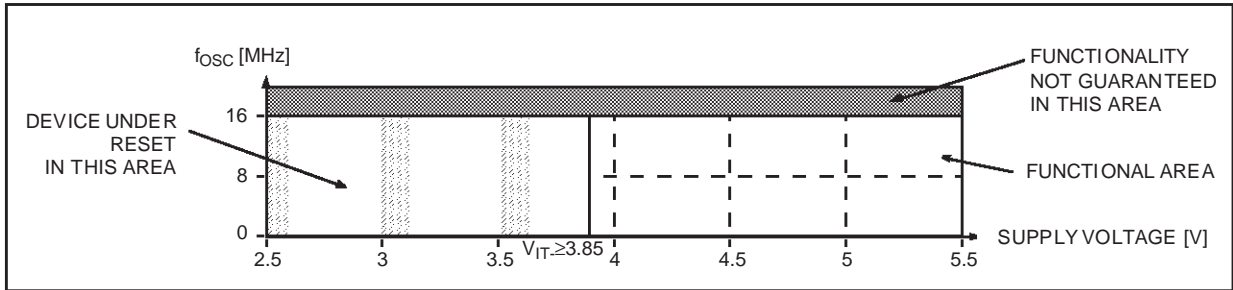


Figure 57. Medium LVD Threshold Versus  $V_{DD}$  and  $f_{OSC}$  for ROM devices <sup>2)</sup>

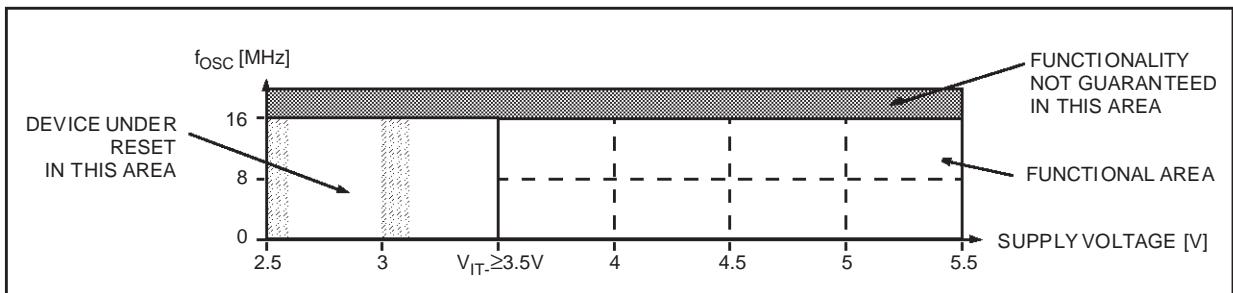
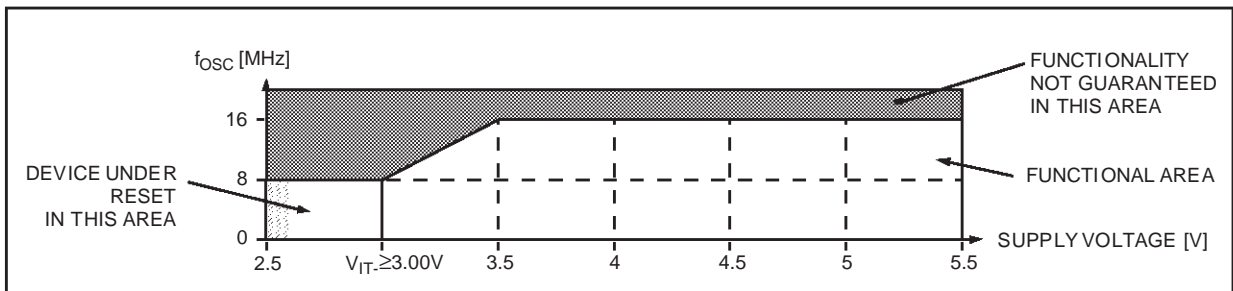


Figure 58. Low LVD Threshold Versus  $V_{DD}$  and  $f_{OSC}$  for ROM devices <sup>2)</sup>



Notes:

1. LVD typical data are based on  $T_A=25^\circ\text{C}$ . They are given only as design guidelines and are not tested.
2. The minimum  $V_{DD}$  rise time rate is needed to insure a correct device power-on and LVD reset. Not tested in production.

**13.4 SUPPLY CURRENT CHARACTERISTICS**

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total de-

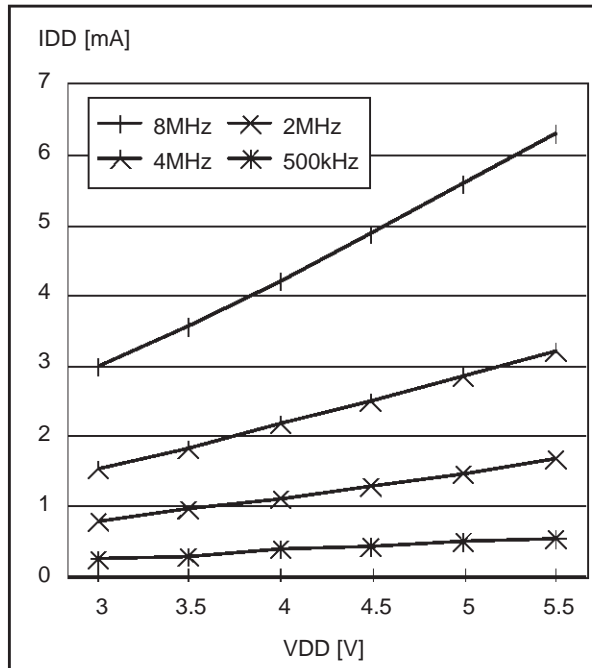
vice consumption, the two current values must be added (except for HALT mode for which the clock is stopped).

Symbol	Parameter	Conditions	Max	Unit
$\Delta I_{DD}(\Delta T_a)$	Supply current variation vs. temperature	Constant $V_{DD}$ and $f_{CPU}$	10	%

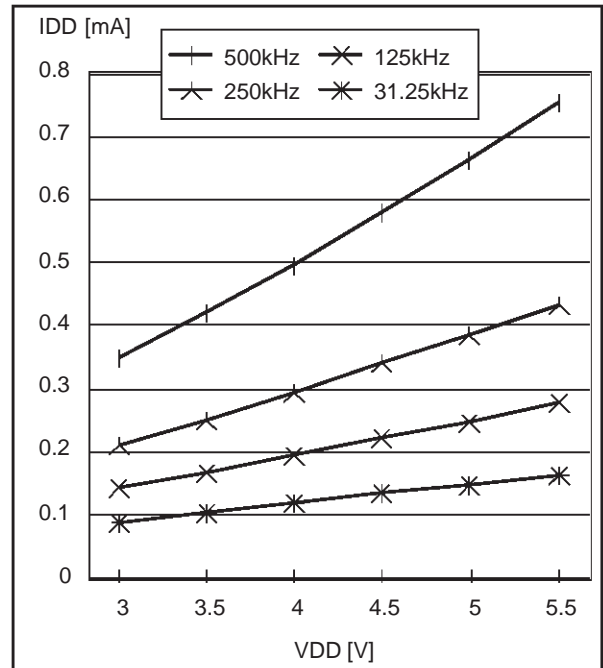
**13.4.1 RUN and SLOW Modes**

Symbol	Parameter	Conditions	Typ <sup>1)</sup>	Max <sup>2)</sup>	Unit
$I_{DD}$	Supply current in RUN mode <sup>3)</sup> (see Figure 59)	$4.5V \leq V_{DD} \leq 5.5V$ $f_{OSC}=1MHz, f_{CPU}=500kHz$	500	900	$\mu A$
		$f_{OSC}=4MHz, f_{CPU}=2MHz$	1500	2500	
	$f_{OSC}=16MHz, f_{CPU}=8MHz$	5600	9000		
	Supply current in SLOW mode <sup>4)</sup> (see Figure 60)	$4.5V \leq V_{DD} \leq 5.5V$ $f_{OSC}=1MHz, f_{CPU}=31.25kHz$	150	450	
$f_{OSC}=4MHz, f_{CPU}=125kHz$		250	550		
$I_{DD}$	Supply current in RUN mode <sup>3)</sup> (see Figure 59)	$3V \leq V_{DD} \leq 3.6V$ $f_{OSC}=1MHz, f_{CPU}=500kHz$	300	550	$\mu A$
		$f_{OSC}=4MHz, f_{CPU}=2MHz$	970	1350	
	$f_{OSC}=16MHz, f_{CPU}=8MHz$	3600	4500		
	Supply current in SLOW mode <sup>4)</sup> (see Figure 60)	$3V \leq V_{DD} \leq 3.6V$ $f_{OSC}=1MHz, f_{CPU}=31.25kHz$	100	250	
$f_{OSC}=4MHz, f_{CPU}=125kHz$		170	300		
		$f_{OSC}=16MHz, f_{CPU}=500kHz$	420	700	

**Figure 59. Typical  $I_{DD}$  in RUN vs.  $f_{CPU}$**



**Figure 60. Typical  $I_{DD}$  in SLOW vs.  $f_{CPU}$**



**Notes:**

1. Typical data are based on  $T_A=25^\circ C$ ,  $V_{DD}=5V$  ( $4.5V \leq V_{DD} \leq 5.5V$  range) and  $V_{DD}=3.3V$  ( $3V \leq V_{DD} \leq 3.6V$  range).
2. Data based on characterization results, tested in production at  $V_{DD}$  max. and  $f_{CPU}$  max.
3. CPU running with memory access, all I/O pins in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load), all peripherals in reset state; clock input (OSC1) driven by external square wave, CSS and LVD disabled.
4. SLOW mode selected with  $f_{CPU}$  based on  $f_{OSC}$  divided by 32. All I/O pins in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load), all peripherals in reset state; clock input (OSC1) driven by external square wave, CSS and LVD disabled.

SUPPLY CURRENT CHARACTERISTICS (Cont'd)

13.4.2 WAIT and SLOW WAIT Modes

Symbol	Parameter	Conditions	Typ <sup>1)</sup>	Max <sup>2)</sup>	Unit	
I <sub>DD</sub>	Supply current in WAIT mode <sup>3)</sup> (see Figure 61)	4.5V ≤ V <sub>DD</sub> ≤ 5.5V	f <sub>OSC</sub> =1MHz, f <sub>CPU</sub> =500kHz	150	280	μA
	f <sub>OSC</sub> =4MHz, f <sub>CPU</sub> =2MHz		560	900		
	f <sub>OSC</sub> =16MHz, f <sub>CPU</sub> =8MHz	2200	3000			
	Supply current in SLOW WAIT mode <sup>4)</sup> (see Figure 62)	4.5V ≤ V <sub>DD</sub> ≤ 5.5V	f <sub>OSC</sub> =1MHz, f <sub>CPU</sub> =31.25kHz	20	70	
f <sub>OSC</sub> =4MHz, f <sub>CPU</sub> =125kHz	90		190			
f <sub>OSC</sub> =16MHz, f <sub>CPU</sub> =500kHz	340		850			
I <sub>DD</sub>	Supply current in WAIT mode <sup>3)</sup> (see Figure 61)	3V ≤ V <sub>DD</sub> ≤ 3.6V	f <sub>OSC</sub> =1MHz, f <sub>CPU</sub> =500kHz	90	200	μA
	f <sub>OSC</sub> =4MHz, f <sub>CPU</sub> =2MHz		350	550		
	f <sub>OSC</sub> =16MHz, f <sub>CPU</sub> =8MHz	1370	1900			
	Supply current in SLOW WAIT mode <sup>4)</sup> (see Figure 62)	3V ≤ V <sub>DD</sub> ≤ 3.6V	f <sub>OSC</sub> =1MHz, f <sub>CPU</sub> =31.25kHz	10	20	
f <sub>OSC</sub> =4MHz, f <sub>CPU</sub> =125kHz	50		80			
f <sub>OSC</sub> =16MHz, f <sub>CPU</sub> =500kHz	200		350			

Figure 61. Typical I<sub>DD</sub> in WAIT vs. f<sub>CPU</sub>

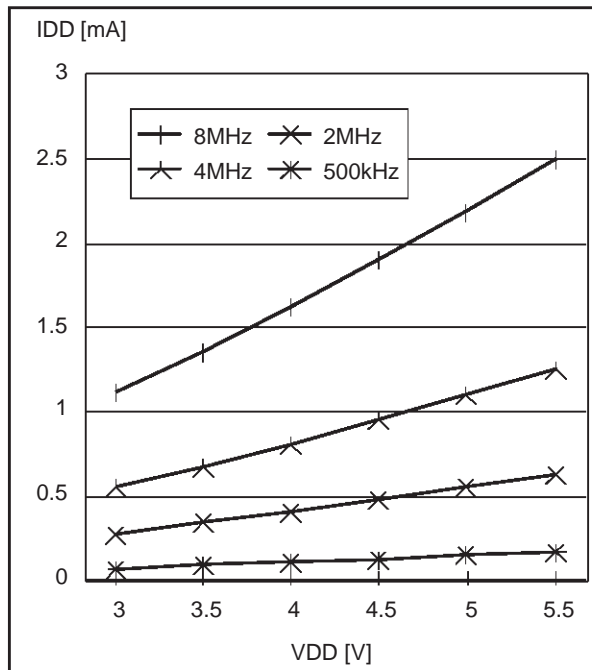
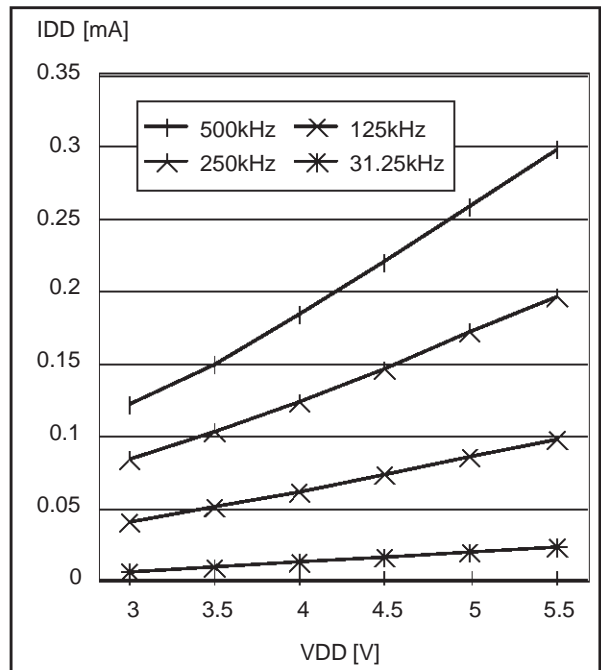


Figure 62. Typical I<sub>DD</sub> in SLOW-WAIT vs. f<sub>CPU</sub>



Notes:

1. Typical data are based on T<sub>A</sub>=25°C, V<sub>DD</sub>=5V (4.5V ≤ V<sub>DD</sub> ≤ 5.5V range) and V<sub>DD</sub>=3.3V (3V ≤ V<sub>DD</sub> ≤ 3.6V range).
2. Data based on characterization results, tested in production at V<sub>DD</sub> max. and f<sub>CPU</sub> max.
3. All I/O pins in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load), all peripherals in reset state; clock input (OSC1) driven by external square wave, CSS and LVD disabled.
4. SLOW-WAIT mode selected with f<sub>CPU</sub> based on f<sub>OSC</sub> divided by 32. All I/O pins in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load), all peripherals in reset state; clock input (OSC1) driven by external square wave, CSS and LVD disabled.

**SUPPLY CURRENT CHARACTERISTICS (Cont'd)**

**13.4.3 HALT Mode**

Symbol	Parameter	Conditions		Typ <sup>1)</sup>	Max	Unit
I <sub>DD</sub>	Supply current in HALT mode <sup>2)</sup>	V <sub>DD</sub> =5.5V	-40°C ≤ T <sub>A</sub> ≤ +85°C	0	10	μA
			-40°C ≤ T <sub>A</sub> ≤ +125°C		50	
		V <sub>DD</sub> =3.6V	-40°C ≤ T <sub>A</sub> ≤ +85°C		6	
			-40°C ≤ T <sub>A</sub> ≤ +125°C		50	

**13.4.4 Supply and Clock Managers**

The previous current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock

source current consumption. To get the total device consumption, the two current values must be added (except for HALT mode).

Symbol	Parameter	Conditions	Typ <sup>1)</sup>	Max <sup>3)</sup>	Unit
I <sub>DD(CK)</sub>	Supply current of internal RC oscillator		500	750	μA
	Supply current of external RC oscillator <sup>4)</sup>		525	750	
	Supply current of resonator oscillator <sup>4) &amp; 5)</sup>	LP: Low power oscillator	200	400	
		MP: Medium power oscillator	300	550	
		MS: Medium speed oscillator	450	750	
HS: High speed oscillator		700	1000		
Clock security system supply current		150	350		
I <sub>DD(LVD)</sub>	LVD supply current	HALT mode	100	150	

**13.4.5 On-Chip Peripherals**

Symbol	Parameter	Conditions		Typ	Unit
I <sub>DD(TIM)</sub>	16-bit Timer supply current <sup>6)</sup>	f <sub>CPU</sub> =8MHz	V <sub>DD</sub> =3.3V	50	μA
			V <sub>DD</sub> =5.0V	150	
I <sub>DD(SPI)</sub>	SPI supply current <sup>7)</sup>	f <sub>CPU</sub> =8MHz	V <sub>DD</sub> =3.3V	250	μA
			V <sub>DD</sub> =5.0V	350	
I <sub>DD(I2C)</sub>	I <sup>2</sup> C supply current <sup>8)</sup>	f <sub>CPU</sub> =8MHz	V <sub>DD</sub> =3.3V	250	μA
			V <sub>DD</sub> =5.0V	350	
I <sub>DD(ADC)</sub>	ADC supply current when converting <sup>9)</sup>	f <sub>ADC</sub> =4MHz	V <sub>DD</sub> =3.3V	800	μA
			V <sub>DD</sub> =5.0V	1100	

**Notes:**

1. Typical data are based on T<sub>A</sub>=25°C.
2. All I/O pins in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load), CSS and LVD disabled. Data based on characterization results, tested in production at V<sub>DD</sub> max. and f<sub>CPU</sub> max.
3. Data based on characterization results, not tested in production.
4. Data based on characterization results done with the external components specified in Section 13.5.3 and Section 13.5.4, not tested in production.
5. As the oscillator is based on a current source, the consumption does not depend on the voltage.
6. Data based on a differential I<sub>DD</sub> measurement between reset configuration (timer counter running at f<sub>CPU</sub>/4) and timer counter stopped (selecting external clock capability). Data valid for one timer.
7. Data based on a differential I<sub>DD</sub> measurement between reset configuration and a permanent SPI master communication (data sent equal to 55h).
8. Data based on a differential I<sub>DD</sub> measurement between reset configuration and I2C peripheral enabled (PE bit set).
9. Data based on a differential I<sub>DD</sub> measurement between reset configuration and continuous A/D conversions.

13.5 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$ .

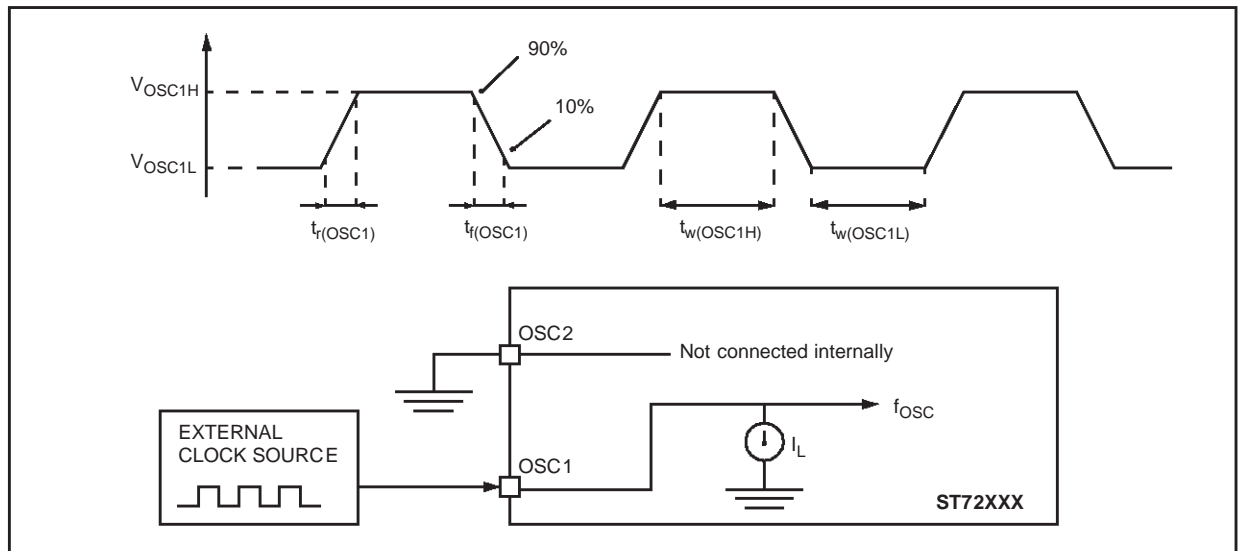
13.5.1 General Timings

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	3	12	$t_{CPU}$
		$f_{CPU}=8MHz$	250	375	1500	ns
$t_{V(IT)}$	Interrupt reaction time <sup>2)</sup> $t_{V(IT)} = \Delta t_{c(INST)} + 10$		10		22	$t_{CPU}$
		$f_{CPU}=8MHz$	1.25		2.75	$\mu s$

13.5.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OSC1H}$	OSC1 input pin high level voltage	see Figure 63	$0.7 \times V_{DD}$		$V_{DD}$	V
$V_{OSC1L}$	OSC1 input pin low level voltage		$V_{SS}$		$0.3 \times V_{DD}$	
$t_{w(OSC1H)}$ $t_{w(OSC1L)}$	OSC1 high or low time <sup>3)</sup>		15			ns
$t_r(OSC1)$ $t_f(OSC1)$	OSC1 rise or fall time <sup>3)</sup>				15	
$I_L$	OSCx Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu A$

Figure 63. Typical Application with an External Clock Source



Notes:

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch.  $\Delta t_{c(INST)}$  is the number of  $t_{CPU}$  cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.



**CLOCK AND TIMING CHARACTERISTICS (Cont'd)**

**13.5.3 Crystal and Ceramic Resonator Oscillators**

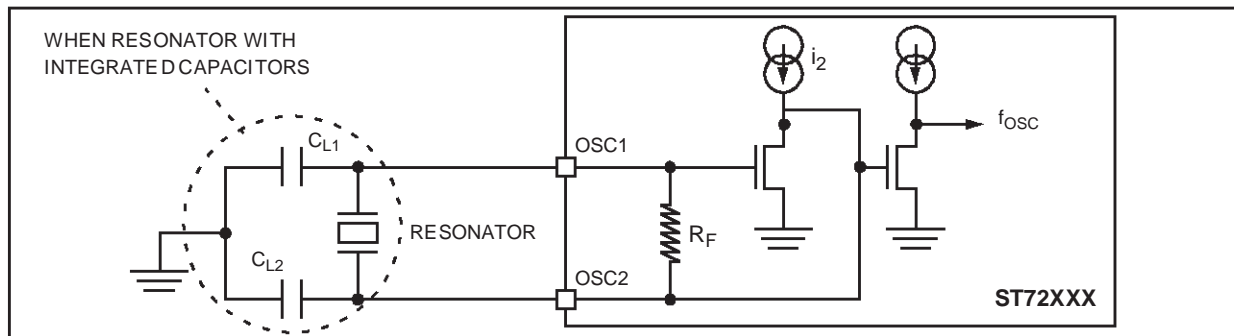
The ST7 internal clock can be supplied with four different Crystal/Ceramic resonator oscillators. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as

close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{OSC}$	Oscillator Frequency <sup>3)</sup>	LP: Low power oscillator MP: Medium power oscillator MS: Medium speed oscillator HS: High speed oscillator	1 >2 >4 >8	2 4 8 16	MHz
$R_F$	Feedback resistor		20	40	k $\Omega$
$C_{L1}$ $C_{L2}$	Recommended load capacitances versus equivalent serial resistance of the crystal or ceramic resonator ( $R_S$ )	$R_S=200\Omega$ LP oscillator $R_S=200\Omega$ MP oscillator $R_S=200\Omega$ MS oscillator $R_S=100\Omega$ HS oscillator	38 32 18 15	56 46 26 21	pF
$i_2$	OSC2 driving current	$V_{DD}=5V$ $V_{IN}=V_{SS}$	40 110 180 400	100 190 360 700	$\mu A$

Oscil.	Typical Crystal or Ceramic Resonators				$C_{L1}$ [pF]	$C_{L2}$ [pF]	$t_{SU(osc)}$ [ms] <sup>2)</sup>		
	Reference	Freq.	Characteristic <sup>1)</sup>						
Crystal	JAUCH	LP	S-200-30-30/50	2MHz	$\Delta f_{OSC}=[\pm 30ppm_{25^\circ C}, \pm 30ppm_{\Delta Ta}]$ , Typ. $R_S=200\Omega$		33	34	10~15
		MP	SS3-400-30-30/30	4MHz	$\Delta f_{OSC}=[\pm 30ppm_{25^\circ C}, \pm 30ppm_{\Delta Ta}]$ , Typ. $R_S=60\Omega$		33	34	7~10
		MS	SS3-800-30-30/30	8MHz	$\Delta f_{OSC}=[\pm 30ppm_{25^\circ C}, \pm 30ppm_{\Delta Ta}]$ , Typ. $R_S=25\Omega$		33	34	2.5~3
		HS	SS3-1600-30-30/30	16MHz	$\Delta f_{OSC}=[\pm 30ppm_{25^\circ C}, \pm 30ppm_{\Delta Ta}]$ , Typ. $R_S=15\Omega$		33	34	1~1.5
Ceramic	MURATA	LP	CSA2.00MG	2MHz	$\Delta f_{OSC}=[\pm 0.5\%_{tolerance}, \pm 0.3\%_{\Delta Ta}, \pm 0.3\%_{aging}, \pm x.x\%_{correl}]$		33	30	4.2
		MP	CSA4.00MG	4MHz	$\Delta f_{OSC}=[\pm 0.5\%_{tolerance}, \pm 0.3\%_{\Delta Ta}, \pm 0.3\%_{aging}, \pm x.x\%_{correl}]$		33	30	2.1
		MS	CSA8.00MTZ	8MHz	$\Delta f_{OSC}=[\pm 0.5\%_{tolerance}, \pm 0.5\%_{\Delta Ta}, \pm 0.3\%_{aging}, \pm x.x\%_{correl}]$		33	30	1.1
		HS	CSA16.00MXZ040	16MHz	$\Delta f_{OSC}=[\pm 0.5\%_{tolerance}, \pm 0.3\%_{\Delta Ta}, \pm 0.3\%_{aging}, \pm x.x\%_{correl}]$		33	30	0.7

**Figure 64. Typical Application with a Crystal or Ceramic Resonator**



**Notes:**

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2.  $t_{SU(OSC)}$  is the typical oscillator start-up time measured between  $V_{DD}=2.8V$  and the fetch of the first instruction (with a quick  $V_{DD}$  ramp-up from 0 to 5V (<50 $\mu s$ ).
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small  $R_S$  value. Refer to crystal/ceramic resonator manufacturer for more details.

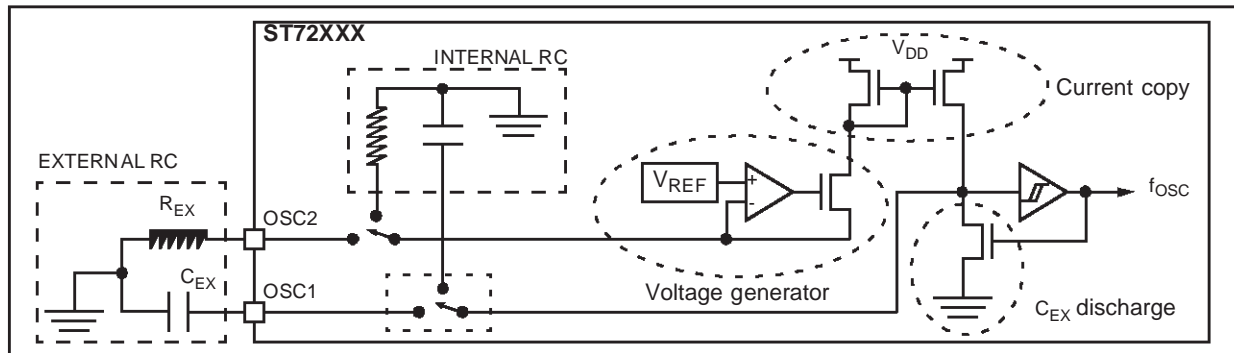
**CLOCK CHARACTERISTICS (Cont'd)**

**13.5.4 RC Oscillators**

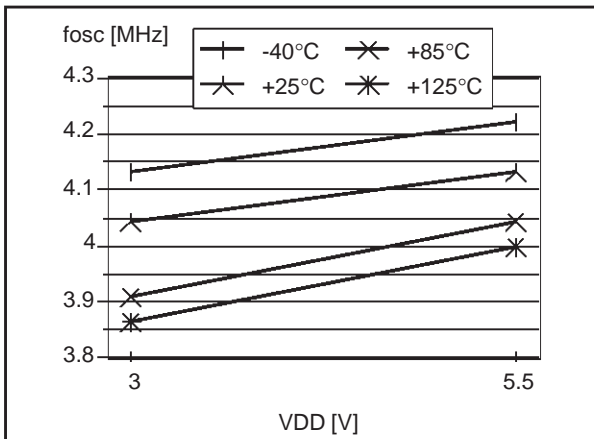
The ST7 internal clock can be supplied with an RC oscillator. This oscillator can be used with internal or external components (selectable by option byte).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>OSC</sub>	Internal RC oscillator frequency <sup>1)</sup>	see Figure 66	3.60		5.10	MHz
	External RC oscillator frequency <sup>2)</sup>		1		14	
t <sub>SU(OSC)</sub>	Internal RC Oscillator Start-up Time <sup>3)</sup>			2.0		ms
	External RC Oscillator Start-up Time <sup>3)</sup>	R <sub>EX</sub> =47KΩ, C <sub>EX</sub> =∞pF		1.0		
		R <sub>EX</sub> =47KΩ, C <sub>EX</sub> =100pF		6.5		
		R <sub>EX</sub> =10KΩ, C <sub>EX</sub> =6.8pF		0.7		
R <sub>EX</sub> =10KΩ, C <sub>EX</sub> =470pF		3.0				
R <sub>EX</sub>	Oscillator external resistor <sup>4)</sup>	see Figure 67	10		47	KΩ
C <sub>EX</sub>	Oscillator external capacitor		0 <sup>5)</sup>		470	pF

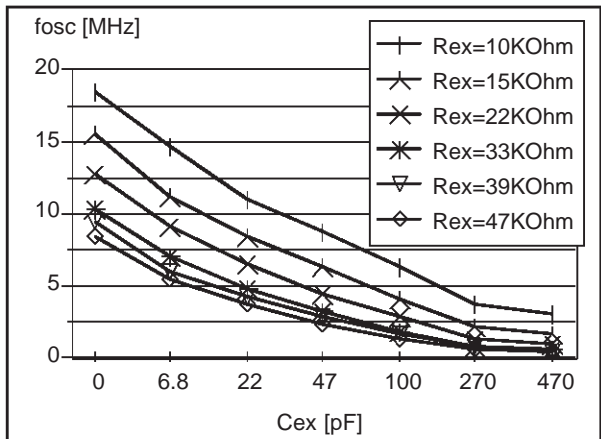
**Figure 65. Typical Application with RC oscillator**



**Figure 66. Typical Internal RC Oscillator**



**Figure 67. Typical External RC Oscillator**



**Notes:**

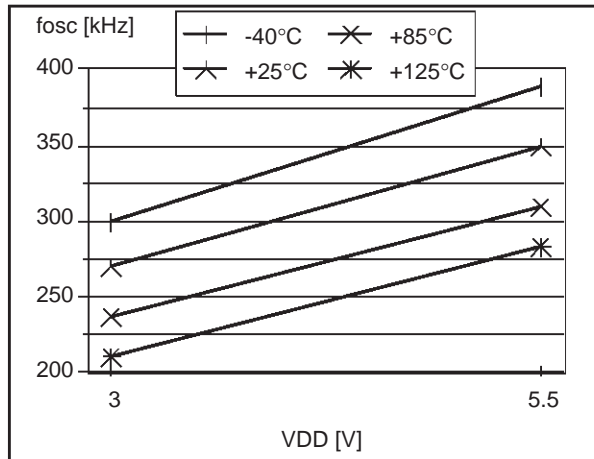
1. Data based on characterization results.
2. Guaranteed frequency range with the specified C<sub>EX</sub> and R<sub>EX</sub> ranges taking into account the device process variation. Data based on design simulation.
3. Data based on characterization results done with V<sub>DD</sub> nominal at 5V, not tested in production.
4. R<sub>EX</sub> must have a positive temperature coefficient (ppm/°C), carbon resistors should therefore not be used.
5. **Important:** when no external C<sub>EX</sub> is applied, the capacitance to be considered is the global parasitic capacitance which is subject to high variation (package, application...). In this case, the RC oscillator frequency tuning has to be done by trying out several resistor values.

**CLOCK CHARACTERISTICS (Cont'd)**

**13.5.5 Clock Security System (CSS)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>SFOSC</sub>	Safe Oscillator Frequency <sup>1)</sup>	T <sub>A</sub> =25°C, V <sub>DD</sub> =5.0V	250	340	430	kHz
		T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V	190	260	330	
f <sub>GFOSC</sub>	Glitch Filtered Frequency <sup>2)</sup>			30		MHz

**Figure 68. Typical Safe Oscillator Frequencies**



**Note:**

1. Data based on characterization results, tested in production between 90KHz and 500KHz.
2. Filtered glitch on the f<sub>OSC</sub> signal. See functional description in Section 6.5 on page 23 for more details.

### 13.6 MEMORY CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

#### 13.6.1 RAM and Hardware Registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RM}$	Data retention mode <sup>1)</sup>	HALT mode (or RESET)	1.6			V

#### 13.6.2 FLASH Program Memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{A(prog)}$	Programming temperature range <sup>2)</sup>		0	25	70	°C
$t_{prog}$	Programming time for 1~16 bytes <sup>3)</sup>	$T_A=+25^{\circ}C$		8	25	ms
	Programming time for 4 or 8kBytes	$T_A=+25^{\circ}C$		2.1	6.4	sec
$t_{ret}$	Data retention <sup>5)</sup>	$T_A=+55^{\circ}C$ <sup>4)</sup>	20			years
$N_{RW}$	Write erase cycles <sup>5)</sup>	$T_A=+25^{\circ}C$	100			cycles

**Notes:**

1. Minimum  $V_{DD}$  supply voltage without losing data stored in RAM (in in HALT mode or under RESET) or in hardware registers (only in HALT mode). Guaranteed by construction, not tested in production.
2. Data based on characterization results, tested in production at  $T_A=25^{\circ}C$ .
3. Up to 16 bytes can be programmed at a time for a 4kBytes FLASH block (then up to 32 bytes at a time for an 8k device)
4. The data retention time increases when the  $T_A$  decreases.
5. Data based on reliability test results and monitored in production.

**13.7 EMC CHARACTERISTICS**

Susceptibility tests are performed on a sample basis during product characterization.

**13.7.1 Functional EMS**

(Electro Magnetic Susceptibility)

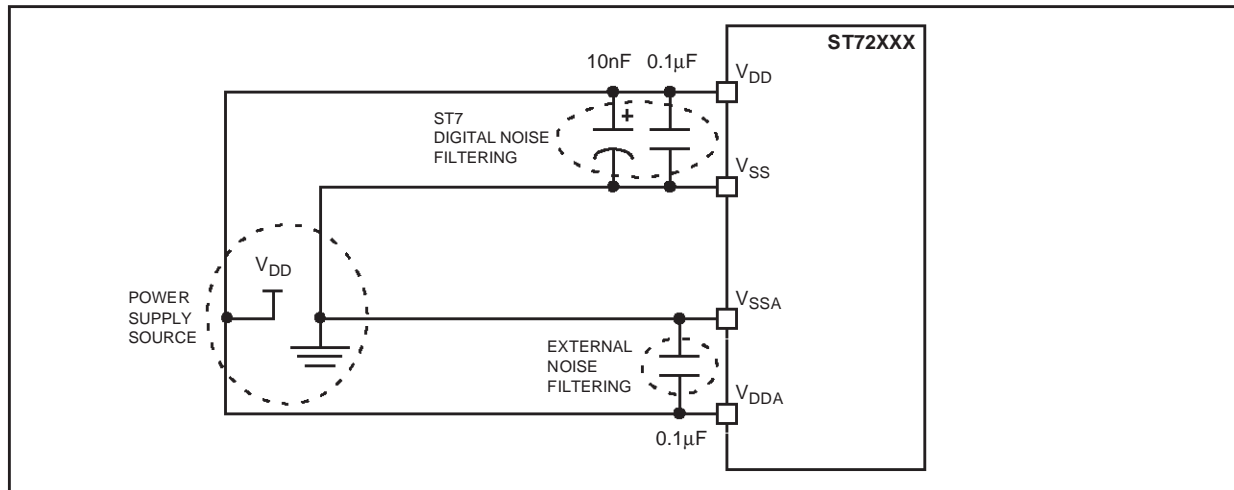
Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD:** Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

Symbol	Parameter	Condition s	Neg <sup>1)</sup>	Pos <sup>1)</sup>	Unit
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD}=5V, T_A=+25^{\circ}C, f_{OSC}=8MHz$ conforms to IEC 1000-4-2	-1	1	kV
$V_{FFTB}$	Fast transient voltage burst limits to be applied through 100pF on $V_{DD}$ and $V_{DD}$ pins to induce a functional disturbance	$V_{DD}=5V, T_A=+25^{\circ}C, f_{OSC}=8MHz$ conforms to IEC 1000-4-4	-4	4	

Figure 69. EMC Recommended star network power supply connection <sup>2)</sup>



**Notes:**

1. Data based on characterization results, not tested in production.
2. The suggested 10nF and 0.1µF decoupling capacitors on the power supply lines are proposed as a good price vs. EMC performance tradeoff. They have to be put as close as possible to the device power supply pins. Other EMC recommendations are given in other sections (I/Os, RESET, OSCx pin characteristics).

**EMC CHARACTERISTICS (Cont'd)**

**13.7.2 Absolute Electrical Sensitivity**

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the AN1181 ST7 application note.

**13.7.2.1 Electro-Static Discharge (ESD)**

Electro-Static Discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends of the number of supply pins of the device (3 parts\*(n+1) supply pin). Two models are usually simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard. See Figure 70 and the following test sequences.

**Human Body Model Test Sequence**

- C<sub>L</sub> is loaded through S1 by the HV pulse generator.
- S1 switches position from generator to R.
- A discharge from C<sub>L</sub> through R (body resistance) to the ST7 occurs.
- S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST7 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.

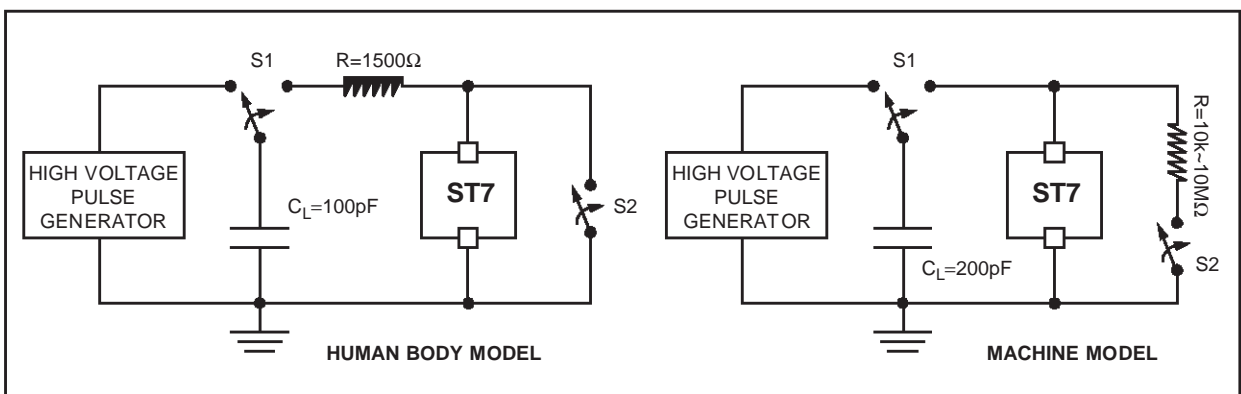
**Machine Model Test Sequence**

- C<sub>L</sub> is loaded through S1 by the HV pulse generator.
- S1 switches position from generator to ST7.
- A discharge from C<sub>L</sub> to the ST7 occurs.
- S2 must be closed 10 to 100ms after the pulse delivery period to ensure the ST7 is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.
- R (machine resistance), in series with S2, ensures a slow discharge of the ST7.

**Absolute Maximum Ratings**

Symbol	Ratings	Conditions	Maximum value <sup>1)</sup>	Unit
V <sub>ESD(HBM)</sub>	Electro-static discharge voltage (Human Body Model)	T <sub>A</sub> =+25°C	2000	V
V <sub>ESD(MM)</sub>	Electro-static discharge voltage (Machine Model)	T <sub>A</sub> =+25°C	200	

**Figure 70. Typical Equivalent ESD Circuits**



**Notes:**

1. Data based on characterization results, not tested in production.

**EMC CHARACTERISTICS (Cont'd)**

**13.7.2.2 Static and Dynamic Latch-Up**

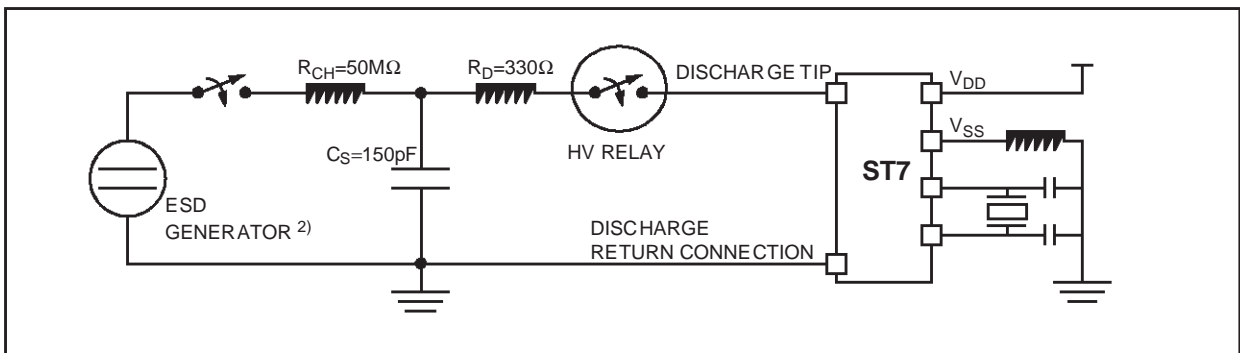
■ **LU:** 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin), a current injection (applied to each input, output and configurable I/O pin) and a power supply switch sequence are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the AN1181 ST7 application note.

■ **DLU:** Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards and is described in Figure 71. For more details, refer to the AN1181 ST7 application note.

**Electrical Sensitivities**

Symbol	Parameter	Conditions	Class <sup>1)</sup>
LU	Static latch-up class	T <sub>A</sub> =+25°C T <sub>A</sub> =+85°C	A A
DLU	Dynamic latch-up class	V <sub>DD</sub> =5.5V, f <sub>OSC</sub> =4MHz, T <sub>A</sub> =+25°C	A

**Figure 71. Simplified Diagram of the ESD Generator for DLU**



**Notes:**

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).
2. Schaffner NSG435 with a pointed test finger.

EMC CHARACTERISTICS (Cont'd)

13.7.3 ESD Pin Protection Strategy

To protect an integrated circuit against Electro-Static Discharge the stress must be controlled to prevent degradation or destruction of the circuit elements. The stress generally affects the circuit elements which are connected to the pads but can also affect the internal devices when the supply pads receive the stress. The elements to be protected must not receive excessive current, voltage or heating within their structure.

An ESD network combines the different input and output ESD protections. This network works, by allowing safe discharge paths for the pins subjected to ESD stress. Two critical ESD stress cases are presented in Figure 72 and Figure 73 for standard pins and in Figure 74 and Figure 75 for true open drain pins.

Standard Pin Protection

To protect the output structure the following elements are added:

- A diode to  $V_{DD}$  (3a) and a diode from  $V_{SS}$  (3b)
- A protection device between  $V_{DD}$  and  $V_{SS}$  (4)

To protect the input structure the following elements are added:

- A resistor in series with the pad (1)
- A diode to  $V_{DD}$  (2a) and a diode from  $V_{SS}$  (2b)
- A protection device between  $V_{DD}$  and  $V_{SS}$  (4)

Figure 72. Positive Stress on a Standard Pad vs.  $V_{SS}$

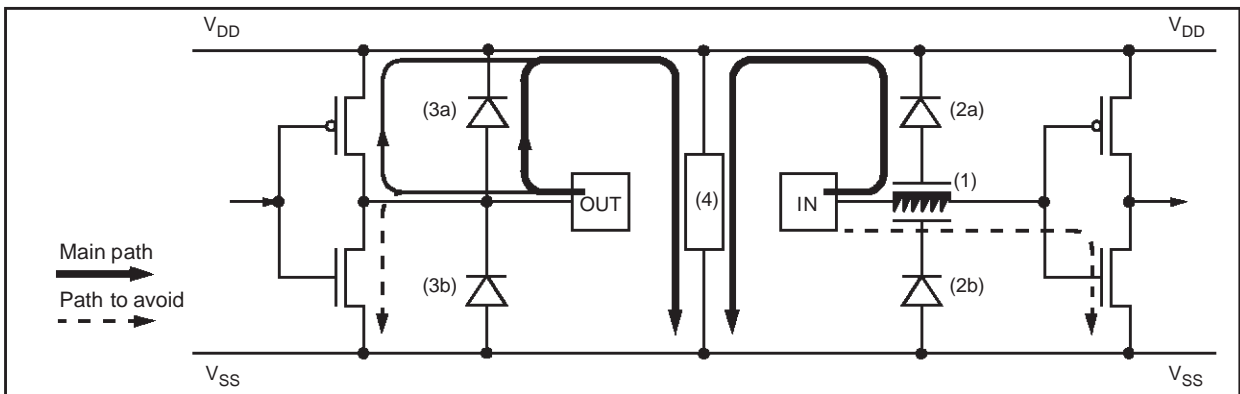
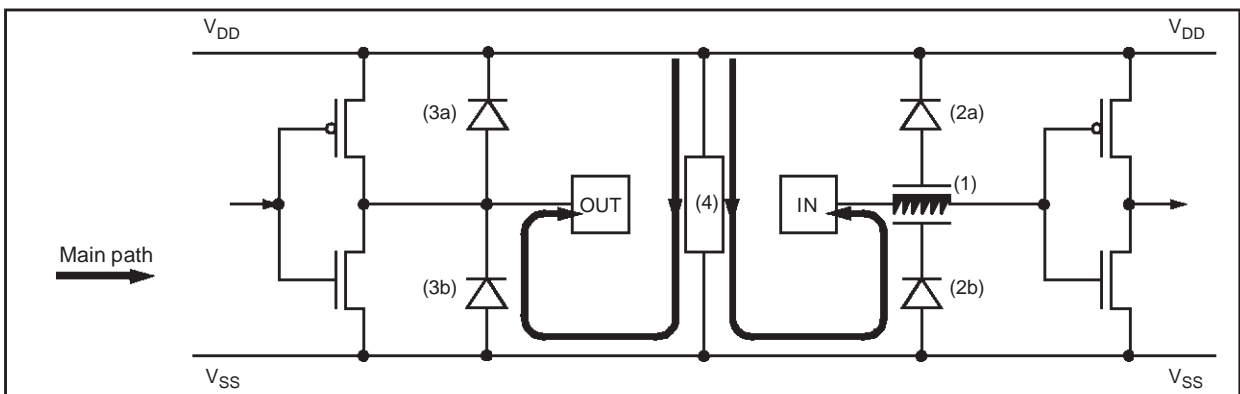


Figure 73. Negative Stress on a Standard Pad vs.  $V_{DD}$





**EMC CHARACTERISTICS (Cont'd)**

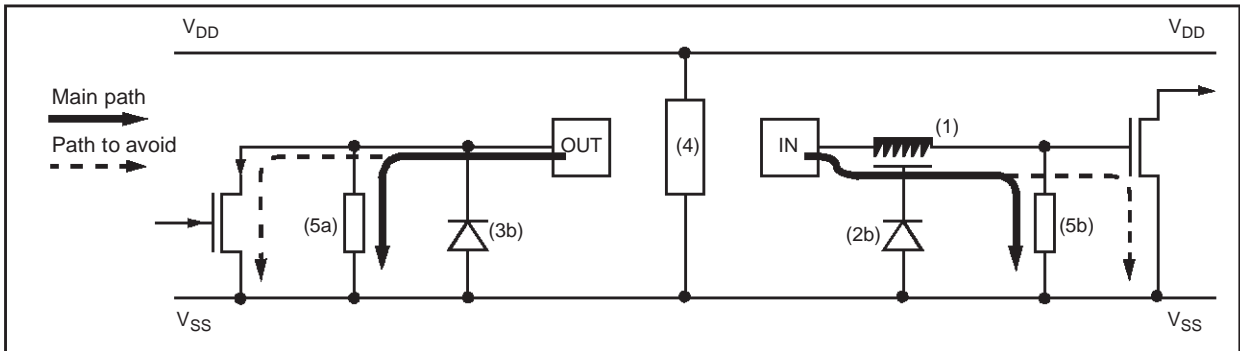
**True Open Drain Pin Protection**

The centralized protection (4) is not involved in the discharge of the ESD stresses applied to true open drain pads due to the fact that a P-Buffer and diode to  $V_{DD}$  are not implemented. An additional local protection between the pad and  $V_{SS}$  (5a & 5b) is implemented to completely absorb the positive ESD discharge.

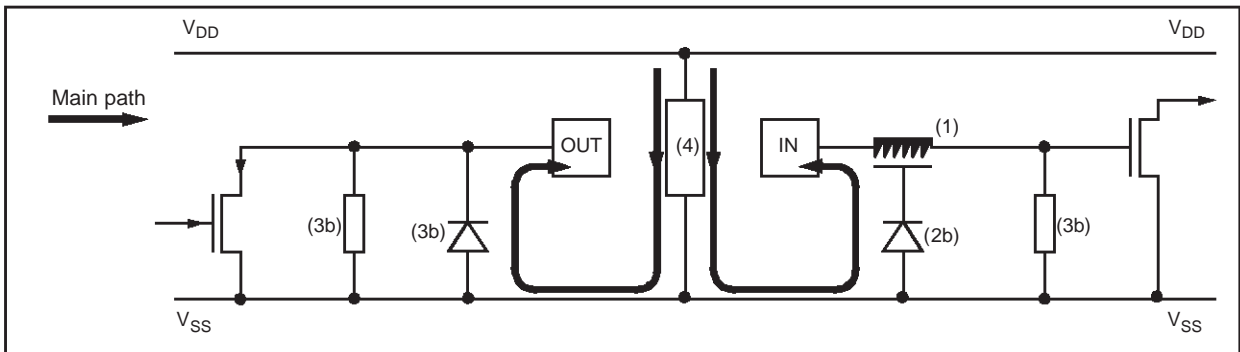
**Multisupply Configuration**

When several types of ground ( $V_{SS}$ ,  $V_{SSA}$ , ...) and power supply ( $V_{DD}$ ,  $V_{DDA}$ , ...) are available for any reason (better noise immunity...), the structure shown in Figure 76 is implemented to protect the device against ESD.

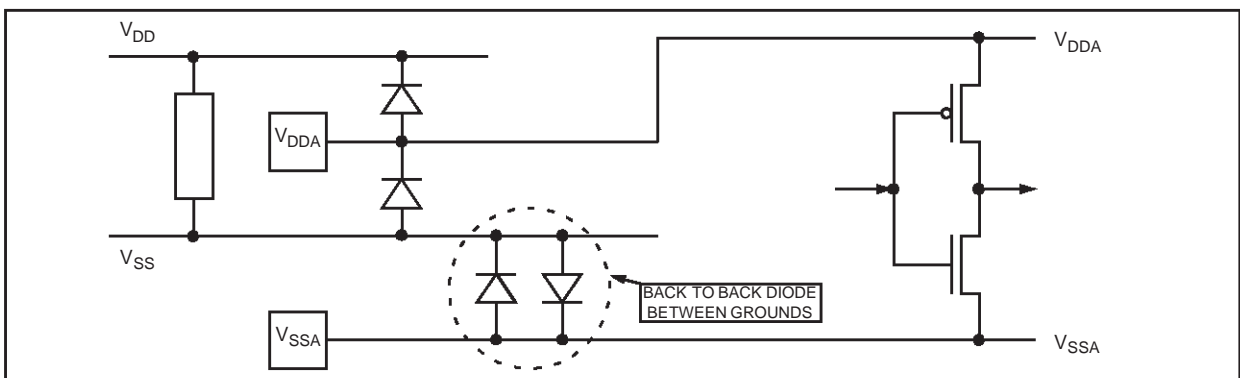
**Figure 74. Positive Stress on a True Open Drain Pad vs.  $V_{SS}$**



**Figure 75. Negative Stress on a True Open Drain Pad vs.  $V_{DD}$**



**Figure 76. Multisupply Configuration**



13.8 I/O PORT PIN CHARACTERISTICS

13.8.1 General Characteristics

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit	
$V_{IL}$	Input low level voltage <sup>2)</sup>				$0.3 \times V_{DD}$	V	
$V_{IH}$	Input high level voltage <sup>2)</sup>		$0.7 \times V_{DD}$				
$V_{hys}$	Schmitt trigger voltage hysteresis <sup>3)</sup>			400		mV	
$I_L$	Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu A$	
$I_S$	Static current consumption <sup>4)</sup>	Floating input mode			200		
$R_{PU}$	Weak pull-up equivalent resistor <sup>5)</sup>	$V_{IN} = V_{SS}$	$V_{DD} = 5V$ $V_{DD} = 3.3V$	80 170	120 200	250 230	k $\Omega$
$C_{IO}$	I/O pin capacitance			5		pF	
$t_{f(I/O)out}$	Output high to low level fall time <sup>6)</sup>	$C_L = 50pF$ Between 10% and 90%		25		ns	
$t_{r(I/O)out}$	Output low to high level rise time <sup>6)</sup>			25			
$t_{w(IT)in}$	External interrupt pulse time <sup>7)</sup>		1			$t_{CPU}$	

Figure 77. Two typical Applications with unused I/O Pin

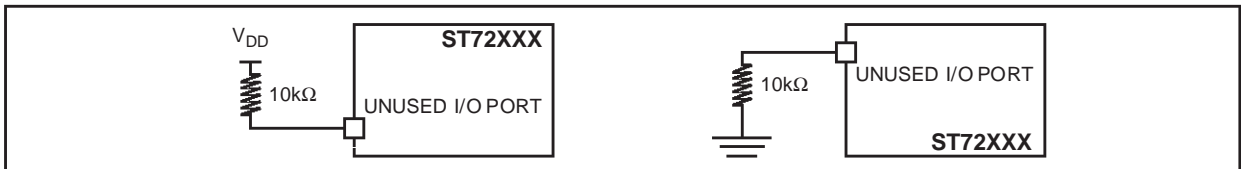
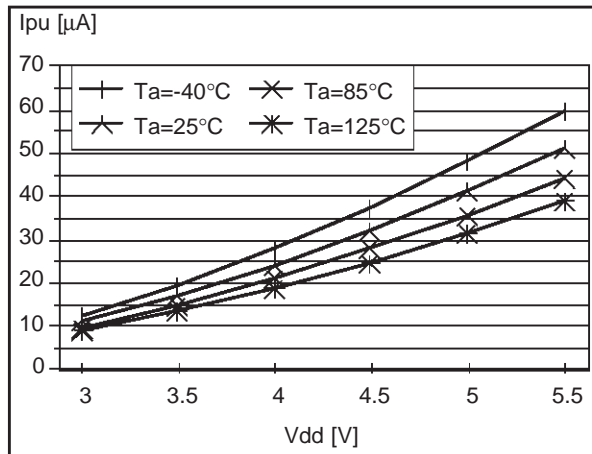


Figure 78. Typical  $I_{PU}$  vs.  $V_{DD}$  with  $V_{IN} = V_{SS}$



Notes:

1. Unless otherwise specified, typical data are based on  $T_A = 25^\circ C$  and  $V_{DD} = 5V$ .
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see Figure 77). Data based on design simulation and/or technology characteristics, not tested in production.
5. The  $R_{PU}$  pull-up equivalent resistor is based on a resistive transistor (corresponding  $I_{PU}$  current characteristics described in Figure 78). This data is based on characterization results, tested in production at  $V_{DD}$  max.
6. Data based on characterization results, not tested in production.
7. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

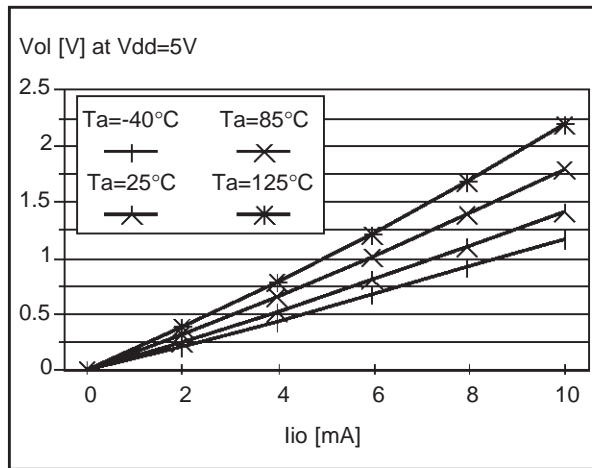
**I/O PORT PIN CHARACTERISTICS (Cont'd)**

**13.8.2 Output Driving Current**

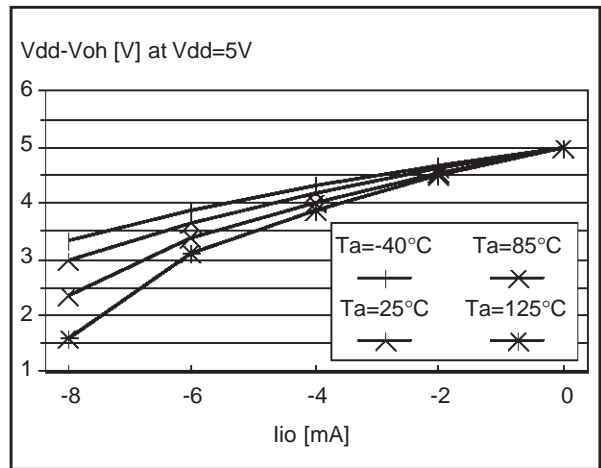
Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{1)}$	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 79 and Figure 82)	$I_{IO}=+5mA$		1.2	V
		$I_{IO}=+2mA$		0.5	
	$I_{IO}=+20mA, T_A \leq 85^\circ C$ $T_A \geq 85^\circ C$		1.3		
			1.5		
Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 80 and Figure 83)	$I_{IO}=+8mA$		0.6		
	$I_{IO}=-5mA, T_A \leq 85^\circ C$ $T_A \geq 85^\circ C$	$V_{DD}-1.4$			
$V_{DD}-1.6$					
$V_{OH}^{2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 81 and Figure 84)	$I_{IO}=-2mA$	$V_{DD}-0.7$		

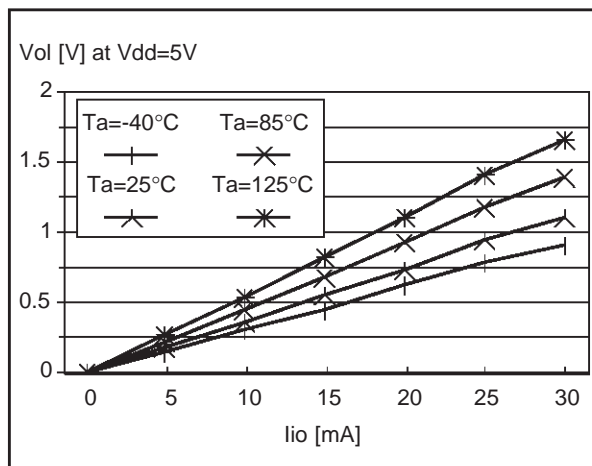
**Figure 79. Typical  $V_{OL}$  at  $V_{DD}=5V$  (standard)**



**Figure 81. Typical  $V_{DD}-V_{OH}$  at  $V_{DD}=5V$**



**Figure 80. Typical  $V_{OL}$  at  $V_{DD}=5V$  (high-sink)**



**Notes:**

1. The  $I_{IO}$  current sunk must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. The  $I_{IO}$  current sourced must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ . True open drain I/O pins does not have  $V_{OH}$ .

I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 82. Typical  $V_{OL}$  vs.  $V_{DD}$  (standard I/Os)

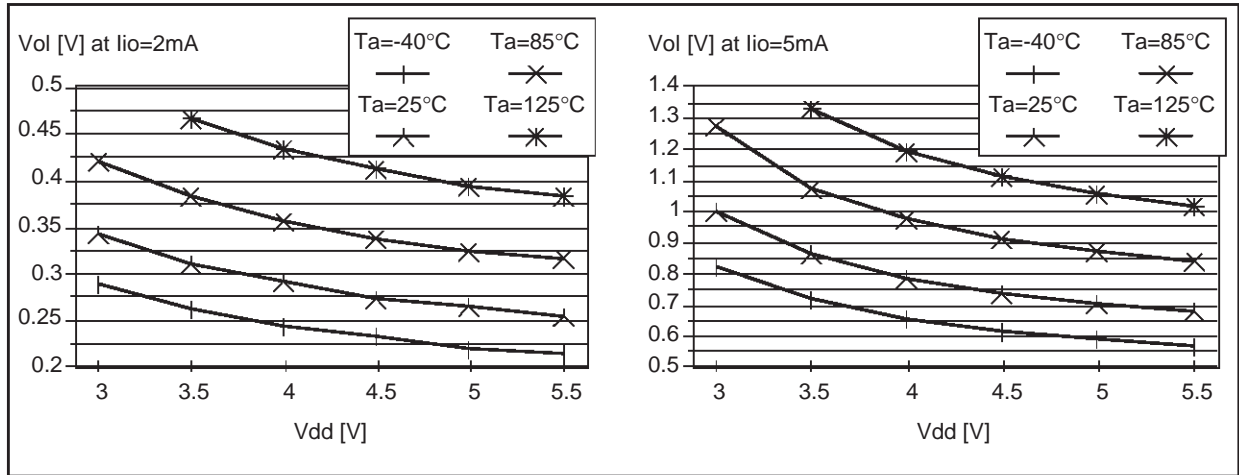


Figure 83. Typical  $V_{OL}$  vs.  $V_{DD}$  (high-sink I/Os)

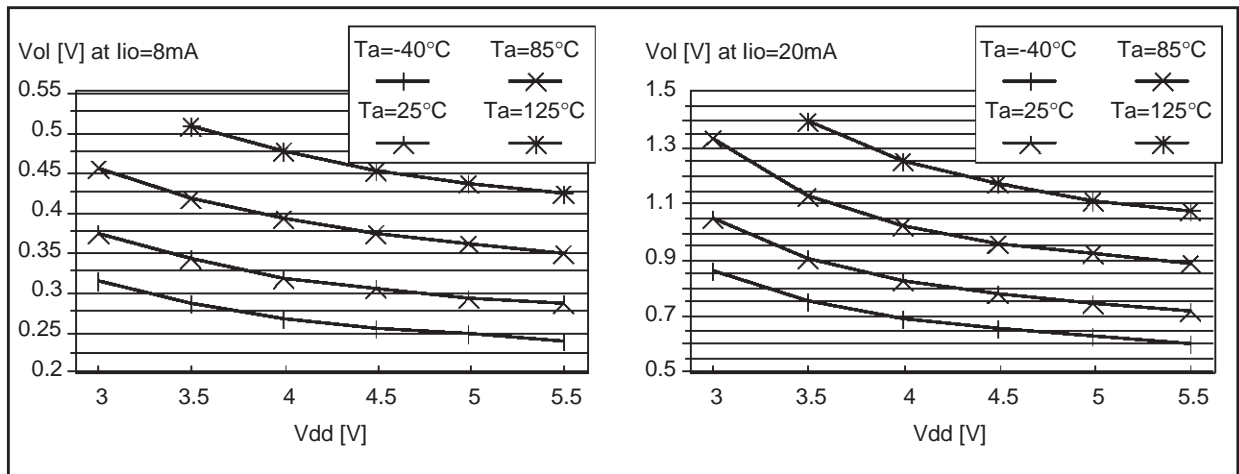
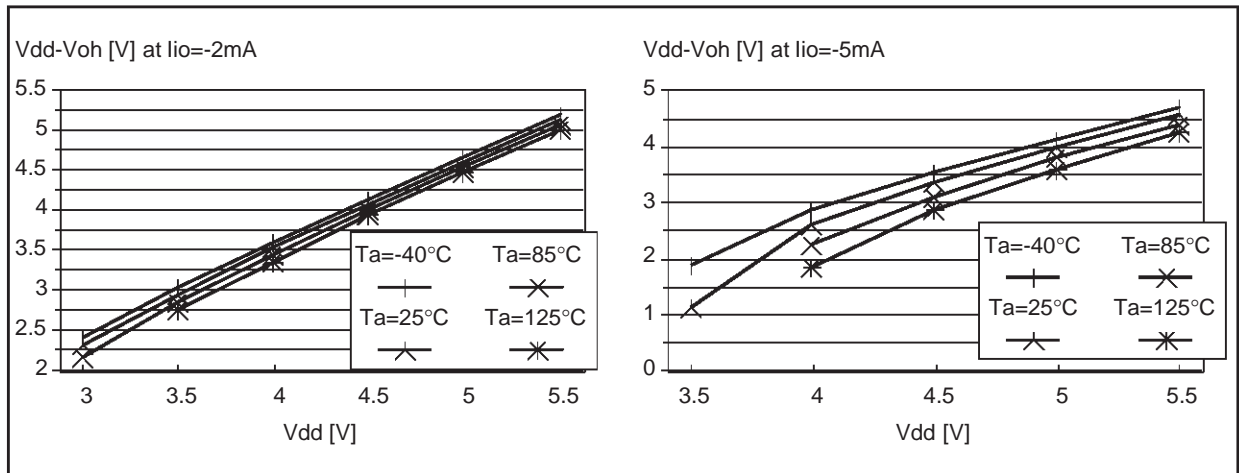


Figure 84. Typical  $V_{DD}-V_{OH}$  vs.  $V_{DD}$



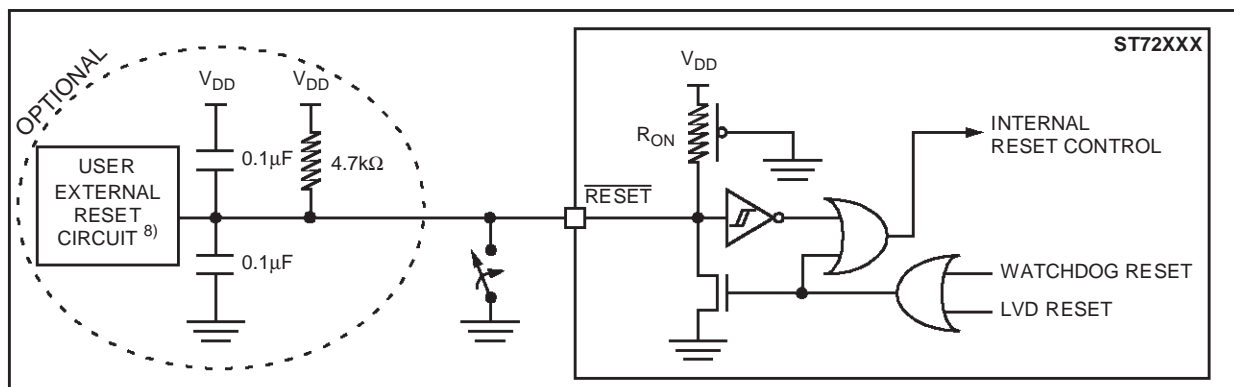
13.9 CONTROL PIN CHARACTERISTICS

13.9.1 Asynchronous  $\overline{\text{RESET}}$  Pin

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit	
$V_{IL}$	Input low level voltage <sup>2)</sup>				$0.3 \times V_{DD}$	V	
$V_{IH}$	Input high level voltage <sup>2)</sup>		$0.7 \times V_{DD}$				
$V_{hys}$	Schmitt trigger voltage hysteresis <sup>3)</sup>			400		mV	
$V_{OL}$	Output low level voltage <sup>4)</sup> (see Figure 87, Figure 88)	$V_{DD}=5V$	$I_{IO}=+5mA$		0.68	0.95	V
			$I_{IO}=+2mA$		0.28	0.45	
$R_{ON}$	Weak pull-up equivalent resistor <sup>5)</sup>	$V_{IN}=V_{SS}$	$V_{DD}=5V$	20	40	60	k $\Omega$
			$V_{DD}=3.3V$	80	100	120	
$t_{w(RSTL)out}$	Generated reset pulse duration	External pin or internal reset sources		6 30		$1/f_{SFOSC}$ $\mu s$	
$t_{h(RSTL)in}$	External reset pulse hold time <sup>6)</sup>		20			$\mu s$	
$t_{g(RSTL)in}$	Filtered glitch duration <sup>7)</sup>				100	ns	

Figure 85. Typical Application with  $\overline{\text{RESET}}$  pin<sup>8)</sup>



Notes:

1. Unless otherwise specified, typical data are based on  $T_A=25^\circ C$  and  $V_{DD}=5V$ .
  2. Data based on characterization results, not tested in production.
  3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
  4. The  $I_{IO}$  current sunk must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
  5. The  $R_{ON}$  pull-up equivalent resistor is based on a resistive transistor (corresponding  $I_{ON}$  current characteristics described in Figure 86). This data is based on characterization results, not tested in production.
  6. To guarantee the reset of the device, a minimum pulse has to be applied to  $\overline{\text{RESET}}$  pin.
  7. All short pulse applied on  $\overline{\text{RESET}}$  pin with a duration below  $t_{h(RSTL)in}$  can be ignored.
  8. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in a noisy environment.
9. The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).

CONTROL PIN CHARACTERISTICS (Cont'd)

Figure 86. Typical  $I_{ON}$  vs.  $V_{DD}$  with  $V_{IN}=V_{SS}$

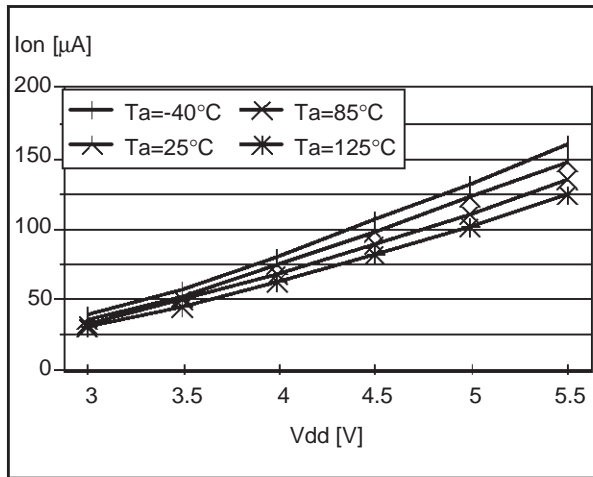


Figure 87. Typical  $V_{OL}$  at  $V_{DD}=5V$  ( $\overline{\text{RESET}}$ )

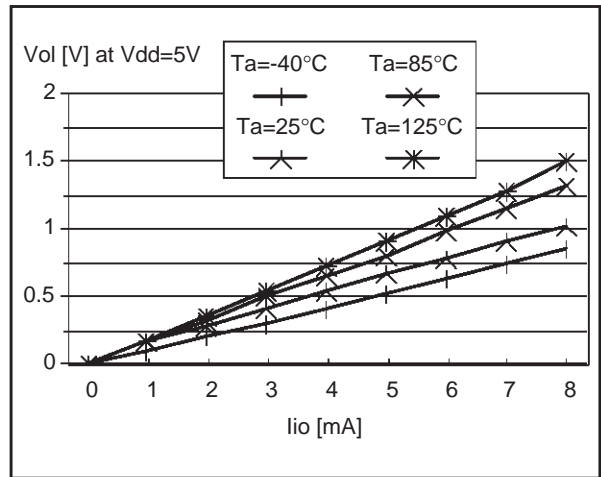
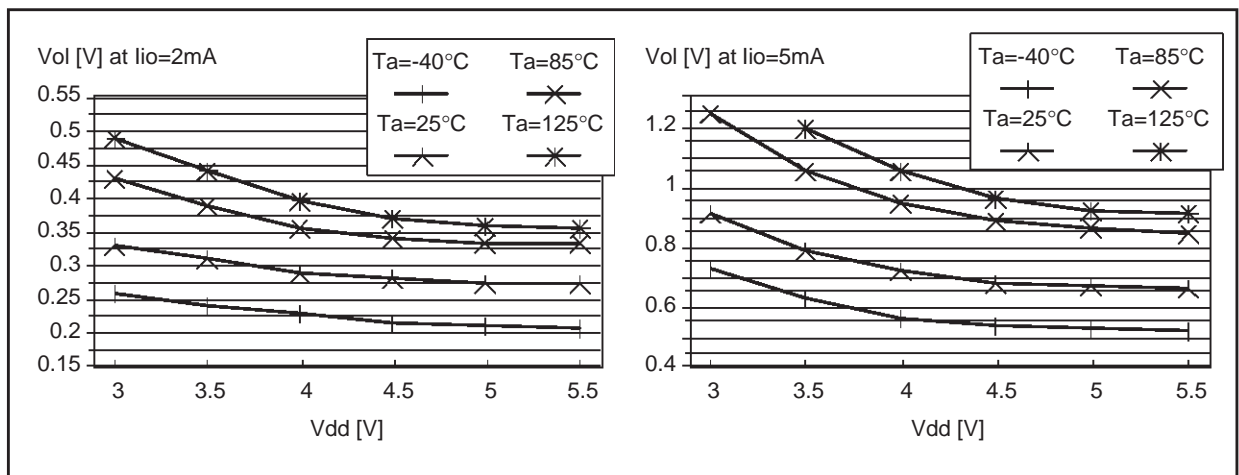


Figure 88. Typical  $V_{OL}$  vs.  $V_{DD}$  ( $\overline{\text{RESET}}$ )



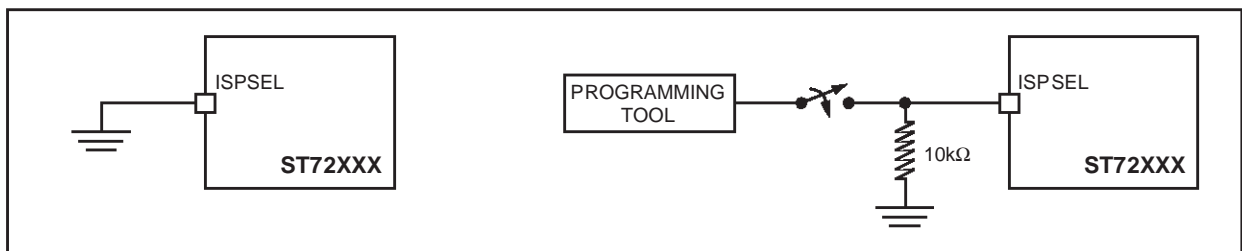
**CONTROL PIN CHARACTERISTICS (Cont'd)**

**13.9.2 ISPSEL Pin**

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IL}$	Input low level voltage <sup>1)</sup>		$V_{SS}$	0.2	V
$V_{IH}$	Input high level voltage <sup>1)</sup>		$V_{DD}-0.1$	12.6	
$I_L$	Input leakage current	$V_{IN}=V_{SS}$		$\pm 1$	$\mu A$

**Figure 89. Two typical Applications with ISPSEL Pin <sup>2)</sup>**



**Notes:**

1. Data based on design simulation and/or technology characteristics, not tested in production.
2. When the ISP Remote mode is not required by the application ISPSEL pin must be tied to  $V_{SS}$ .

**13.10 TIMER PERIPHERAL CHARACTERISTICS**

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

**13.10.1 Watchdog Timer**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(WDG)}$	Watchdog time-out duration		12,288		786,432	$t_{CPU}$
		$f_{CPU}=8MHz$	1.54		98.3	ms

**13.10.2 16-Bit Timer**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		1			$t_{CPU}$
$t_{res(PWM)}$	PWM resolution time		2			$t_{CPU}$
		$f_{CPU}=8MHz$	250			ns
$f_{EXT}$	Timer external clock frequency		0		$f_{CPU}/4$	MHz
$f_{PWM}$	PWM repetition rate		0		$f_{CPU}/4$	MHz
$Res_{PWM}$	PWM resolution				16	bit



13.11 COMMUNICATION INTERFACE CHARACTERISTICS

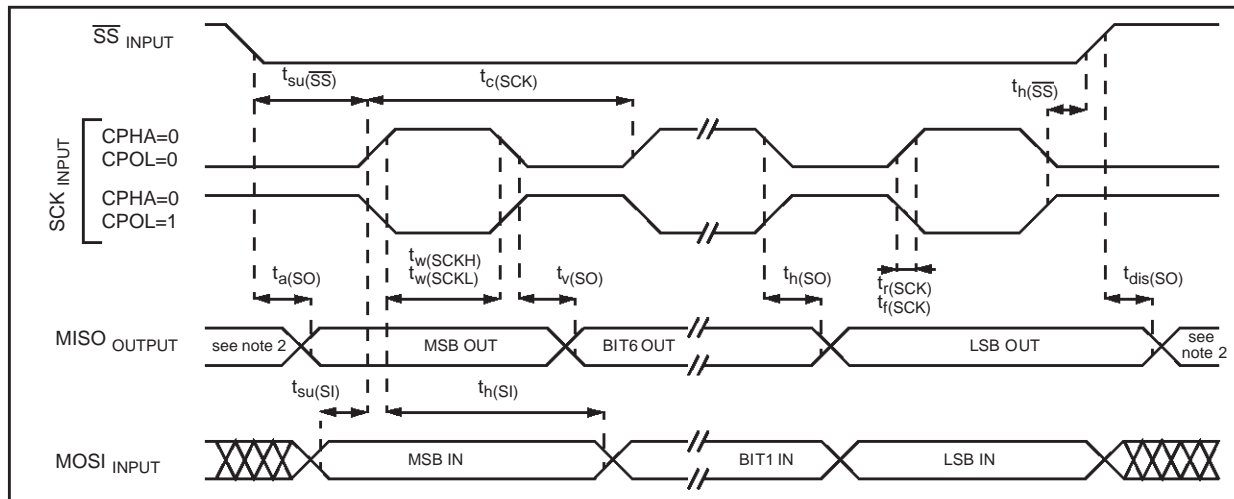
13.11.1 SPI - Serial Peripheral Interface

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics ( $\overline{SS}$ , SCK, MOSI, MISO).

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}$ 1/ $t_c(SCK)$	SPI clock frequency	Master $f_{CPU}=8MHz$	$f_{CPU}/128$ 0.0625	$f_{CPU}/4$ 2	MHz
		Slave $f_{CPU}=8MHz$	0	$f_{CPU}/2$ 4	
$t_r(SCK)$ $t_f(SCK)$	SPI clock rise and fall time		see I/O port pin description		
$t_{su}(\overline{SS})$	$\overline{SS}$ setup time	Slave	120		ns
$t_h(\overline{SS})$	$\overline{SS}$ hold time	Slave	120		
$t_w(SCKH)$ $t_w(SCKL)$	SCK high and low time	Master	100		
		Slave	90		
$t_{su}(MI)$ $t_{su}(SI)$	Data input setup time	Master	100		
		Slave	100		
$t_h(MI)$ $t_h(SI)$	Data input hold time	Master	100		
		Slave	100		
$t_a(SO)$	Data output access time	Slave	0	120	
$t_{dis}(SO)$	Data output disable time	Slave		240	
$t_v(SO)$	Data output valid time	Slave (after enable edge)		120	
$t_h(SO)$	Data output hold time		0		
$t_v(MO)$	Data output valid time	Master (before capture edge)	0.25		$t_{CPU}$
$t_h(MO)$	Data output hold time		0.25		

Figure 90. SPI Slave Timing Diagram with CPHA=0<sup>3)</sup>



Notes:

1. Data based on design simulation and/or characterisation results, not tested in production.
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends on the I/O port configuration.
3. Measurement points are done at CMOS levels:  $0.3xV_{DD}$  and  $0.7xV_{DD}$ .

COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

Figure 91. SPI Slave Timing Diagram with CPHA=1<sup>1)</sup>

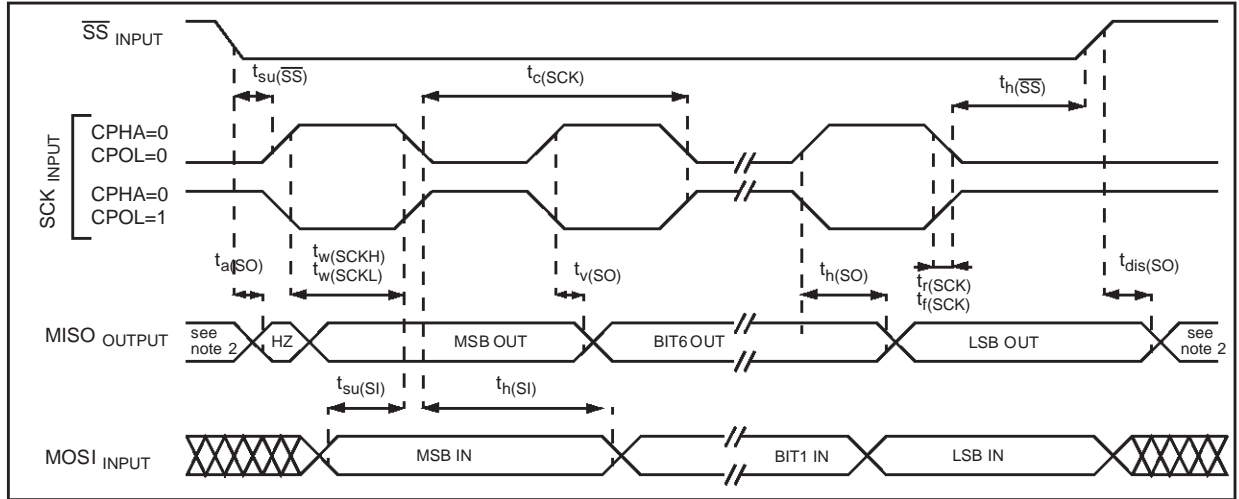
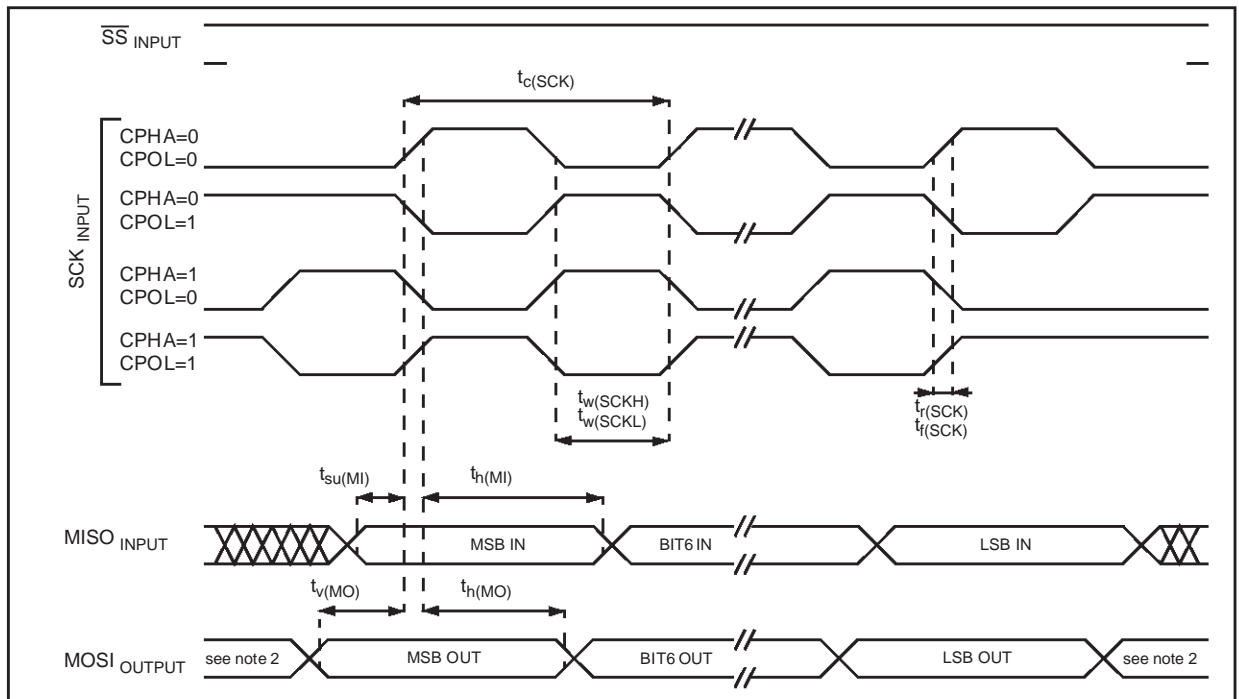


Figure 92. SPI Master Timing Diagram <sup>1)</sup>



Notes:

1. Measurement points are done at CMOS levels:  $0.3 \times V_{DD}$  and  $0.7 \times V_{DD}$ .
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends of the I/O port configuration.

COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

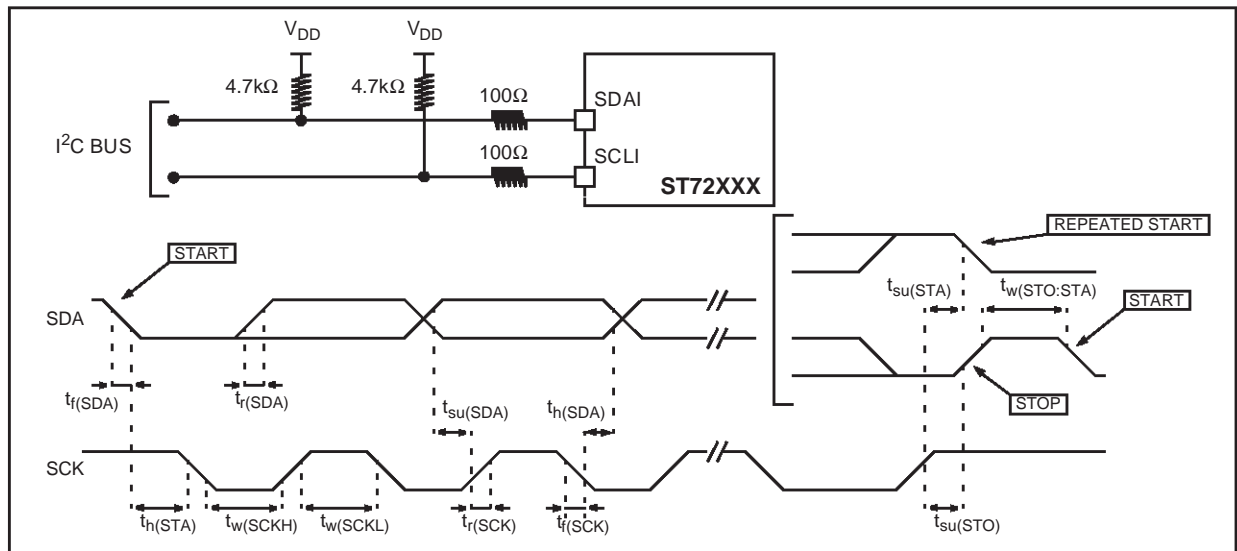
13.11.2 I<sup>2</sup>C - Inter IC Control Interface

Subject to general operating conditions for V<sub>DD</sub>, f<sub>OSC</sub>, and T<sub>A</sub> unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDAI and SCLI). The ST7 I<sup>2</sup>C interface meets the requirements of the Standard I<sup>2</sup>C communication protocol described in the following table.

Symbol	Parameter	Standard mode I <sup>2</sup> C		Fast mode I <sup>2</sup> C		Unit
		Min <sup>1)</sup>	Max <sup>1)</sup>	Min <sup>1)</sup>	Max <sup>1)</sup>	
t <sub>w</sub> (SCLL)	SCL clock low time	4.7		1.3		μs
t <sub>w</sub> (SCLH)	SCL clock high time	4.0		0.6		
t <sub>su</sub> (SDA)	SDA setup time	250		100		ns
t <sub>h</sub> (SDA)	SDA data hold time	0 <sup>3)</sup>		0 <sup>2)</sup>	900 <sup>3)</sup>	
t <sub>r</sub> (SDA) t <sub>r</sub> (SCL)	SDA and SCL rise time		1000	20+0.1C <sub>b</sub>	300	
t <sub>f</sub> (SDA) t <sub>f</sub> (SCL)	SDA and SCL fall time		300	20+0.1C <sub>b</sub>	300	
t <sub>h</sub> (STA)	START condition hold time	4.0		0.6		μs
t <sub>su</sub> (STA)	Repeated START condition setup time	4.7		0.6		
t <sub>su</sub> (STO)	STOP condition setup time	4.0		0.6		ns
t <sub>w</sub> (STO:STA)	STOP to START condition time (bus free)	4.7		1.3		ms
C <sub>b</sub>	Capacitive load for each bus line		400		400	pF

Figure 93. Typical Application with I<sup>2</sup>C Bus and Timing Diagram <sup>4)</sup>



Notes:

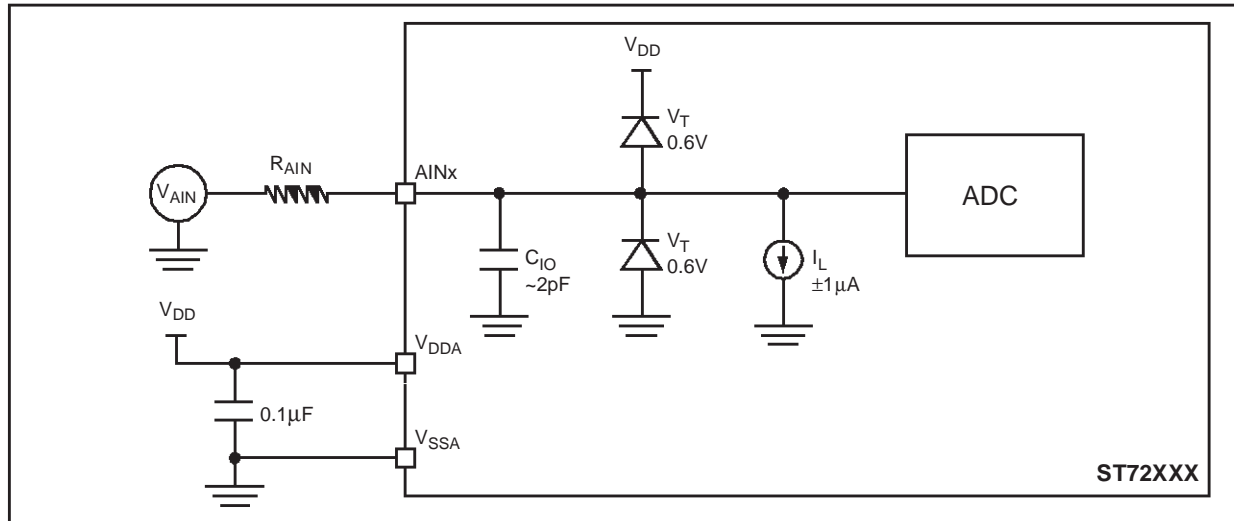
1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. Measurement points are done at CMOS levels: 0.3xV<sub>DD</sub> and 0.7xV<sub>DD</sub>.

13.12 8-BIT ADC CHARACTERISTICS

Subject to general operating conditions for  $V_{DD}$ ,  $f_{OSC}$ , and  $T_A$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>1)</sup>	Max	Unit
$f_{ADC}$	ADC clock frequency				4	MHz
$V_{AIN}$	Conversion range voltage <sup>2)</sup>		$V_{SSA}$		$V_{DDA}$	V
$R_{AIN}$	External input resistor				$10^3$ <sup>3)</sup>	k $\Omega$
$C_{ADC}$	Internal sample and hold capacitor			6		pF
$t_{STAB}$	Stabilization time after ADC enable			$0^4$		$\mu$ s
$t_{ADC}$	Conversion time (Sample+Hold)	$f_{CPU}=8\text{MHz}, f_{ADC}=4\text{MHz}$		3		
	- Sample capacitor loading time - Hold conversion time			4 8		$1/f_{ADC}$

Figure 94. Typical Application with ADC



Notes:

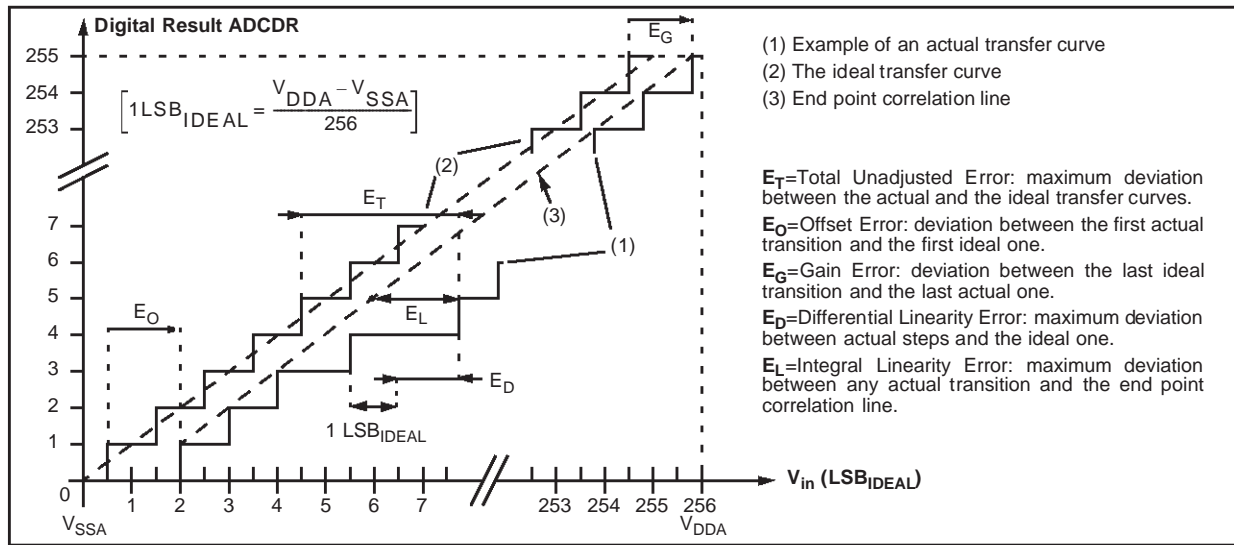
1. Unless otherwise specified, typical data are based on  $T_A=25^\circ\text{C}$  and  $V_{DD}-V_{SS}=5\text{V}$ . They are given only as design guidelines and are not tested.
2. When  $V_{DDA}$  and  $V_{SSA}$  pins are not available on the pinout, the ADC refer to  $V_{DD}$  and  $V_{SS}$ .
3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than  $10\text{k}\Omega$ ). Data based on characterization results, not tested in production.
4. The stabilization time of the AD converter is masked by the first  $t_{LOAD}$ . The first conversion after the enable is then always valid.

8-BIT ADC CHARACTERISTICS (Cont'd)

ADC Accuracy

Symbol	Parameter	Conditions	Min	Max	Unit
$ E_T $	Total unadjusted error <sup>1)</sup>	$V_{DD}=5.0V, ^3)$ $f_{CPU}=8MHz$		1	LSB
$E_O$	Offset error <sup>1)</sup>		-0.5	0.5	
$E_G$	Gain Error <sup>1)</sup>		-0.5	0.5	
$ E_D $	Differential linearity error <sup>1)</sup>			0.5	
$ E_L $	Integral linearity error <sup>1)</sup>			0.5	

Figure 95. ADC Accuracy Characteristics



Notes:

- ADC Accuracy vs. Negative Injection Current:  
 For  $I_{INJ} = 0.8mA$ , the typical leakage induced inside the die is  $1.6\mu A$  and the effect on the ADC accuracy is a loss of 1 LSB for each  $10K\Omega$  increase of the external analog source impedance. This effect on the ADC accuracy has been observed under worst-case conditions for injection:
  - negative injection
  - injection to an Input with analog capability, adjacent to the enabled Analog Input
  - at  $5V V_{DD}$  supply, and worst case temperature.
- Data based on characterization results over the whole temperature range, monitored in production.

### 14 PACKAGE CHARACTERISTICS

#### 14.1 PACKAGE MECHANICAL DATA

Figure 96. 32-Pin Shrink Plastic Dual In Line Package

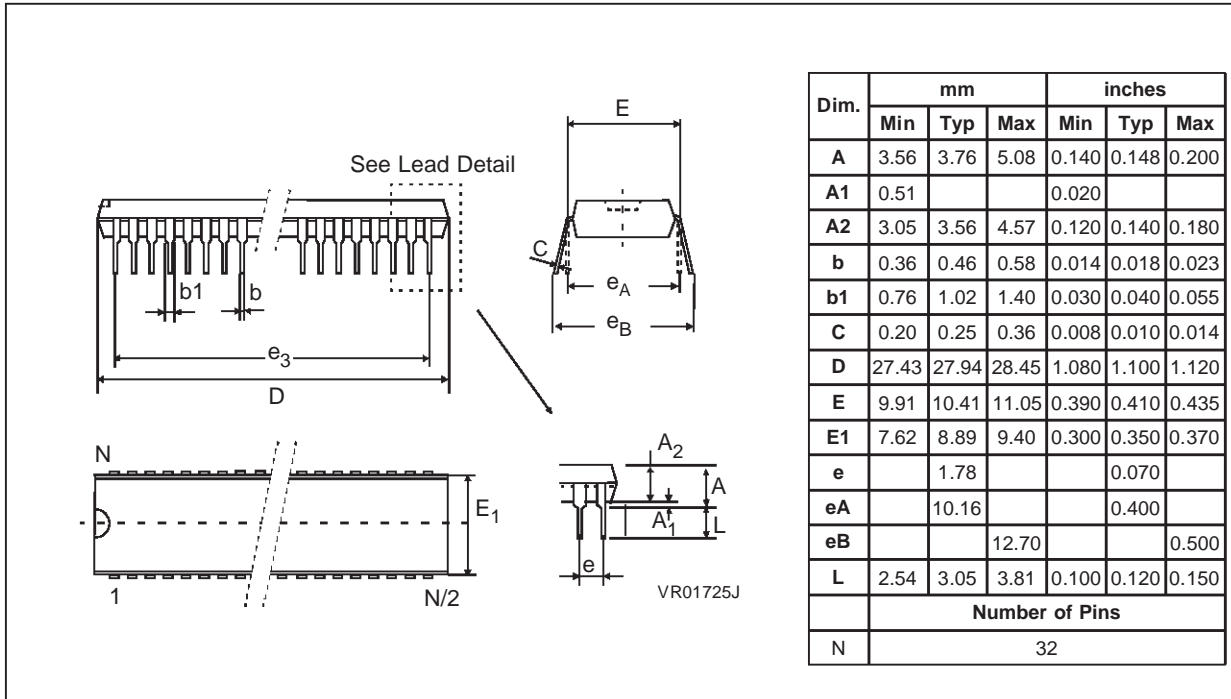
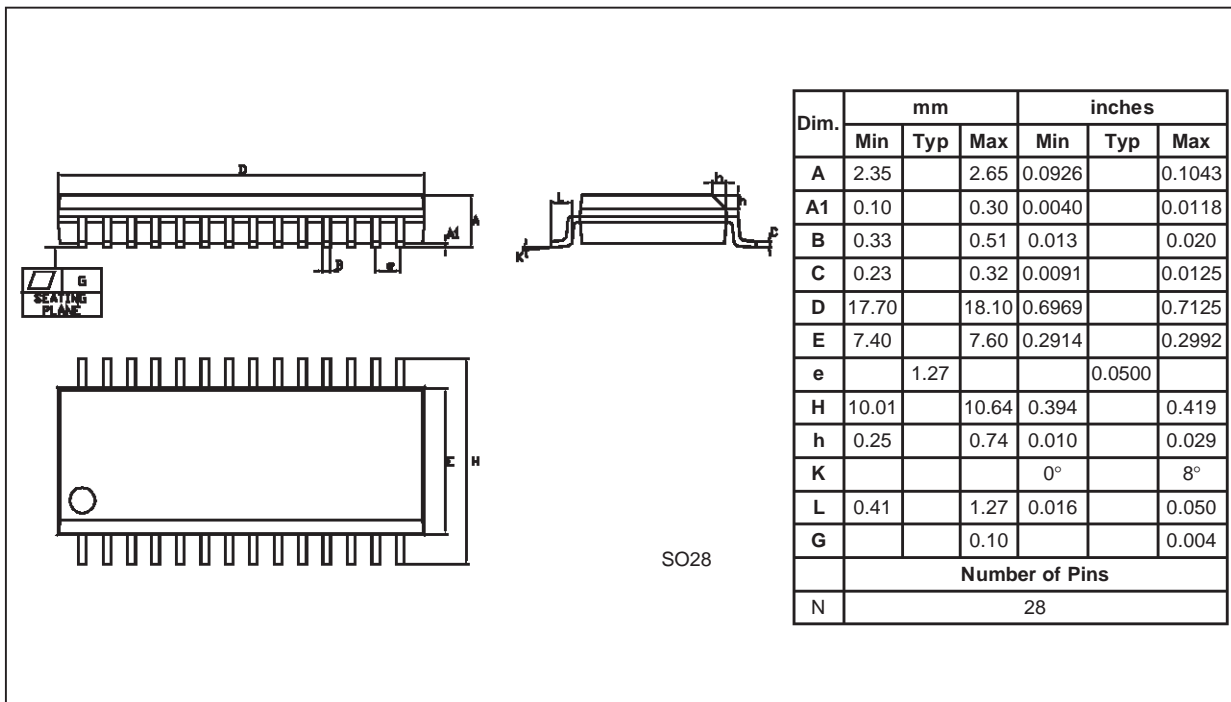


Figure 97. 28-Pin Plastic Small Outline Package, 300-mil Width



## 14.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
$R_{thJA}$	Package thermal resistance (junction to ambient)		
	SDIP32 SO28	60 75	°C/W
$P_D$	Power dissipation <sup>1)</sup>	500	mW
$T_{Jmax}$	Maximum junction temperature <sup>2)</sup>	150	°C

**Notes:**

1. The power dissipation is obtained from the formula  $P_D = P_{INT} + P_{PORT}$  where  $P_{INT}$  is the chip internal power ( $I_{DD} \times V_{DD}$ ) and  $P_{PORT}$  is the port power dissipation determined by the user.
2. The average chip-junction temperature can be obtained from the formula  $T_J = T_A + P_D \times R_{thJA}$ .

14.3 SOLDERING AND GLUEABILITY INFORMATION

Recommended soldering information given only as design guidelines in Figure 98 and Figure 99.

Recommended glue for SMD plastic packages dedicated to molding compound with silicone:

- Heraeus: PD945, PD955
- Loctite: 3615, 3298

Figure 98. Recommended Wave Soldering Profile (with 37% Sn and 63% Pb)

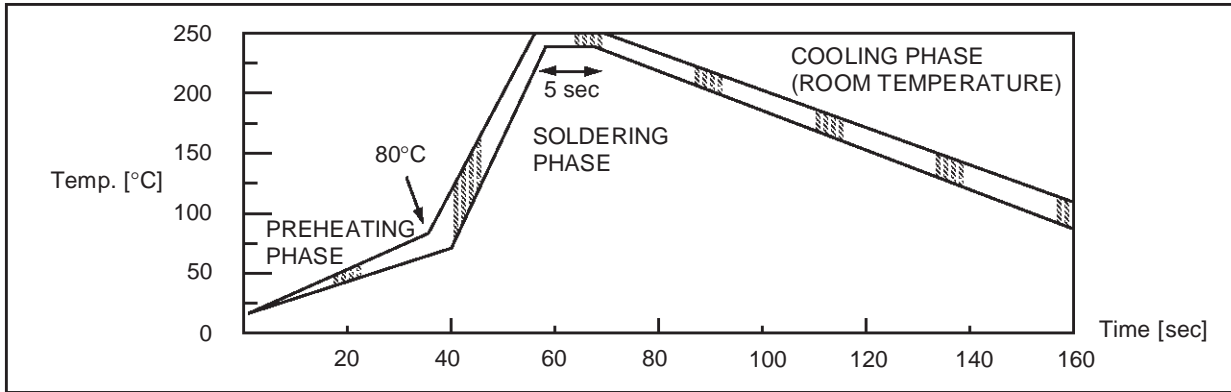
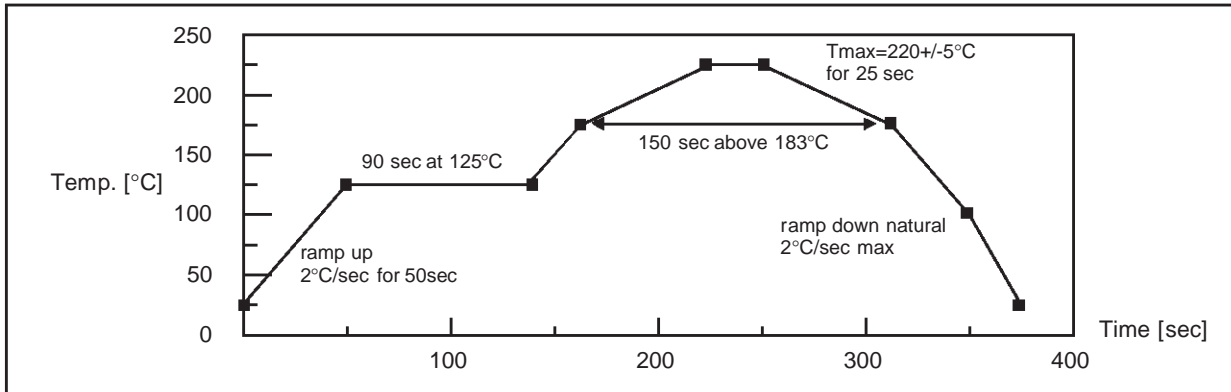


Figure 99. Recommended Reflow Soldering Oven Profile (MID JEDEC)



14.4 PACKAGE/SOCKET FOOTPRINT PROPOSAL

Table 21. Suggested List of SDIP32 Socket Types

Package / Probe	Adaptor / Socket Reference	Same Footprint	Socket Type
SDIP32 EMU PROBE	TEXTTOOL 232-1291-00	X	Textool

Table 22. Suggested List of SO28 Socket Types

Package / Probe	Adaptor / Socket Reference	Same Footprint	Socket Type
SO28	ENPLAS OTS-28-1.27-04		Open Top
	YAMAICHI IC51-0282-334-1		Clamshell
EMU PROBE	Adapter from SO28 to SDIP32 footprint (delivered with emulator)	X	SMD to SDIP



## 15 DEVICE CONFIGURATION AND ORDERING INFORMATION

Each device is available for production in user programmable versions (FLASH) as well as in factory coded versions (ROM). FLASH devices are shipped to customers with a default content (FFh), while ROM factory coded parts contain the code supplied by the customer. This implies that FLASH devices have to be configured by the customer using the Option Bytes while the ROM devices are factory-configured.

### 15.1 OPTION BYTES

The two option bytes allow the hardware configuration of the microcontroller to be selected.

The option bytes have no address in the memory map and can be accessed only in programming mode (for example using a standard ST7 programming tool). The default content of the FLASH is fixed to FFh.

In masked ROM devices, the option bytes are fixed in hardware by the ROM code (see option list).

#### USER OPTION BYTE 0

Bit 7:2 = **Reserved**, must always be 1.

Bit 1 = **EXTIT** *External Interrupt Configuration*.

This option bit allows the external interrupt mapping to be configured as shown in Table 23.

**Table 23. External Interrupt Configuration**

External IT0	External IT1	EXTIT
Ports PA7-PA0	Ports PB7-PB0 Ports PC5-PC0	1
Ports PA7-PA0 Ports PC5-PC0	Ports PB7-PB0	0

Bit 0 = **FMP** *Full memory protection*.

This option bit enables or disables external access to the internal program memory (read-out protection). Clearing this bit causes the erasing (to 00h) of the whole memory (including the option byte).

0: Program memory not read-out protected

1: Program memory read-out protected

#### USER OPTION BYTE 1

Bit 7 = **CFC** *Clock filter control on/off*

This option bit enables or disables the clock filter (CF) features.

0: Clock filter enabled

1: Clock filter disabled

Bit 6:4 = **OSC[2:0]** *Oscillator selection*

These three option bits can be used to select the main oscillator as shown in Table 24.

Bit 3:2 = **LVD[1:0]** *Low voltage detection selection*

These option bits enable the LVD block with a selected threshold as shown in Table 25.

Bit 1 = **WDG HALT** *Watchdog and halt mode*

This option bit determines if a RESET is generated when entering HALT mode while the Watchdog is active.

0: No Reset generation when entering Halt mode

1: Reset generation when entering Halt mode

Bit 0 = **WDG SW** *Hardware or software watchdog*

This option bit selects the watchdog type.

0: Hardware (watchdog always enabled)

1: Software (watchdog to be enabled by software)

**Table 24. Main Oscillator Configuration**

Selected Oscillator	OSC2	OSC1	OSC0
External Clock (Stand-by)	1	1	1
~4 MHz Internal RC	1	1	0
1~14 MHz External RC	1	0	X
Low Power Resonator (LP)	0	1	1
Medium Power Resonator (MP)	0	1	0
Medium Speed Resonator (MS)	0	0	1
High Speed Resonator (HS)	0	0	0

**Table 25. LVD Threshold Configuration**

Configuration	LVD1	LVD0
LVD Off	1	1
Highest Voltage Threshold (~4.50V)	1	0
Medium Voltage Threshold (~4.05V)	0	1
Lowest Voltage Threshold (~3.45V)	0	0

	USER OPTION BYTE 0								USER OPTION BYTE 1								
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
	Reserved							EXTIT	FMP	CFC	OSC 2	OSC 1	OSC 0	LVD1	LVD0	WDG HALT	WDG SW
Default Value	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1

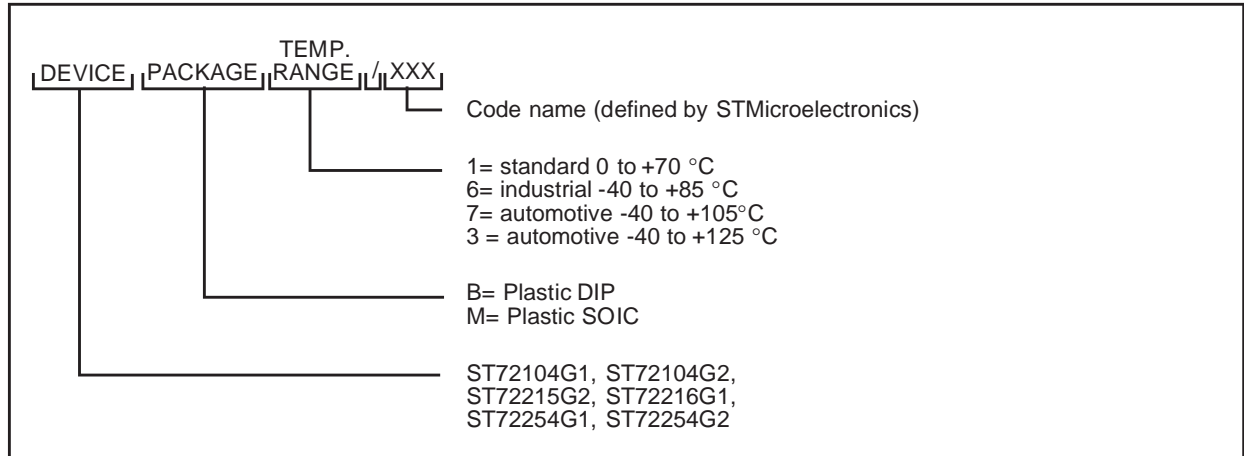
**15.2 DEVICE ORDERING INFORMATION AND TRANSFER OF CUSTOMER CODE**

Customer code is made up of the ROM contents and the list of the selected options (if any). The ROM contents are to be sent on diskette, or by electronic means, with the S19 hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

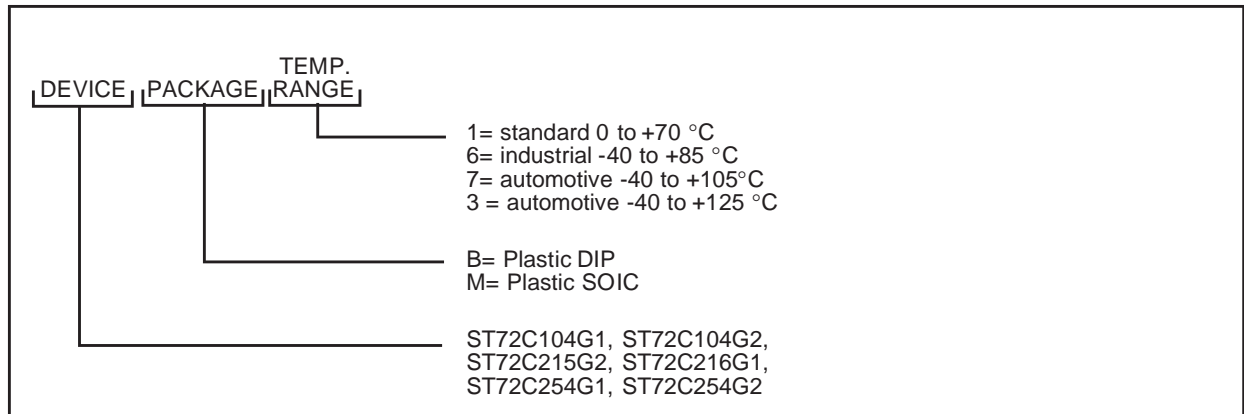
The selected options are communicated to STMicroelectronics using the correctly completed OPTION LIST appended.

The STMicroelectronics Sales Organization will be pleased to provide detailed information on contractual points.

**Figure 100. ROM Factory Coded Device Types**



**Figure 101. FLASH User Programmable Device Types**



TRANSFER OF CUSTOMER CODE (Cont'd)

MICROCONTROLLER OPTION LIST			
Customer	.....		
Address	.....		
	.....		
Contact	.....		
Phone No	.....		
Reference	.....		
STMicroelectronics references			
Device:	<input type="checkbox"/> ST72104G1	<input type="checkbox"/> ST72215G2	<input type="checkbox"/> ST72254G1
	<input type="checkbox"/> ST72104G2	<input type="checkbox"/> ST72216G1	<input type="checkbox"/> ST72254G2
Package:	<input type="checkbox"/> SDIP32	<input type="checkbox"/> SO28 with Standard conditioning (tube)	
		<input type="checkbox"/> SO28 with Tape & Reel conditioning	
External Interrupt:	<input type="checkbox"/> IT0 interrupt vector Port A, IT1 interrupt vector Port B & C		
	<input type="checkbox"/> IT0 interrupt vector Port A & C, IT1 interrupt vector Port B		
Temperature Range:	<input type="checkbox"/> 0°C to + 70°C	<input type="checkbox"/> - 40°C to + 105°C	
	<input type="checkbox"/> - 40°C to + 85°C	<input type="checkbox"/> - 40°C to + 125°C	
Clock Source Selection:	<input type="checkbox"/> Resonator:	<input type="checkbox"/> LP: Low power resonator (1 to 2 MHz)	
		<input type="checkbox"/> MP: Medium power resonator (2 to 4 MHz)	
		<input type="checkbox"/> MS: Medium speed resonator (4 to 8 MHz)	
		<input type="checkbox"/> HS: High speed resonator (8 to 16 MHz)	
	<input type="checkbox"/> RC Network:	<input type="checkbox"/> Internal	
		<input type="checkbox"/> External	
	<input type="checkbox"/> External Clock		
Clock Security System:	<input type="checkbox"/> Disabled	<input type="checkbox"/> Enabled	
Watchdog Selection:	<input type="checkbox"/> Software Activation	<input type="checkbox"/> Hardware Activation	
Halt when Watchdog on:	<input type="checkbox"/> Reset	<input type="checkbox"/> No reset	
Readout Protection:	<input type="checkbox"/> Disabled	<input type="checkbox"/> Enabled	
LVD Reset	<input type="checkbox"/> Disabled	<input type="checkbox"/> Enabled:	<input type="checkbox"/> Highest threshold (4.05V/4.30V)
			<input type="checkbox"/> Medium threshold (3.65V/3.90V)
			<input type="checkbox"/> Lowest threshold (3.10V/3.35V)
Comments :	.....		
Supply Operating Range in the application:	.....		
Notes	.....		
Signature	.....		
Date	.....		

**15.3 DEVELOPMENT TOOLS**

STMicroelectronics offers a range of hardware and software development tools for the ST7 micro-controller family. Full details of tools available for the ST7 from third party manufacturers can be obtained from the STMicroelectronics Internet site:

→ <http://mcu.st.com>.

**Third Party Tools**

- ACTUM
- BP
- COSMIC
- CMX
- DATA I/O
- HITEK
- HIWARE
- ISYSTEM
- KANDA
- LEAP

Tools from these manufacturers include C compilers, emulators and gang programmers.

**STMicroelectronics Tools**

Three types of development tool are offered by ST, all of them connect to a PC via a parallel (LPT) port: see Table 26 and Table 27 for more details.

**Table 26. STMicroelectronic Tool Features**

	In-Circuit Emulation	Programming Capability <sup>1)</sup>	Software Included
<b>ST7 Development Kit</b>	Yes. (Same features as HDS2 emulator but without logic analyzer)	Yes (DIP packages only)	ST7 CD ROM with: – ST7 Assembly toolchain – STVD7 and WGDB7 powerful Source Level Debugger for Win 3.1, Win 95 and NT – C compiler demo versions – ST Realizer for Win 3.1 and Win 95. – Windows Programming Tools for Win 3.1, Win 95 and NT
<b>ST7 HDS2 Emulator</b>	Yes, powerful emulation features including trace/ logic analyzer	No	
<b>ST7 Programming Board</b>	No	Yes (All packages)	

**Table 27. Dedicated STMicroelectronics Development Tools**

Supported Products	ST7 Development Kit	ST7 HDS2 Emulator	ST7 Programming Board
ST72254G1, ST72C254G1 ST72254G2, ST72C254G2 ST72215G2, ST72C215G2 ST72216G1, ST72C216G1 ST72104G1, ST72C104G1, ST72104G2, ST72C104G2	ST7MDT1-DVP2	ST7MDT1-EMU2B	ST7MDT1-EPB2/EU ST7MDT1-EPB2/US ST7MDT1-EPB2/UK

**Note:**

1. In-Situ Programming (ISP) interface for FLASH devices.

**15.4 ST7 APPLICATION NOTES**

Identification	Description
<b>PROGRAMMING AND TOOLS</b>	
AN985	Executing code in ST7 RAM
AN986	Using the ST7 indirect addressing mode
AN987	ST7 in-circuit programming
AN988	Starting with ST7 assembly tool chain
AN989	Starting with ST7 Hiware C
AN1039	ST7 math utility routines
AN1064	Writing optimized hiware C language for ST7
AN1179	Programming ST7 Flash Microcontrollers in Remote ISP Mode (In-Situ Programming)
<b>EXAMPLE DRIVERS</b>	
AN969	ST7 SCI communication between the ST7 and a PC
AN970	ST7 SPI communication between the ST7 and E PROM
AN971	ST7 I C communication between the ST7 and E PROM
AN972	ST7 software SPI master communication
AN973	SCI software communication with a PC using ST72251 16-bit timer
AN974	Real time clock with the ST7 timer output compare
AN976	Driving a buzzer using the ST7 PWM function
AN979	Driving an analog keyboard with the ST7 ADC
AN980	ST7 keypad decoding techniques, implementing wake-up on keystroke
AN1017	Using the ST7 USB microcontroller
AN1041	Using ST7 PWM signal to generate analog output (sinusoid)
AN1042	ST7 routine for I C slave mode management
AN1044	Multiple interrupt sources management for ST7 MCUs
AN1045	ST7 software implementation of I C bus master
AN1047	Managing reception errors with the ST7 SCI peripheral
AN1048	ST7 software LCD driver
AN1048	ST7 timer PWM duty cycle switch for true 0% or 100% duty cycle
<b>PRODUCT OPTIMIZATION</b>	
AN982	Using ceramic resonators with the ST7
AN1014	How to minimize the ST7 power consumption
AN1070	ST7 checksum selfchecking capability
<b>PRODUCT EVALUATION</b>	
AN910	ST7 and ST9 performance benchmarking
AN990	ST7 benefits versus industry standard
AN1181	Electrostatic discharge sensitivity measurement
<b>APPLICATION EXAMPLES</b>	
AN1086	ST7 / ST10U435 CAN-Do solutions for car multiplexing

**15.5 TO GET MORE INFORMATION**

To get the latest information on this product please use the ST web server. → <http://mcu.st.com/>



## **16 SUMMARY OF CHANGES**

Description of the changes between the current release of the specification and the previous one.

<b>Rev.</b>	<b>Main changes</b>	<b>Date</b>
2.2	Power saving mode corrected in Figure 18 on page 28 and Figure 20 on page 29.	Feb-00

**Notes:**

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