



STB24NF10

N - CHANNEL 100V - 0.07Ω - 24A TO-263 LOW GATE CHARGE STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB24NF10	100 V	< 0.077 Ω	24 A

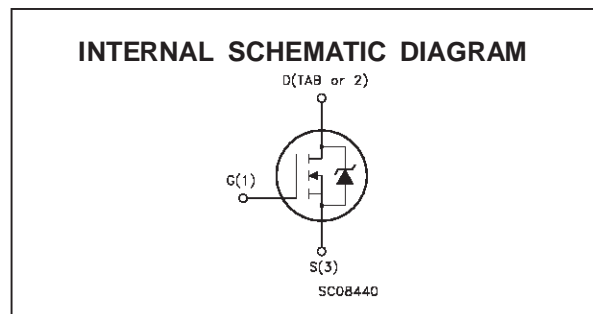
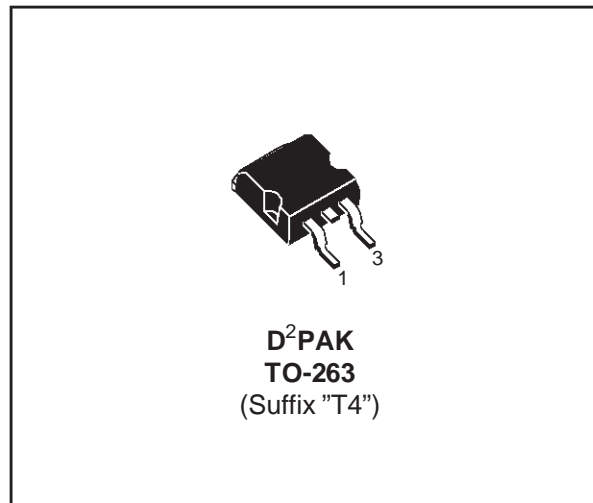
- TYPICAL R_{DS(on)} = 0.07 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	24	A
I _D	Drain Current (continuous) at T _c = 100 °C	15	A
I _{DM} (•)	Drain Current (pulsed)	96	A
P _{tot}	Total Dissipation at T _c = 25 °C	80	W
	Derating Factor	0.53	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	9	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	75	mJ
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(2) starting T_j = 25 °C, I_b = 24A, V_{DD} = 50V

(1) I_{SD} ≤ 24 A, di/dt ≤ 300A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMA}

STB24NF10

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.87	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 V$ $I_D = 12 A$		0.07	0.077	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	24			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 12 A$		20		S
C_{iss}	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		870		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			52		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 12\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		58		ns
t_r	Rise Time			45		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 24\text{ A}$ $V_{GS} = 10\text{ V}$		30		nC
Q_{gs}	Gate-Source Charge			6		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 27\text{ V}$ $I_D = 12\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		49		ns
t_f	Fall Time			17		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 80\text{ V}$ $I_D = 24\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Inductive Load, see fig. 5)		43		ns
t_f	Fall Time			36		ns
t_c	Cross-over Time			39		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				24	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				96	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 24\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 24\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		100		ns
Q_{rr}	Reverse Recovery Charge			375		nC
I_{RRM}	Reverse Recovery Current			7.5		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



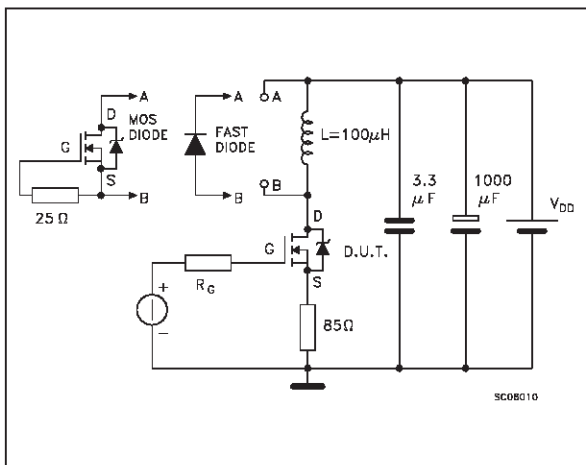
Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

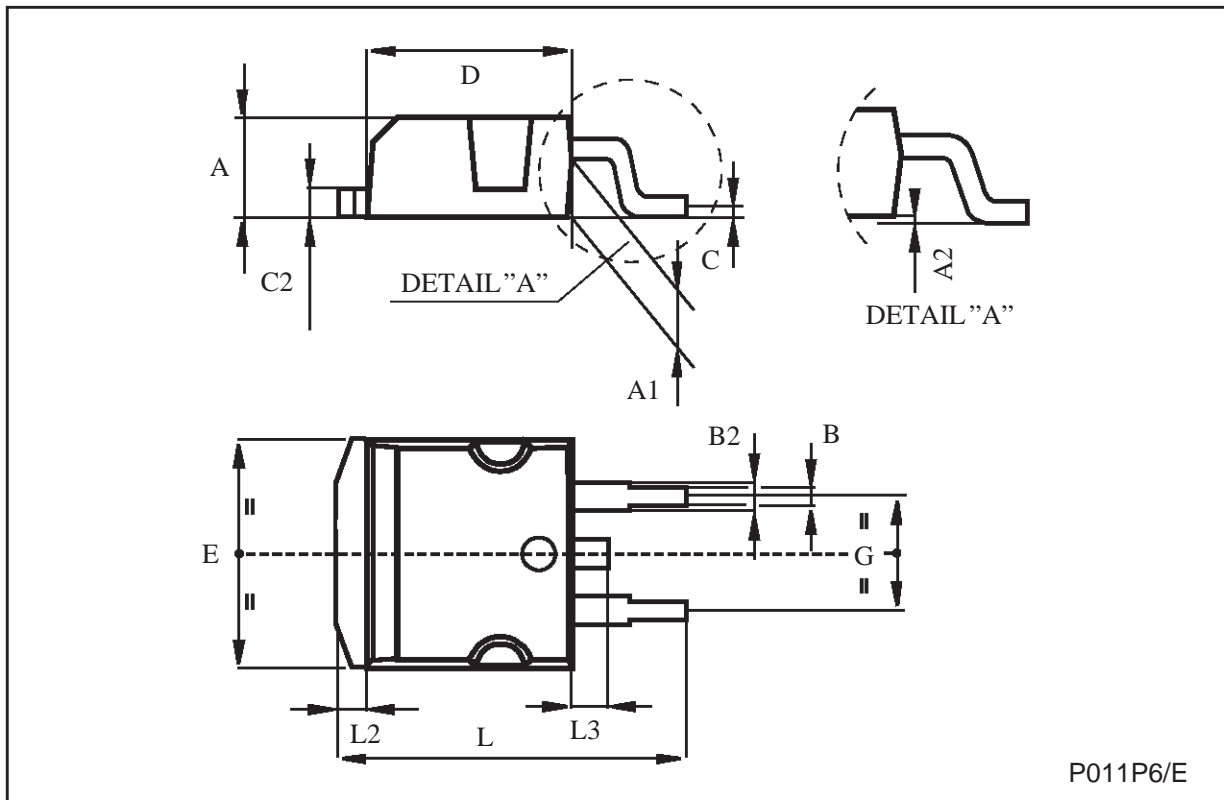


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



P011P6/E

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>