



LK115D00 SERIES

VERY LOW DROP WITH INHIBIT VOLTAGE REGULATORS

- VERY LOW DROPOUT VOLTAGE (0.2V TYP.)
- VERY LOW QUIESCENT CURRENT (TYP. 0.01 μ A IN OFF MODE, 280 μ A IN ON MODE)
- OUTPUT CURRENT UP TO 100 mA
- TWO LOGIC-CONTROLLED ELECTRONIC SHUTDOWNS
- OUTPUT VOLTAGES OF 2; 2.5; 3; 3.3; 4; 4.75; 4.85; 5; 5.5V
- INTERNAL CURRENT AND THERMAL LIMIT
- ONLY 2.2 μ F FOR STABILITY
- V_{OUT} TOLLERANCE $\pm 3\%$ AT 25 °C
- SUPPLY VOLTAGE REJECTION: 80 db (TYP.)
- TEMPERATURE RANGE: -40 TO 125 °C

DESCRIPTION

The LK115D00 series are very Low Drop regulators available in SO-8 package and in a wide range of output voltages.

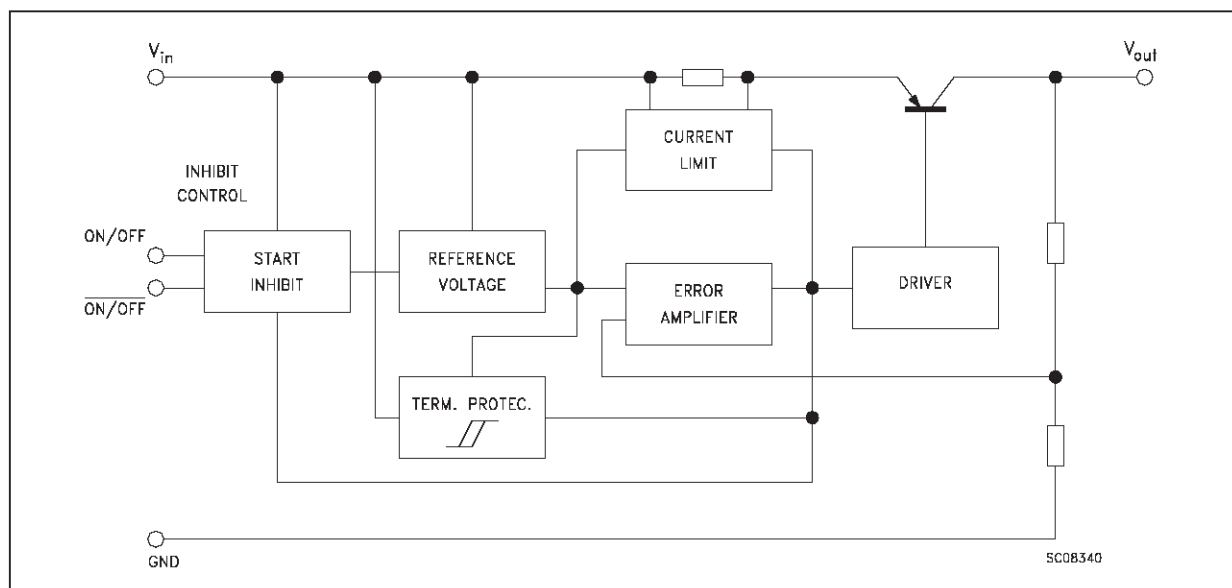
The very Low Drop voltage (0.2V) and the very low quiescent current (0.01 μ A in OFF MODE,



280 μ A in ON MODE) make them particularly suitable for Low Noise, Low Power applications and specially in battery powered systems.

Both active HIGH and active LOW shutdown Logic Control are available (pin2 and 3). This means that when the device is used as a local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. It requires only a 2.2 μ F capacitor for stability allowing space and cost saving.

BLOCK DIAGRAM

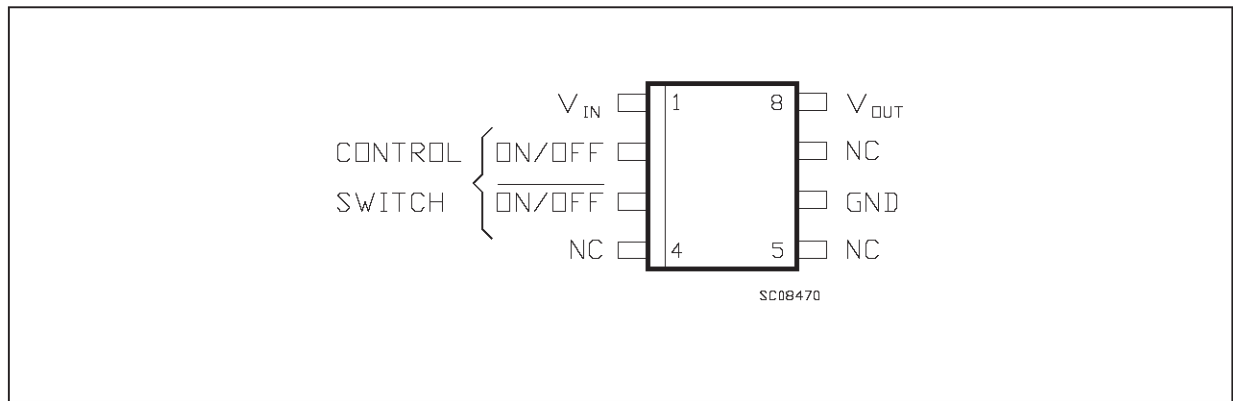


LK115D00 SERIES

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	20	V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{stg}	Storage Temperature Range	- 40 to 150	°C
T_{op}	Operating Junction Temperature Range	- 40 to 125	°C

CONNECTION DIAGRAM (top view)

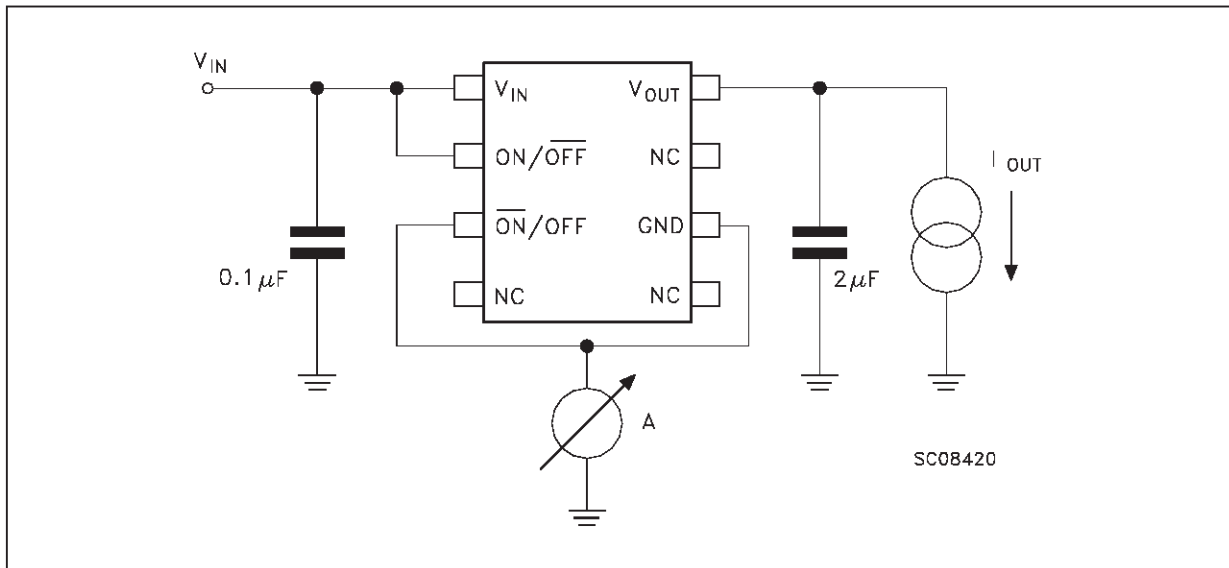


ORDERING NUMBERS

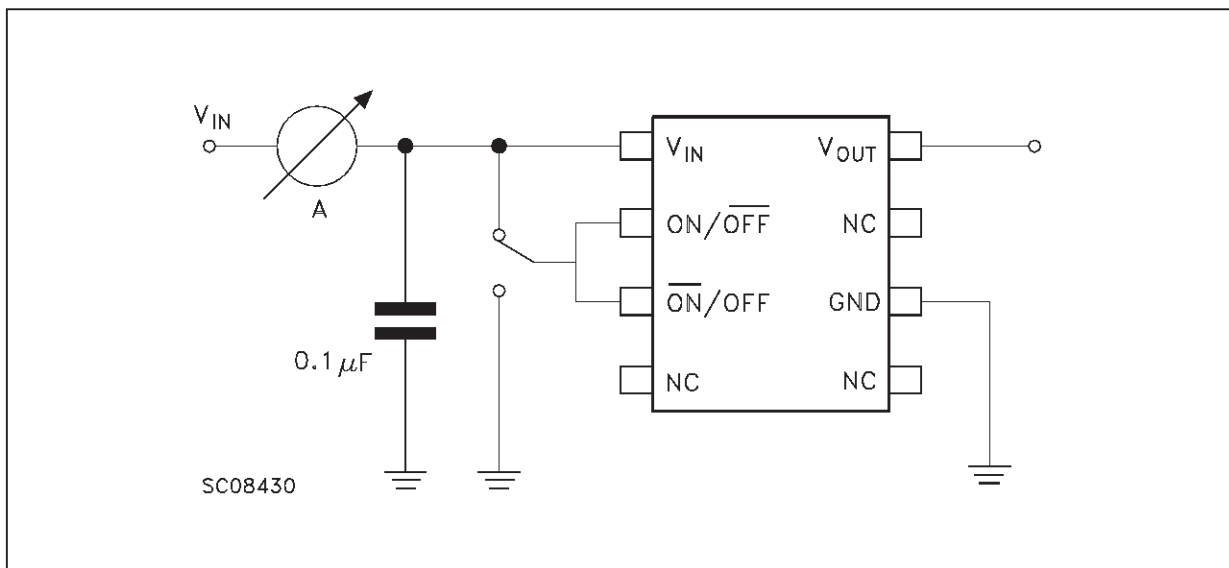
Type	Output Voltage
LK115D20	2 V
LK115D25	2.5 V
LK115D30	3 V
LK115D33	3.3 V
LK115D40	4 V
LK115D47	4.75 V
LK115D48	4.85 V
LK115D50	5 V
LK115D55	5.5 V

(*) Available on request

TEST CIRCUITS: Supply Current (ON MODE)



TEST CIRCUITS: Supply Current (OFF MODE)



NOTE: The switch emulates the two possibilities to set the regulator in OFF mode.

TRUTH TABLE

ON/OFF (PIN 2)	ON/OFF (PIN 3)	STATUS
H	L	ON
H	H	OFF
L	L	OFF
L	H	NOT ALLOWED

NOTES: Logic Levels are those defined in the electrical characteristics

LK115D00 SERIES

ELECTRICAL CHARACTERISTICS FOR LK115D20 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$,
 $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 4\text{ V}$	1.940	2	2.060	V
		$I_o = 10\text{ mA}$, $V_i = 4\text{ V}$, $-40 < T_a < 125\text{ }^\circ\text{C}$	1.9		2.1	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 3\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		2	10	mV
ΔV_o	Load Regulation	$V_i = 3\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 3\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 3\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 3\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 4\text{ V} \pm 1\text{ V}$				
		$f = 120\text{ Hz}$		83		dB
		$f = 1\text{ KHz}$		78		dB
		$f = 10\text{ KHz}$		59		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		44		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} -$		V_{in}	V
		Pin 2 to V_{in} ON	0.2		$V_{in} -$	V
			0		2.4	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

ELECTRICAL CHARACTERISTICS FOR LK115D25 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$,
 $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 4.5\text{ V}$	2.425	2.5	2.575	V
		$I_o = 10\text{ mA}$, $V_i = 4.5\text{ V}$, $-40 < T_a < 125\text{ }^\circ\text{C}$	2.375		2.625	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 3.5\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		2	10	mV
ΔV_o	Load Regulation	$V_i = 3.5\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 3.5\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 3.5\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 3.5\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 4.5\text{ V} \pm 1\text{ V}$				
		$f = 120\text{ Hz}$		81		dB
		$f = 1\text{ KHz}$		76		dB
		$f = 10\text{ KHz}$		58		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		55		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} -$		V_{in}	V
		Pin 2 to V_{in} ON	0.2		$V_{in} -$	V
			0		2.4	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

ELECTRICAL CHARACTERISTICS FOR LK115D30 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$, $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 5\text{ V}$	2.910	3	3.090	V
		$I_o = 10\text{ mA}$, $V_i = 5\text{ V}$, $-40 < T_a < 125^\circ\text{C}$	2.850		3.150	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 4\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		2	10	mV
ΔV_o	Load Regulation	$V_i = 4\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 4\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 4\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 4\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 5\text{ V} \pm 1\text{ V}$		79		dB
		$f = 120\text{ Hz}$		74		dB
		$f = 1\text{ KHz}$		57		dB
		$f = 10\text{ KHz}$				
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		66		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} - 0.2$		V_{in}	V
		Pin 2 to V_{in} ON	0		$V_{in} - 2.4$	V
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

ELECTRICAL CHARACTERISTICS FOR LK115D33 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$, $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 5.3\text{ V}$	3.2	3.3	3.4	V
		$I_o = 10\text{ mA}$, $V_i = 5.3\text{ V}$, $-40 < T_a < 125^\circ\text{C}$	3.135		3.465	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 4.3\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		2	10	mV
ΔV_o	Load Regulation	$V_i = 4.3\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 4.3\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 4.3\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 4.3\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 5.3\text{ V} \pm 1\text{ V}$		79		dB
		$f = 120\text{ Hz}$		74		dB
		$f = 1\text{ KHz}$		57		dB
		$f = 10\text{ KHz}$				
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		72.6		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} - 0.2$		V_{in}	V
		Pin 2 to V_{in} ON	0		$V_{in} - 2.4$	V
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

LK115D00 SERIES

ELECTRICAL CHARACTERISTICS FOR LK115D40 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$,
 $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 6\text{ V}$	3.880	4	4.120	V
		$I_o = 10\text{ mA}$, $V_i = 6\text{ V}$, $-40 < T_a < 125\text{ }^\circ\text{C}$	3.8		4.2	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 5\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		3	15	mV
ΔV_o	Load Regulation	$V_i = 5\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 5\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 5\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 5\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 5\text{ V} \pm 1\text{ V}$				
		$f = 120\text{ Hz}$		77		dB
		$f = 1\text{ KHz}$		72		dB
		$f = 10\text{ KHz}$		56		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		88		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} -$		V_{in}	V
		Pin 2 to V_{in} ON	0.2		$V_{in} -$	V
			0		2.4	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

ELECTRICAL CHARACTERISTICS FOR LK115D47 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$,
 $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 6.8\text{ V}$	4.607	4.75	4.892	V
		$I_o = 10\text{ mA}$, $V_i = 6.8\text{ V}$, $-40 < T_a < 125\text{ }^\circ\text{C}$	4.513		4.987	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 5.8\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		3	15	mV
ΔV_o	Load Regulation	$V_i = 5.8\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 5.8\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 5.8\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 5.8\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 6.8\text{ V} \pm 1\text{ V}$				
		$f = 120\text{ Hz}$		75		dB
		$f = 1\text{ KHz}$		70		dB
		$f = 10\text{ KHz}$		55		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		104.5		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} -$		V_{in}	V
		Pin 2 to V_{in} ON	0.2		$V_{in} -$	V
			0		2.4	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

ELECTRICAL CHARACTERISTICS FOR LK115D48 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$,
 $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 6.9\text{ V}$	4.705	4.85	4.966	V
		$I_o = 10\text{ mA}$, $V_i = 6.9\text{ V}$, $-40 < T_a < 125^\circ\text{C}$	4.607		5.093	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 5.9\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		3	15	mV
ΔV_o	Load Regulation	$V_i = 5.9\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 5.9\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 5.9\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 5.9\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 6.9\text{ V} \pm 1\text{ V}$				
		$f = 120\text{ Hz}$		75		dB
		$f = 1\text{ KHz}$		70		dB
		$f = 10\text{ KHz}$		55		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		106.7		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} -$		V_{in}	V
		Pin 2 to V_{in} ON	0.2		$V_{in} -$	V
			0		2.4	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

ELECTRICAL CHARACTERISTICS FOR LK115D50 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$,
 $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 7\text{ V}$	4.85	5	5.15	V
		$I_o = 10\text{ mA}$, $V_i = 7\text{ V}$, $-40 < T_a < 125^\circ\text{C}$	4.75		5.25	V
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V
I_{out}	Output Current Limit		120	200		mA
ΔV_o	Line Regulation	$V_i = 6\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		3	15	mV
ΔV_o	Load Regulation	$V_i = 6\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV
I_d	Quiescent Current	ON MODE				
		$V_i = 6\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA
		$V_i = 6\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA
	OFF MODE	$V_i = 6\text{ to }20\text{ V}$		0.01	2	μA
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 7\text{ V} \pm 1\text{ V}$				
		$f = 120\text{ Hz}$		75		dB
		$f = 1\text{ KHz}$		70		dB
		$f = 10\text{ KHz}$		55		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		110		μV
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V
		Pin 3 to GND ON	2.4		V_{in}	V
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} -$		V_{in}	V
		Pin 2 to V_{in} ON	0.2		$V_{in} -$	V
			0		2.4	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF

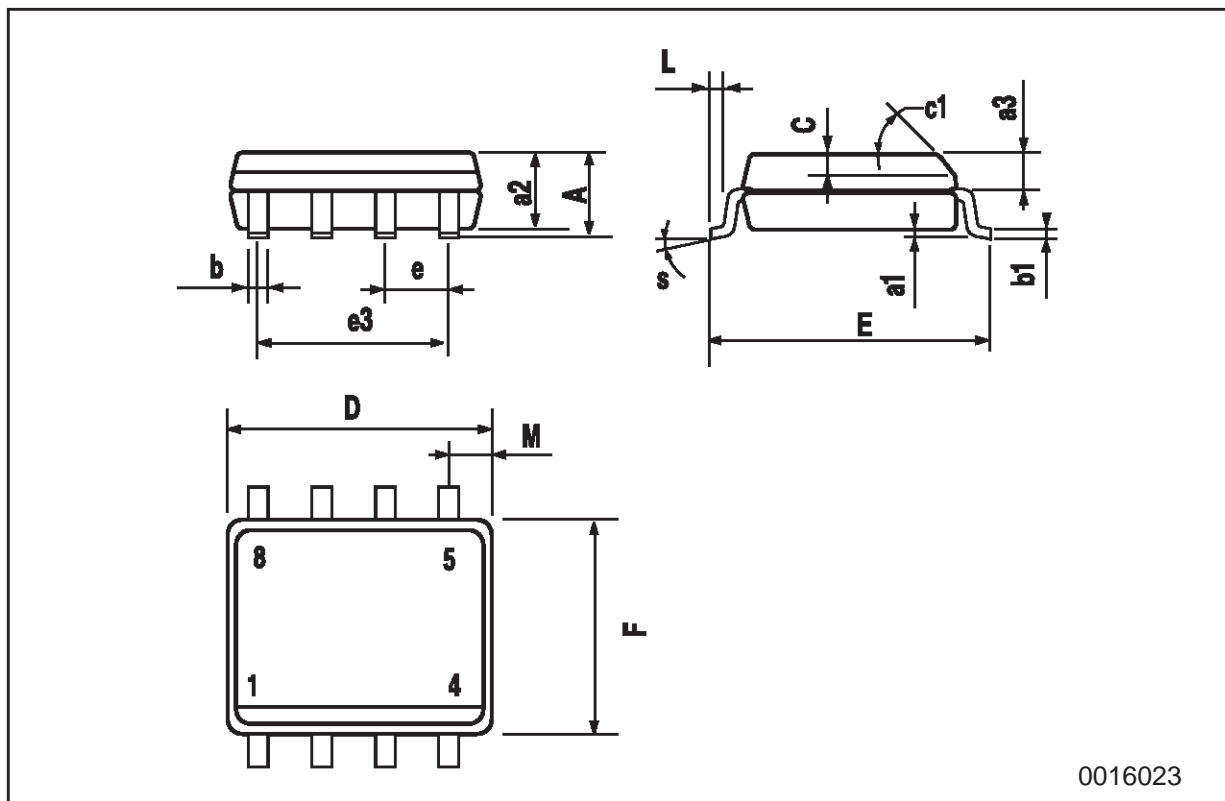
LK115D00 SERIES

ELECTRICAL CHARACTERISTICS FOR LK115D55 (refer to the test circuits, $T_j = 25\text{ }^\circ\text{C}$, $C_i = 0.1\text{ }\mu\text{F}$, $C_o = 2.2\text{ }\mu\text{F}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
V_o	Output Voltage	$I_o = 10\text{ mA}$, $V_i = 7.5\text{ V}$	5.335	5.5	5.665	V	
		$I_o = 10\text{ mA}$, $V_i = 7.5\text{ V}$, $-40 < T_a < 125\text{ }^\circ\text{C}$	5.225		5.775	V	
V_i	Operating Input Voltage	$I_o = 100\text{ mA}$			20	V	
I_{out}	Output Current Limit		120	200		mA	
ΔV_o	Line Regulation	$V_i = 6.5\text{ to }20\text{ V}$, $I_o = 0.5\text{ mA}$		3	15	mV	
ΔV_o	Load Regulation	$V_i = 6.5\text{ V}$, $I_o = 0.5\text{ to }100\text{ mA}$		4	20	mV	
I_d	Quiescent Current	ON MODE					
		$V_i = 6.5\text{ to }20\text{ V}$, $I_o = 0\text{ mA}$		0.28	0.5	mA	
		$V_i = 6.5\text{ to }20\text{ V}$, $I_o = 100\text{ mA}$		1.5	3	mA	
	OFF MODE	$V_i = 6.5\text{ to }20\text{ V}$		0.01	2	μA	
SVR	Supply Voltage Rejection	$I_o = 5\text{ mA}$, $V_i = 7.5\text{ V} \pm 1\text{ V}$ $f = 120\text{ Hz}$ $f = 1\text{ KHz}$ $f = 10\text{ KHz}$		74		dB	
					69		dB
					55		dB
eN	Output Noise Voltage	$B = 10\text{ Hz to }100\text{ KHz}$		121		μV	
V_d	Dropout Voltage	$I_o = 60\text{ mA}$		0.17		V	
V_{Hlc}	ON/OFF Control (pin 2)	Pin 3 to GND OFF	0		0.5	V	
		Pin 3 to GND ON	2.4		V_{in}	V	
V_{Llc}	ON/OFF Control (pin 3)	Pin 2 to V_{in} OFF	$V_{in} - 0.2$		V_{in}	V	
		Pin 2 to V_{in} ON	0		$V_{in} - 2.4$	V	
C_o	Output Bypass Capacitance	$\text{ESR} = 0.5\text{ to }10\text{ }\Omega$, $I_o = 0\text{ to }100\text{ mA}$	2	10		μF	

SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1998 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.