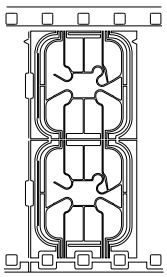
M14256
M14128

Memory Card IC
256/128 Kbit Serial I²C Bus EEPROM

PRELIMINARY DATA

- Compatible with I^2C Extended Addressing
- Two Wire I^2C Serial Interface
  Supports 400 kHz Protocol
- Single Supply Voltage (2.5 V to 5.5 V)
- Hardware Write Control
- BYTE and PAGE WRITE (up to 64 Bytes)
- BYTE, RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 100,000 Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)
- 5 ms Programming Time (typical)



Micromodule (D22)

DESCRIPTION

Each device is an electrically erasable programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance, Double Polysilicon, CMOS technology. This guarantees an endurance typically well above 100,000 Erase/Write cycles, with a data retention of 40 years. The memory operates with a power supply as low as 2.5 V.

The M14256 and M14128 are available in micromodule form only. For availability of the M14256 or

Figure 1. Logic Diagram

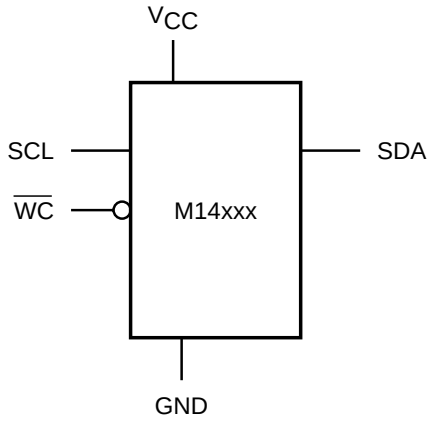
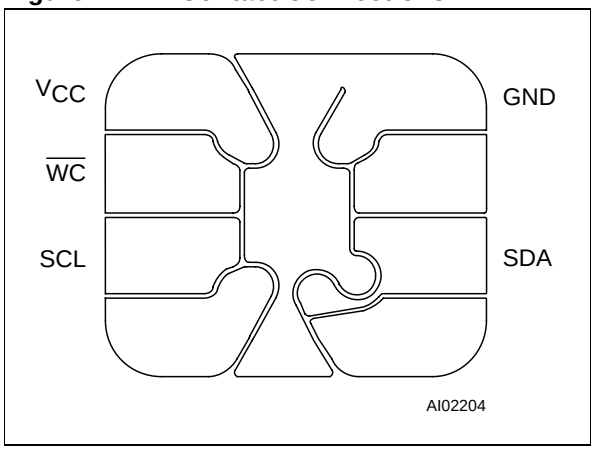


Table 1. Signal Names

SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
GND	Ground

Figure 2. D22 Contact Connections



M14128 in wafer form, please contact your ST sales office.

Each memory device is compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory device carries a built-in 7-bit unique Device Type Identifier code (1010000) in accordance with the I^2C bus definition. Only one memory device can be attached to each I^2C bus.

The memory device behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition, generated by the bus master. The START condition is followed by the Device Select Code which is composed of a stream of 7 bits (1010000), plus one read/write bit (R/$\overline{W}$) and is terminated by an acknowledge bit.

When writing data to the memory, the memory device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoACK for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to synchronize all data in and out of the memory. A pull up resistor can be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-40 to 120	°C
V_{IO}	Input or Output range	-0.6 to 6.5	V
V_{CC}	Supply Voltage	-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	4000	V
	Electrostatic Discharge Voltage (Machine model) [3]	400	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

Write Control ($\overline{WC}$)

The hardware Write Control contact ($\overline{WC}$) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} and write operations are allowed.

When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

DEVICE OPERATION

The memory device supports the XI^{2}C (Extended I^{2}C) protocol, as summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock, SCL, is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoACK, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 data bits.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends 8 bits to the SDA bus line (with the most significant bit first). These bits represent the Device Select Code (7 bits) and a $\overline{RW}$ bit.

The seven most significant bits of the Device Select Code are the Device Type Identifier, according to the I^{2}C bus definition. For the memory device, the seven bits are fixed at 1010000b (A0h), as shown in Table 5.

The 8th bit is the read or write bit ($\overline{RW}$). This bit is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the cor-

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^{2}C Bus

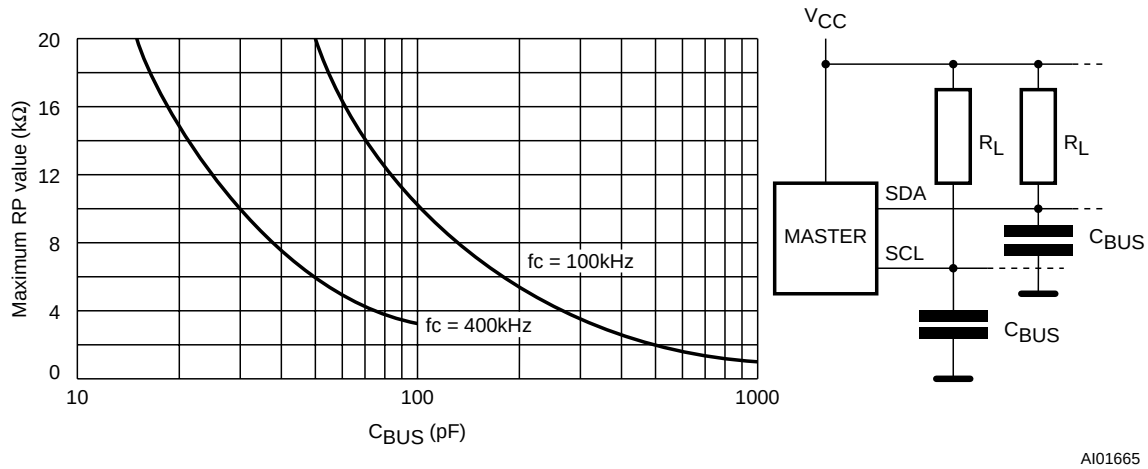
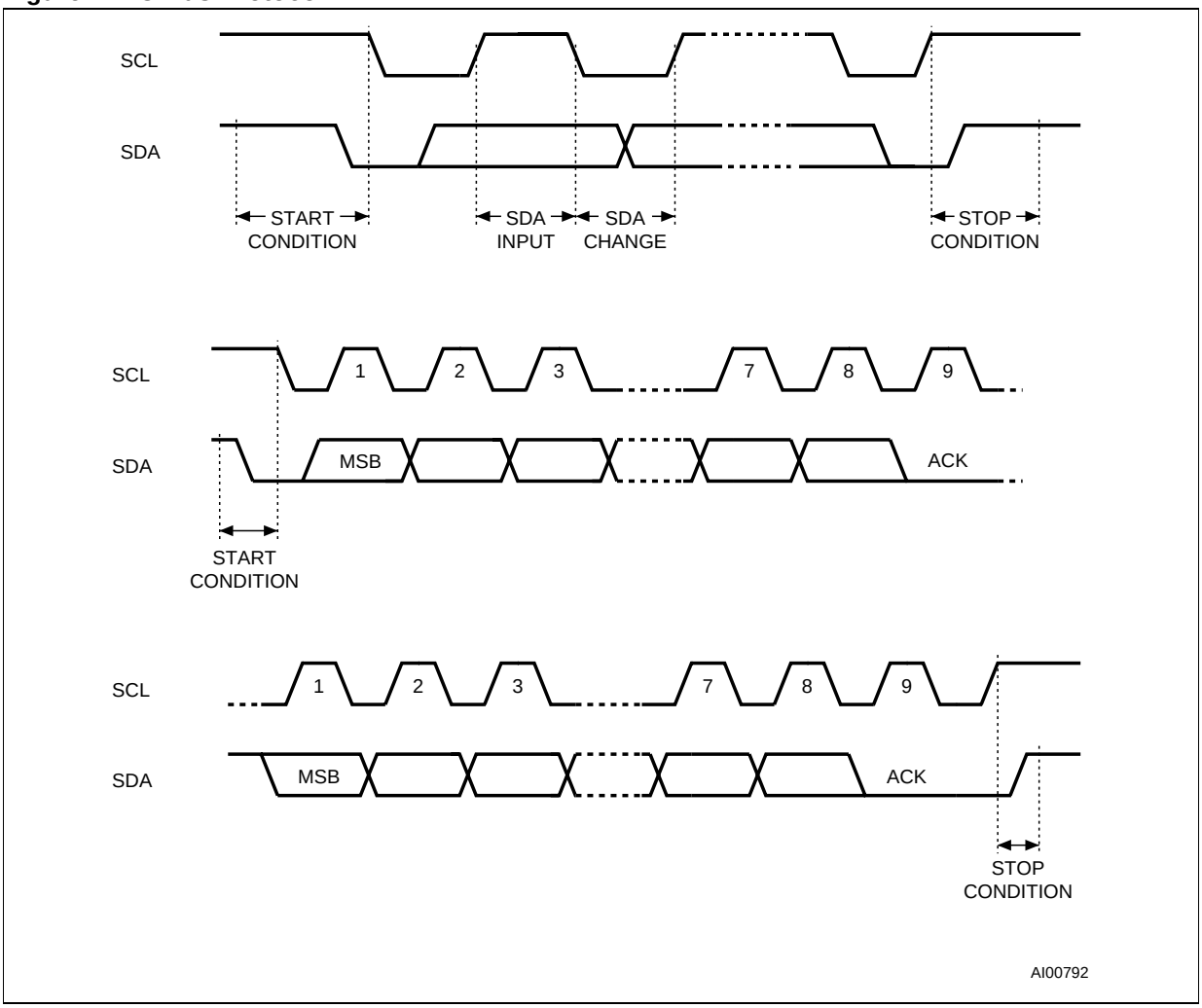


Figure 4. I²C Bus Protocol



responding memory gives an acknowledgment on the SDA bus during the 9th bit time. If the memory does not match the Device Select code, it will de-select itself from the bus, and go into stand-by mode.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 3) is sent first, followed by the Least significant Byte (Table 4). Bits b15 to b0 form the address of the byte in memory. Bit b15 is treated as a Don't Care bit on the M14256 memory. Bits b15 and b14 are treated as Don't Care bits on the M14128 memory.

Table 3. Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

Note: 1. b15 is Don't Care on the M14256 series.
b15 and b14 are Don't Care on the M14128 series.

Table 4. Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Table 5. Device Select Code [1]

	Device Code				Chip Enable			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	$R\overline{W}$

Note: 1. The most significant bit, b7, is sent first.

Write Operations

Following a START condition the master sends a Device Select code with the R$\overline{W}$ bit set to '0', as shown in Table 6. The memory acknowledges it and waits for two bytes of address, which provides access to the memory area. After receipt of each byte address, the memory again responds with an acknowledge and waits for the data byte. Writing in the memory may be inhibited if the input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the end of the two bytes address) will not modify the memory content and will NOT be acknowledged on data bytes, as shown in Figure 5.

Byte Write

In the Byte Write mode, after the Device Select code and the address, the master sends one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory replies with a NoACK, and the location is not modified. If, instead, the $\overline{WC}$ pin has been held at 0, as shown in Figure 6, the memory replies with an ACK. The master terminates the transfer by generating a STOP condition.

Page Write

The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b14-b6 for the M14256 and b13-b6 for the M14128) are the same. The master sends from one up to 64 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, each data byte is followed by a NoACK and the location is not modified. After each byte is transferred, the internal byte address counter (the six least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any

Figure 5. Write Mode Sequences with $\overline{WC}$=1

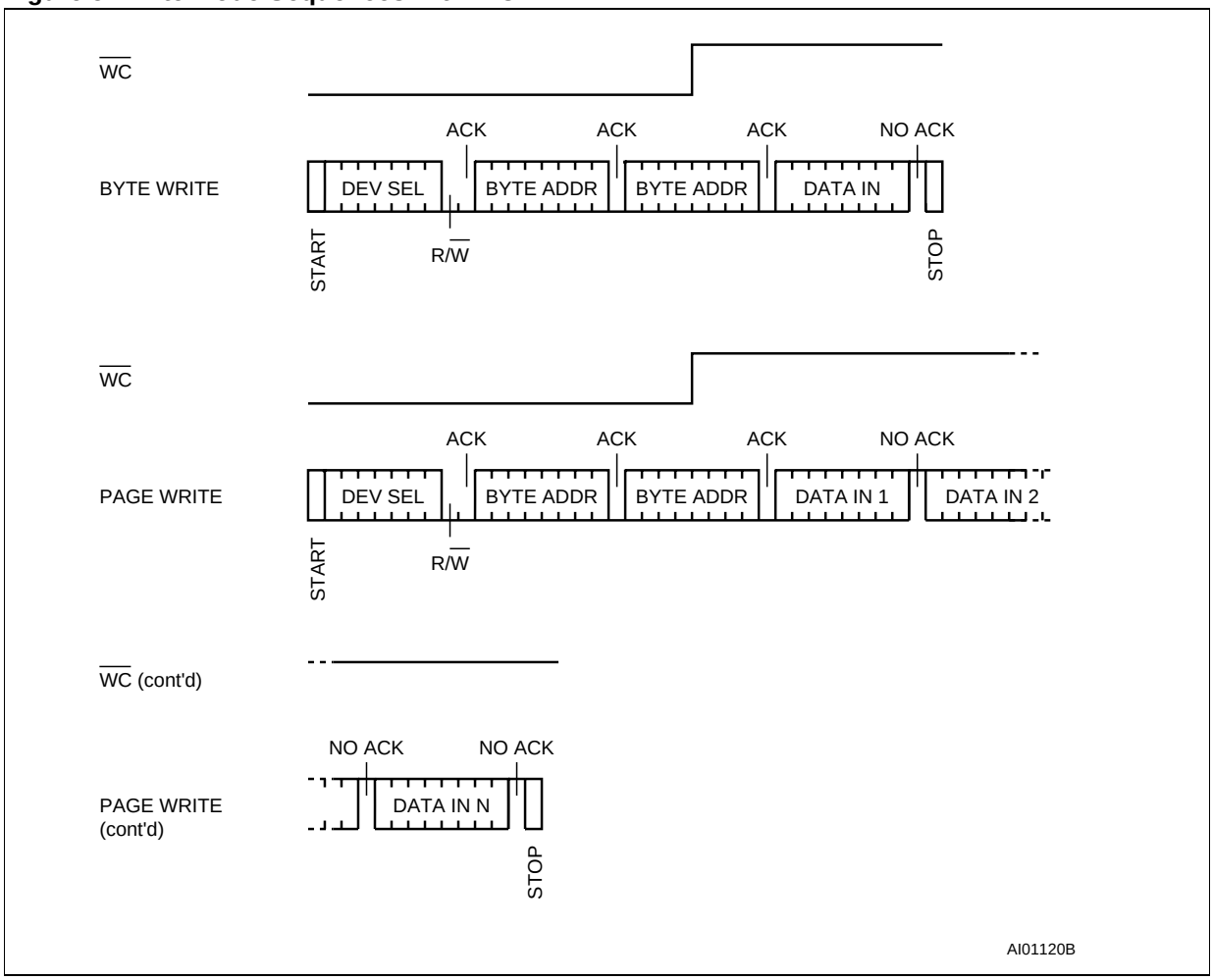
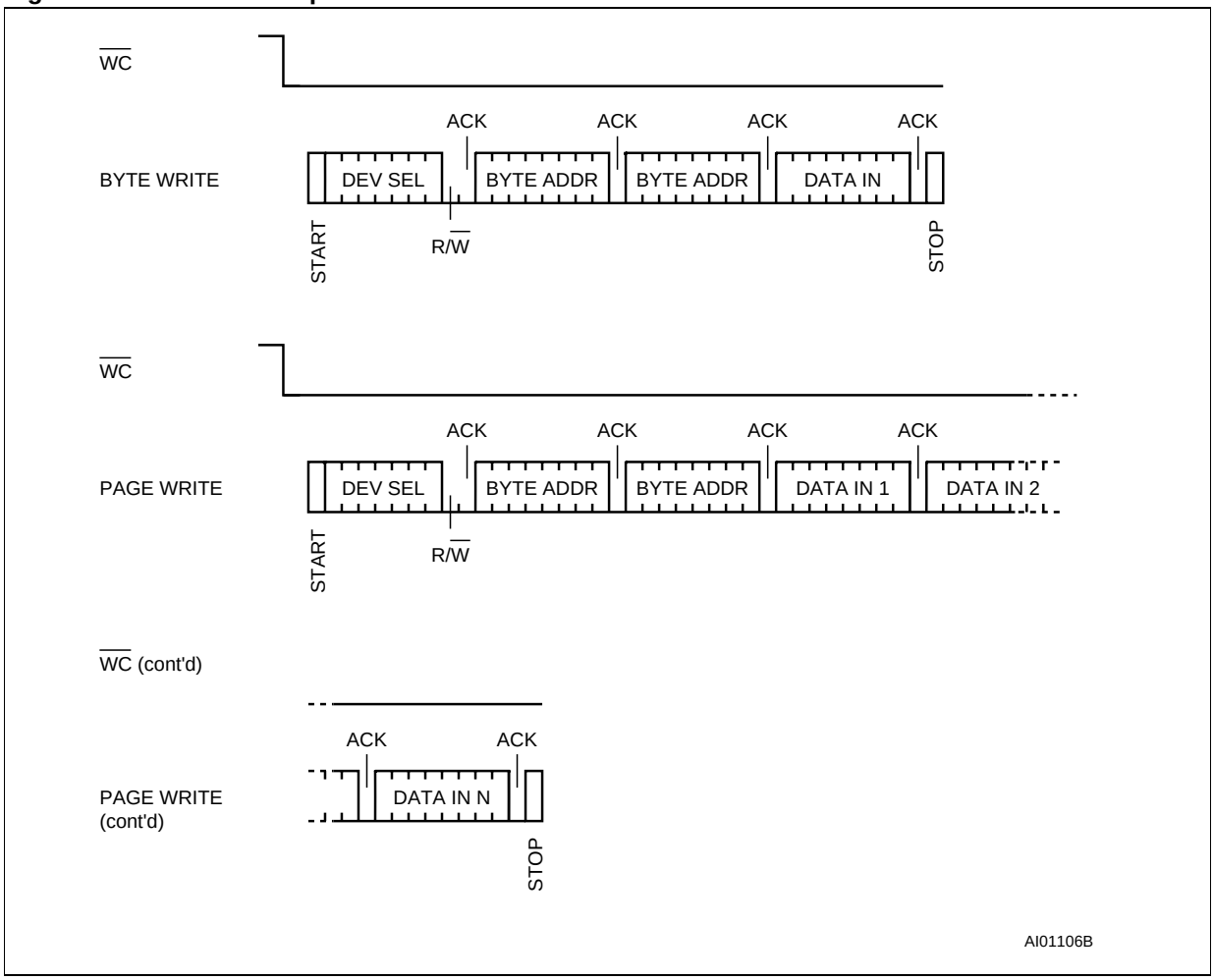


Table 6. Operating Modes

Mode	R$\overline{W}$ bit	$\overline{WC}$ [1]	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, R$\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	'1'	X	≥ 1	Similar to Current or Random Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, R$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	≤ 64	START, Device Select, R$\overline{W}$ = '0'

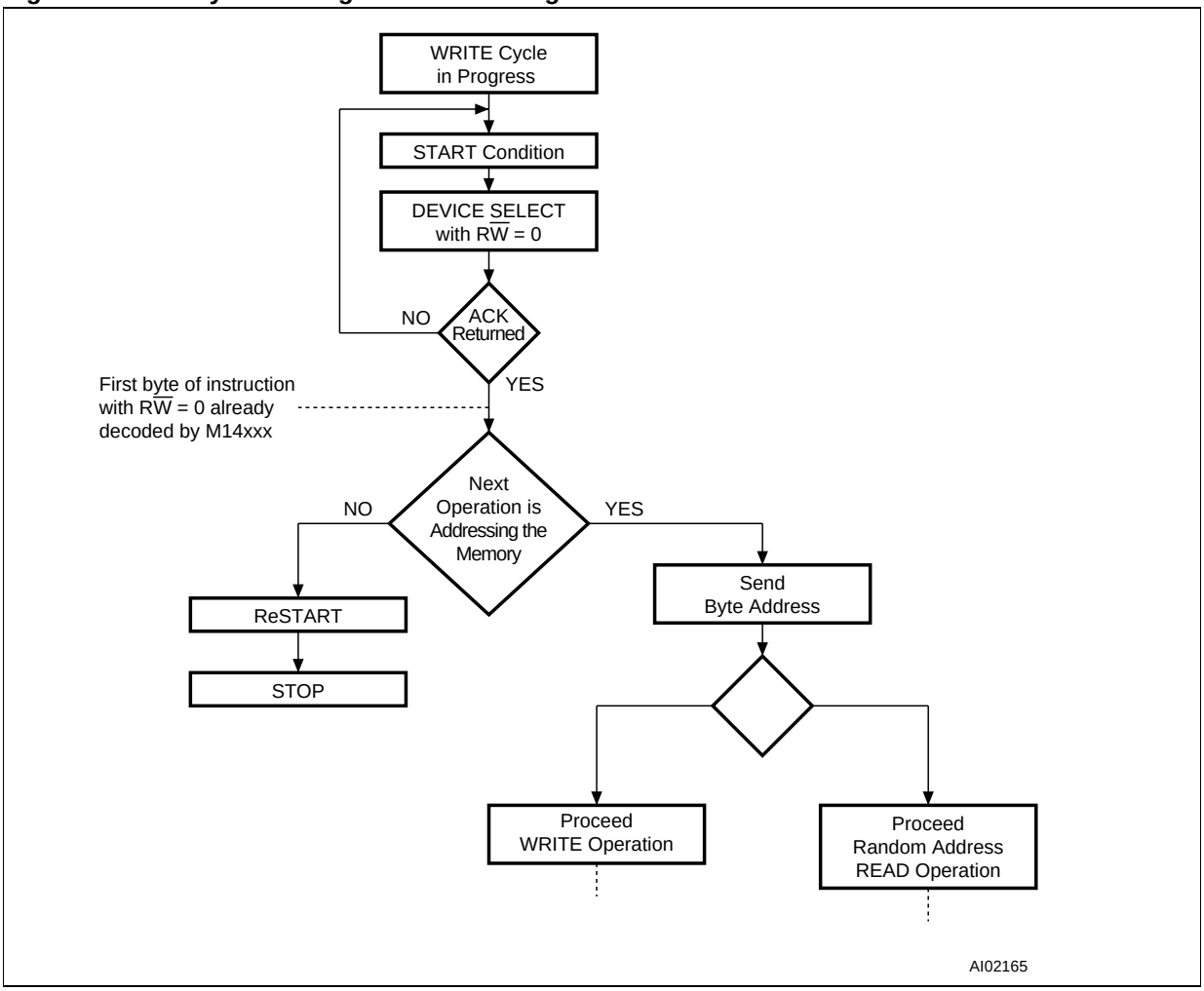
Note: 1. X = V_{IH} or V_{IL}.

Figure 6. Write Mode Sequences with $\overline{WC}$=0



byte or page write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition triggers an internal memory program cycle only if the STOP condition is internally decoded immediately after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the Memory will not respond to any request.

Figure 7. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is indicated in Table 7, but the typical time is shorter. To make use of this, an ACK polling sequence can be used by the master.

The sequence, as shown in Figure 7, is as follows:

– Initial condition: a Write is in progress.

– Step 1: the master issues a START condition followed by a device select byte (first byte of the new instruction).

– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are independent of the state of the $\overline{WC}$ pin. On delivery, the memory content is set at all “1’s” (FFh).

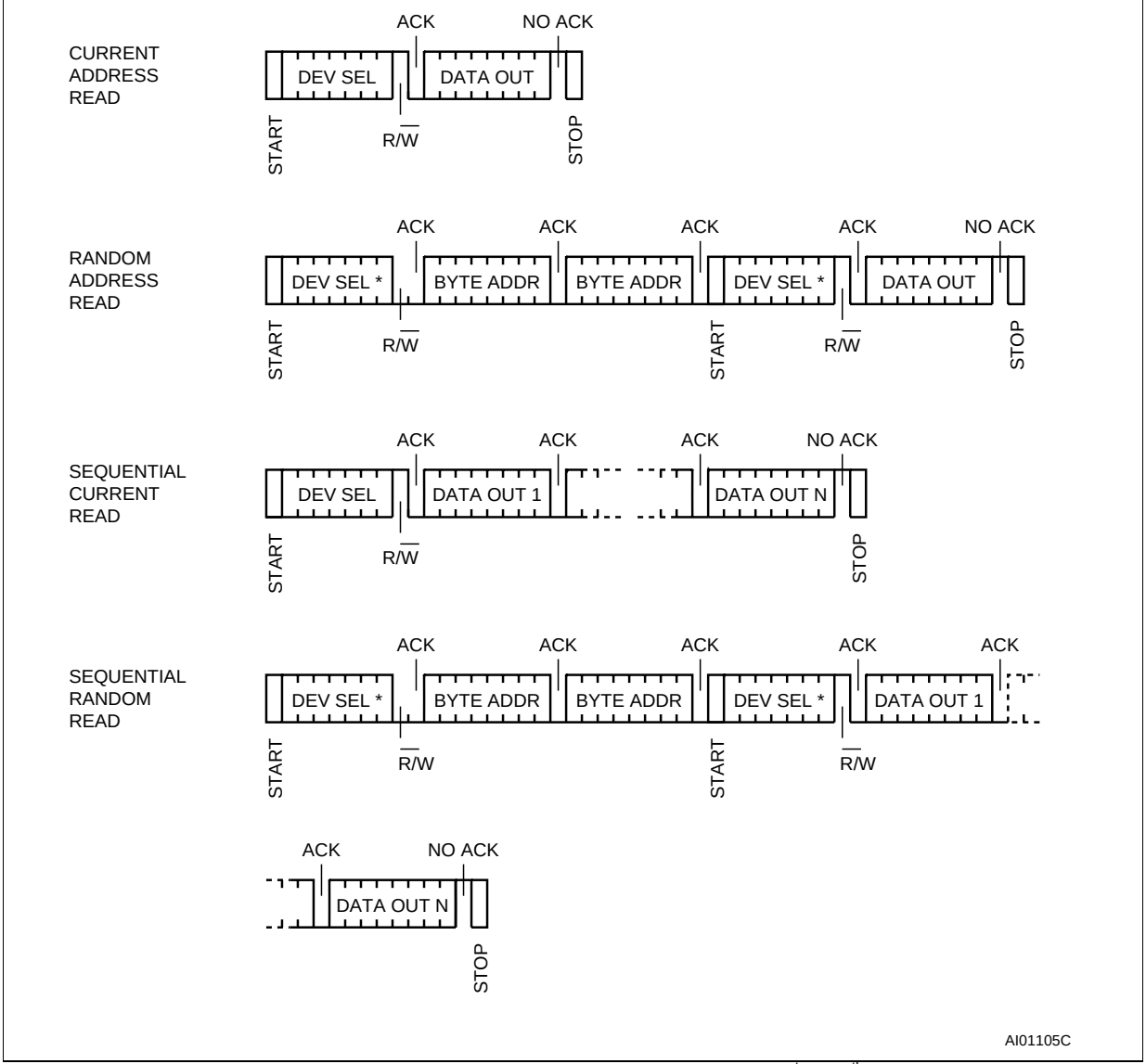
Current Address Read

The memory has an internal address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a device select with the $\overline{RW}$ bit set to ‘1’. The memory acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition, as shown in Figure 8.

Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 8. This is followed by another START condition from the master and the device select is repeated with

Figure 8. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select bytes of a Random Read (in the 1st and 4th bytes) must be identical.

the R$\overline{W}$ bit set to '1'. The memory acknowledges this, and outputs the byte addressed. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master *does* acknowledge the data byte output, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition. The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter will 'roll-over' and the memory will continue to output data from the start of the memory block.

Acknowledge in Read Mode

In all read modes the memory waits for an acknowledgment during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its standby state.

Table 7. AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 2.5 V to 5.5 V)

Symbol	Alt.	Parameter	Fast I^2C 400 kHz		I^2C 100 kHz		Unit
			Min	Max	Min	Max	
t_{CH1CH2} [2]	t_R	Clock Rise Time		300		1000	ns
t_{CL1CL2} [2]	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time	20	300	20	1000	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX} [1]	$t_{SU:STA}$	Clock High to Input Transition	600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		4000		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		4000		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid		1000		3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		100	kHz
t_W	t_{WR}	Write Time		10		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested

Table 8. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 2.5 V to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0 V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		20	µA
		$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage (SCL, SDA)		- 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		- 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} - 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Figure 9. AC Waveforms

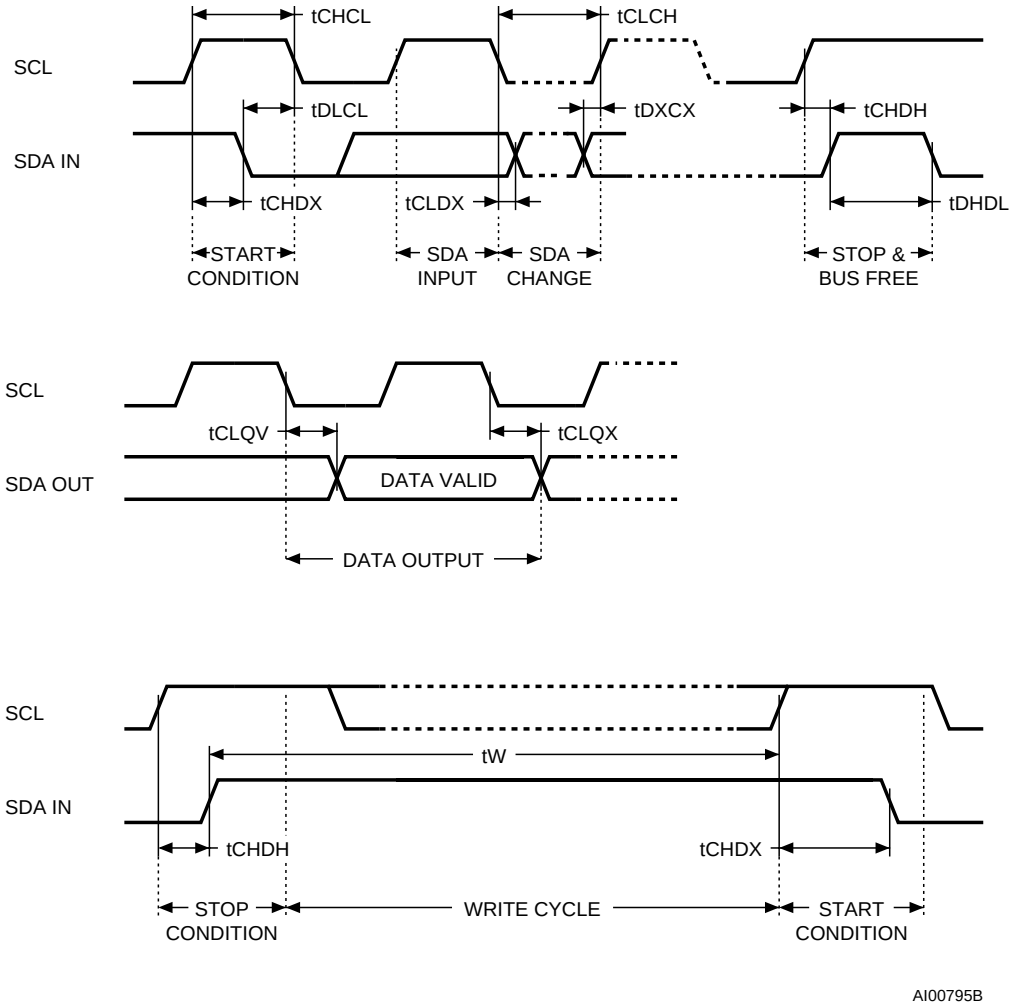


Table 9. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 10. AC Testing Input Output Waveforms

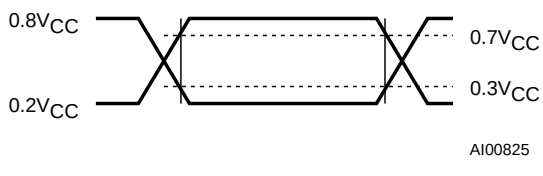


Table 10. Input Parameters[1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{NS}	Low Pass Filter Input Time Constant (SCL & SDA Inputs)		100	400	ns

Note: 1. Sampled only, not 100% tested.

Table 11. Ordering Information Scheme

Example: M14256 - W D22

Memory Capacity

256	256 Kbit
128	128 Kbit

Delivery Form

D22	Module on Super 35 mm film

Operating Voltage

W	2.5 V to 5.5 V

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all ‘1’s (FFh).

The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.