M28W160BT
M28W160BB

16 Mbit (1Mb x16, Boot Block) Low Voltage Flash Memory

- SUPPLY VOLTAGE
  - V_{DD} = 2.7V to 3.6V: for Program, Erase and Read
  - V_{DDQ} = 1.65V or 2.7V: Input/Output option
  - V_{PP} = 12V: optional Supply Voltage for fast Program
- ACCESS TIME
  - 2.7V to 3.6V: 90ns
  - 2.7V to 3.6V: 100ns
- PROGRAMMING TIME:
  - 10µs typical
  - Double Word Programming Option
- PROGRAM/ERASE CONTROLLER (P/E.C.)
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- MEMORY BLOCKS
  - Parameter Blocks (Top or Bottom location)
  - Main Blocks
- BLOCK PROTECTION on TWO PARAMETER BLOCKS
  - $\overline{WP}$ for Block Protection
- AUTOMATIC STAND-BY MODE
- PROGRAM and ERASE SUSPEND
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS of DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M28W160BT: 90h
  - Bottom Device Code, M28W160BB: 91h

TSOP48 (N)
12 x 20mm

µBGA46 (GB)
8 x 6 solder balls

Figure 1. Logic Diagram

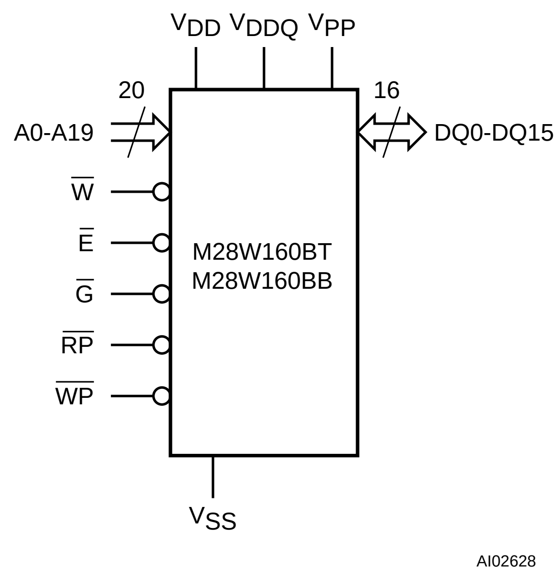


Figure 2. µBGA Connections (Top view through package)

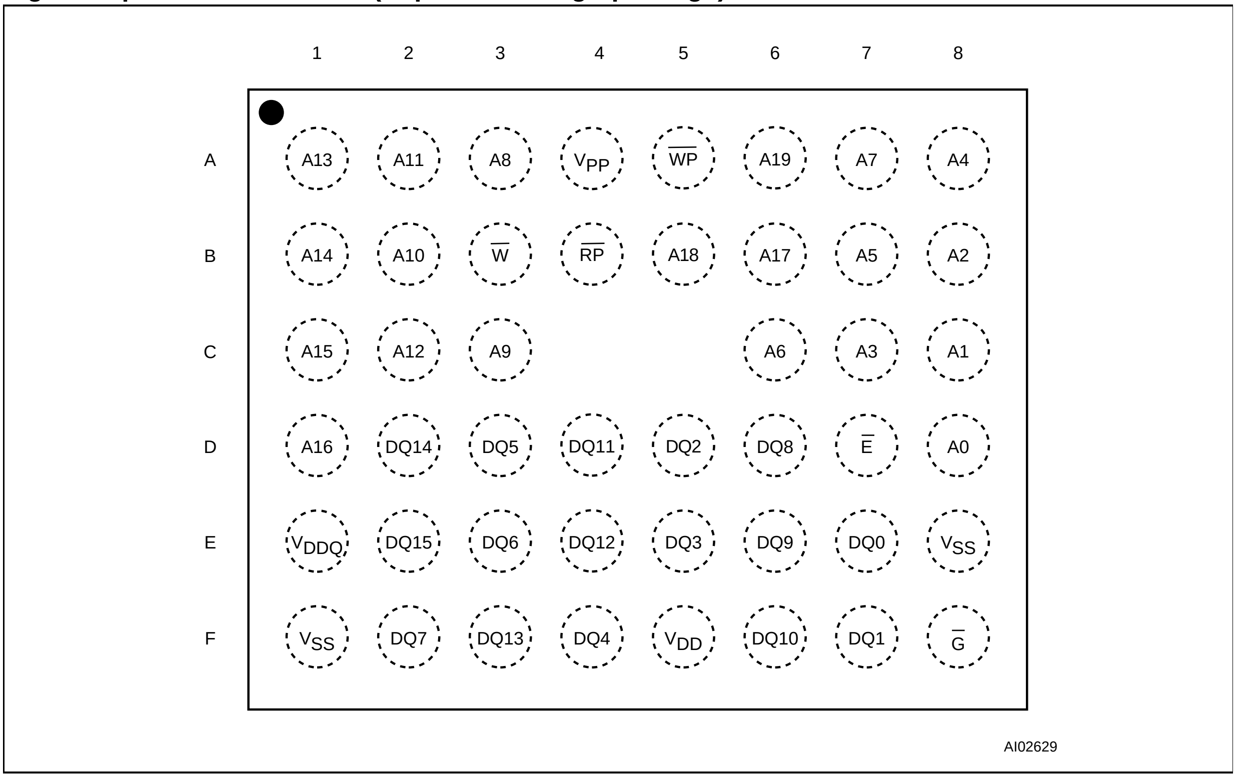


Figure 3. TSOP Connections

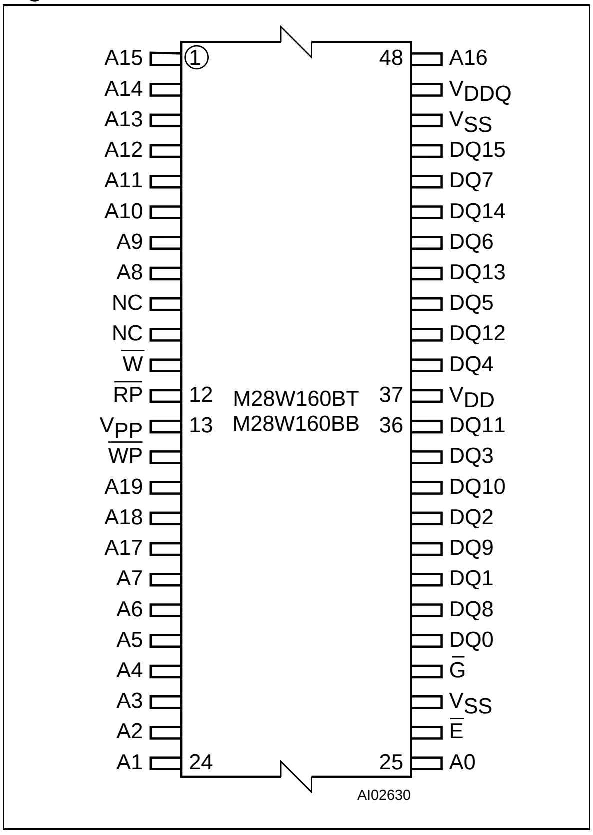


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Input/Output, Command Inputs
DQ8-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
$\overline{WP}$	Write Protect
V_{DD}	Supply Voltage
V_{DDQ}	Power Supply for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
NC	Not Connected Internally

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature [2]	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 155	°C
V_{IO}	Input or Output Voltage	–0.6 to V_{DDQ}+0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6 to 4.1	V
V_{PP}	Program Voltage	–0.6 to 13	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.

DESCRIPTION

The M28W160B is a 16 Mbit non-volatile Flash memory that can be erased electrically at the block level and programmed in-system on a Word-by-Word basis. The device is offered in the TSOP48 (10 x 20mm) and the µBGA46, 0.75mm ball pitch packages. When shipped, all bits of the M28W160B are in the ‘1’ state.

The array matrix organisation allows each block to be erased and reprogrammed without affecting other blocks. Each block can be programmed and erased over 100,000 cycles. V_{DDQ} allows to drive the I/O pin down to 1.65V. An optional 12V V_{PP} power supply is provided to speed up the program phase at customer production line environment. An internal Command Interface (C.I.) decodes the instructions to access/modify the memory content. The Program/Erase Controller (P/E.C.) automatically executes the algorithms taking care of the timings necessary for program and erase operations. Verification is performed too, unburdening the microcontroller, while the Status Register tracks the status of the operation.

The following instructions are executed by the M28W160B: Read Array, Read Electronic Signature, Read Status Register, Clear Status Register, Program, Double Word Program, Block Erase, Program/Erase Suspend, Program/Erase Resume and CFI Query.

Organisation

The M28W160B is organised as 1 Mbit by 16 bits. A0-A19 are the address lines; DQ0-DQ15 are the Data Input/Output. Memory control is provided by Chip Enable $\overline{E}$, Output Enable $\overline{G}$ and Write Enable $\overline{W}$ inputs. The Program and Erase operations are managed automatically by the P/E.C. Block protection against Program or Erase provides additional data security.

The upper two (or lower two) parameter blocks can be protected to secure the code content of the memory. $\overline{WP}$ controls protection and unprotection operations.

Memory Blocks

The device features an asymmetrical blocked architecture. The M28W160B has an array of 39 blocks: 8 Parameter Blocks of 4 KWord and 31 Main Blocks of 32 KWord. M28W160BT has the Parameter Blocks at the top of the memory address space while the M28W160BB locates the Parameter Blocks starting from the bottom. The memory maps are shown in Tables 3 and 4.

The two upper parameter block can be protected from accidental programming or erasure using $\overline{WP}$. Each block can be erased separately. Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed.

Table 3. Top Boot Block Addresses, M28W160BT

#	Size (KWord)	Address Range
38	4	FF000-FFFFF
37	4	FE000-FEFFF
36	4	FD000-FDFFF
35	4	FC000-FCFFF
34	4	FB000-FBFFF
33	4	FA000-FAFFF
32	4	F9000-F9FFF
31	4	F8000-F8FFF
30	32	F0000-F7FFF
29	32	E8000-EFFFF
28	32	E0000-E7FFF
27	32	D8000-DFFFF
26	32	D0000-D7FFF
25	32	C8000-CFFFF
24	32	C0000-C7FFF
23	32	B8000-BFFFF
22	32	B0000-B7FFF
21	32	A8000-AFFFF
20	32	A0000-A7FFF
19	32	98000-9FFFF
18	32	90000-97FFF
17	32	88000-8FFFF
16	32	80000-87FFF
15	32	78000-7FFFF
14	32	70000-77FFF
13	32	68000-6FFFF
12	32	60000-67FFF
11	32	58000-5FFFF
10	32	50000-57FFF
9	32	48000-4FFFF
8	32	40000-47FFF
7	32	38000-3FFFF
6	32	30000-37FFF
5	32	28000-2FFFF
4	32	20000-27FFF
3	32	18000-1FFFF
2	32	10000-17FFF
1	32	08000-0FFFF
0	32	00000-07FFF

Table 4. Bottom Boot Block Addresses, M28W160BB

#	Size (KWord)	Address Range
38	32	F8000-FFFFF
37	32	F0000-F7FFF
36	32	E8000-EFFFF
35	32	E0000-E7FFF
34	32	D8000-DFFFF
33	32	D0000-D7FFF
32	32	C8000-CFFFF
31	32	C0000-C7FFF
30	32	B8000-BFFFF
29	32	B0000-B7FFF
28	32	A8000-AFFFF
27	32	A0000-A7FFF
26	32	98000-9FFFF
25	32	90000-97FFF
24	32	88000-8FFFF
23	32	80000-87FFF
22	32	78000-7FFFF
21	32	70000-77FFF
20	32	68000-6FFFF
19	32	60000-67FFF
18	32	58000-5FFFF
17	32	50000-57FFF
16	32	48000-4FFFF
15	32	40000-47FFF
14	32	38000-3FFFF
13	32	30000-37FFF
12	32	28000-2FFFF
11	32	20000-27FFF
10	32	18000-1FFFF
9	32	10000-17FFF
8	32	08000-0FFFF
7	4	07000-07FFF
6	4	06000-06FFF
5	4	05000-05FFF
4	4	04000-04FFF
3	4	03000-03FFF
2	4	02000-02FFF
1	4	01000-01FFF
0	4	00000-00FFF

SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs (A0-A19). The address signals are inputs driven with CMOS voltage levels. They are latched during a write operation.

Data Input/Output (DQ0-DQ15). The data inputs, a word to be programmed or a command to the C.I., are latched on the Chip Enable $\overline{E}$ or Write Enable $\overline{W}$ rising edge, whichever occurs first. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected, the outputs are disabled or $\overline{RP}$ is tied to V_{IL}. Commands are issued on DQ0-DQ7.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ at V_{IH} deselects the memory and reduces the power consumption to the stand-by level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at V_{IL}.

Output Enable ($\overline{G}$). The Output Enable controls the data Input/Output buffers.

Write Enable ($\overline{W}$). This input controls writing to the Command Register, Input Address and Data latches.

Write Protect ($\overline{WP}$). Write Protect is an input to protect or unprotect the two lockable parameter blocks. When $\overline{WP}$ is at V_{IL}, the lockable blocks are protected. Program or erase operations are not achievable. When $\overline{WP}$ is at V_{IH}, the lockable blocks are unprotected and they can be programmed or erased (refer to Table 9).

Reset Input ($\overline{RP}$). The $\overline{RP}$ input provides hardware reset of the memory. When $\overline{RP}$ is at V_{IL}, the memory is in reset mode: the outputs are put to High-Z and the current consumption is minimised. When $\overline{RP}$ is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters read array mode.

V_{DD} Supply Voltage (2.7V to 3.6V). V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase). It ranges from 2.7V to 3.6V.

V_{DDQ} Supply Voltage (1.65V to V_{DD}). V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or it can use a separate supply. It can be powered either from 1.65V to 2.2V or from 2.7V to 3.6V.

V_{PP} Program Supply Voltage (12V). V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PP} is kept in a low voltage range (0V to 3.6V) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions. V_{PP} value is only sampled at the beginning of a program or erase; a change in its value after the operation has been started does not have any effect and program or erase are carried on regularly.

If V_{PP} is used in the range 11.4V to 12.6V acts as a power supply pin. In this condition V_{PP} value must be stable until P/E algorithm is completed (see Table 22 and 23).

V_{SS} Ground. V_{SS} is the reference for all the voltage measurements.

DEVICE OPERATIONS

Four control pins rule the hardware access to the Flash memory: $\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{RP}$. The following operations can be performed using the appropriate bus cycles: Read, Write the Command of an Instruction, Output Disable, Stand-by, Reset (see Table 5).

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the CFI. Both Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) must be at V_{IL} in order to perform the read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output independently of the device selection. The data read depend on the previous command written to the memory (see instructions RD, RSIG, RSR, RCFI). Read Array is the default state of the device when exiting Reset or after power-up.

Write. Write operations are used to give Commands to the memory or to latch Input Data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are at V_{IL} with Output Enable $\overline{G}$ at V_{IH}. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$, whichever occur first.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is at V_{IH}.

Stand-by. Stand-by disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable $\overline{E}$ is at V_{IH} and the device is in read mode. The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs. If $\overline{E}$ switches to V_{IH} during program or erase operation, the device enters in stand-by when finished.

Reset. During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high impedance. The memory is in Reset mode when $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the Stand-by level, independently from the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs. If $\overline{RP}$ is pulled to V_{SS} during a Program or Erase, this operation is aborted and the memory content is no longer valid as it has been compromised by the aborted operation.

Table 5. User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{WP}$	V_{PP}	DQ0-DQ15
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Don't Care	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{DD} or V_{PPH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Don't Care	Hi-Z
Stand-by	V_{IH}	X	X	V_{IH}	X	Don't Care	Hi-Z
Reset	X	X	X	V_{IL}	X	Don't Care	Hi-Z

Note: 1. X = V_{IL} or V_{IH}, V_{PPH} = 12V ± 5%.

Table 6. Read Electronic Signature (RSIG Instruction)

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1-A7	A8-A19	DQ0-DQ7	DQ8-DQ15
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Don't Care	20h	00h
Device Code	M28W160BT	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	90h	00h
	M28W160BB	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	91h	00h

Note: 1. $\overline{RP}$ = V_{IH}.

INSTRUCTIONS AND COMMANDS

Eleven instructions are available (see Tables 7 and 8) to perform Read Memory Array, Read Status Register, Read Electronic Signature, CFI Query, Erase, Program, Double Word Program, Clear Status Register, Program/Erase Suspend and Program/Erase Resume. Status Register output may be read at any time, during programming or erase, to monitor the progress of the operation.

An internal Command Interface (C.I.) decodes the instructions while an internal Program/Erase Controller (P/E.C.) handles all timing and verifies the correct execution of the Program and Erase instructions. P/E.C. provides a Status Register whose bits indicate operation and exit status of the internal algorithms.

The Command Interface is reset to Read Array when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequence must be followed exactly. Any invalid combination of commands will reset the device to Read Array.

Read (RD)

The Read instruction consists of one write cycle (refer to Device Operations section) giving the command FFh. Next read operations will read the addressed location and output the data. When a device reset occurs, the memory is in Read Array as default.

Read Status Register (RSR)

The Status Register indicates when a program or erase operation is complete and the success or failure of operation itself. Issue a Read Status Register Instruction (70h) to read the Status Register content.

The Read Status Register instruction may be issued at any time, also when a Program/Erase operation is ongoing. The following Read operations output the content of the Status Register. The Status Register is latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to V_{IH}. Either $\overline{E}$ or $\overline{G}$ must be toggled to update the latched data. Additionally, any read attempt during program or erase operation will automatically output the content of the Status Register.

Read Electronic Signature (RSIG)

The Read Electronic Signature instruction consists of one write cycle (refer to Device Operations section) giving the command 90h. A subsequent read will output the Manufacturer or the Device Code (Electronic Signature) depending on the levels of A0 (see Tables 6). The Electronic Signature can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of M28W160B. The Manufacturer Code is output when the address lines A0 is at V_{IL}, the Device Code is output when A0 is at V_{IH}. Address A1-A7 must be kept to V_{IL}, other addresses are ignored. The codes are output on DQ0-DQ7 with DQ8-DQ15 at 00h.

CFI Query (RCFI)

The Common Flash Interface Query mode is entered by writing 98h. Next read operations will read the CFI data. The CFI data structure contains also a security area; in this section, a 64 bit unique security number is written, starting at address 80h. This area can be accessed only in read mode by the final use and there are no ways of changing the code after it has been written by ST. Write a read instruction to return to Read mode (refer to the Common Flash Interface section).

Table 7. Commands

Hex Code	Command
00h, 01h, 60h, 2Fh, C0h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
30h	Double Word Program Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h or 98h	Read Electronic Signature, or CFI Query
B0h	Program/Erase Suspend
D0h	Program/Erase Resume, or Erase Confirm
FFh	Read Array

Table 8. Instructions

Mne-monic	Instruction	Cycles	1st Cycle			2nd Cycle			3nd Cycle		
			Operat.	Addr. (1)	Data	Operat.	Addr.	Data	Operat.	Addr.	Data
RD	Read Memory Array	1+	Write	X	FFh	Read (2)	Read Address	Data			
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register			
RSIG	Read Electronic Signature	1+	Write	X	90h or 98h	Read (2)	Signature Address (3)	Signature			
RCFI	CFI Query	1+	Write	55h	98h or 90h	Read (2)	CFI Address	Query			
EE	Erase	2	Write	X	20h	Write	Block Address	D0h			
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input			
DPG (4)	Double Word Program	3	Write	X	30h	Write	Address 1	Data Input	Write	Address 2	Data Input
CLRS	Clear Status Register	1	Write	X	50h						
PES	Program/ Erase Suspend	1	Write	X	B0h						
PER	Program/ Erase Resume	1	Write	X	D0h						

Note: 1. X = Don't Care.
2. The first cycle of the RD, RSR, RSIG or RCFI instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Address A7-A1 must be kept to V_{IL}. Other address bits are ignored.
4. Address 1 and Address 2 must be consecutive Addresses differing only for address bit A0.

Erase (EE)

Block erasure sets all the bits within the selected block to '1'. One block at a time can be erased. It is not necessary to program the block with 00h as the P/E.C. will do it automatically before erasing. This instruction uses two write cycles. The first command written is the Erase Set up command 20h. The second command is the Erase Confirm command D0h. An address within the block to be erased is given and latched into the memory during the input of the second command. If the second command given is not an erase confirm, the status register bits b4 and b5 are set and the instruction aborts.

Read operations output the status register after erasure has started.

Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure. Status register bit b1 returns '1' if the user is attempting to program a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}.

Erase aborts if $\overline{RP}$ turns to V_{IL}. As data integrity cannot be guaranteed when the erase operation is aborted, the erase must be repeated. A Clear Status Register instruction must be issued to reset b1, b3, b4 and b5 of the Status Register. During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and PES (Program/Erase Suspend) instructions.

Table 9. Memory Blocks Protection Truth Table

V_{PP} (1,3)	$\overline{RP}$ (2,4)	$\overline{WP}$ (1,4)	Lockable Blocks	Other Blocks
X	V_{IL}	X	Protected	Protected
V_{IL}	V_{IH}	X	Protected	Protected
V_{DD} or V_{PPH} (5)	V_{IH}	V_{IL}	Protected	Unprotected
V_{DD} or V_{PPH} (5)	V_{IH}	V_{IH}	Unprotected	Unprotected

Note: 1. Notes:1.X' = Don't Care
2. $\overline{RP}$ is the Reset/Power Down.
3. V_{PP} is the program or erase supply voltage.
4. V_{IH}/V_{IL} are logic high and low levels.
5. V_{PP} must be also greater than the Program Voltage Lock-Out V_{PPLK}.

Table 10. Status Register Bits

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a word.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Invalid, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPLK} when a Program or Erase instruction is executed. V_{PP} is sampled only at the beginning of the Erase/Program operation.
			'0'	V_{PP} OK	
PSS	2	Program Suspend Status	'1'	Suspended	On a Program Suspend instruction P/ECS and PSS bits are set to '1'. PSS remains '1' until a Program Resume Instruction is given
			'0'	In Progress or Completed	
BPS	1	Block Protection Status	'1'	Program/Erase on protected Block, Abort	BPS bit is set to '1' if a Program or Erase operation has been attempted on a protected block
			'0'	No operation to protected blocks	
	0	Reserved			

Note: Logic level '1' is High, '0' is Low.

Program (PG)

The memory array can be programmed word-by-word. This instruction uses two write cycles. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C.

Read operations output the Status Register content after the programming has started. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status register bit b1 returns '1' if the user is attempting to program a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}. Programming aborts if $\overline{RP}$ goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be erased and reprogrammed. A Clear Status Register instruction must be issued to reset b4, b3 and b1 of the Status Register.

During the execution of the program by the P/E.C., the memory accepts only the RSR (Read Status Register) and PES (Program/Erase Suspend) instructions.

Double Word Program (DPG)

This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel.The two words must differ only for the address A0. Programming should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH} but result could be uncertain. This instruction uses three write cycles. The first command written is the Double Word Program Set-Up command 30h. A second write operation latches the Address and the Data of the first word to be written, the third write operation latches the Address and the Data of the second word to be written and starts the P/E.C. Read operations output the Status Register content after the programming has started. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status register bit b1 returns '1' if the user is attempting to program a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}. Programming aborts if $\overline{RP}$ goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be erased and reprogrammed. A Clear Status Register instruction must be issued to reset b4, b3 and b1 of the Status Register.

During the execution of the program by the P/E.C., the memory accepts only the RSR (Read Status Register) and PES (Program/Erase Suspend) instructions.

Clear Status Register (CLRS)

The Clear Status Register uses a single write operation which clears bits b1, b3, b4 and b5 to '0'. Its use is necessary before any new operation when an error has been detected.

The Clear Status Register is executed writing the command 50h.

Program/Erase Suspend (PES)

Program/Erase suspend is accepted only during the Program Erase instruction execution. When a Program/Erase Suspend command is written to the C.I., the P/E.C. freezes the Program/Erase operation. Program/Erase Resume (PER) continues the Program/Erase operation. Program/Erase Suspend consists of writing the command B0h without any specific address.

The Status Register bit b2 is set to '1' (within 5µs) when the program has been suspended. b2 is set to '0' in case the program is completed or in progress. The Status Register bit b6 is set to '1' (within 30µs) when the erase has been suspended. b6 is set to '0' in case the erase is completed or in progress. The valid commands while erase is suspended are Program/Erase Resume, Program, Read Array, Read Status Register, Read Identifier, CFI Query. While program is suspended the same command set is valid except for program instruction. During program/erase suspend mode, the chip can be placed in a pseudo-stand-by mode by taking $\overline{E}$ to V_{IH}. This reduces active current consumption. Program/Erase is aborted if $\overline{RP}$ turns to V_{IL}.

Program/Erase Resume (PER)

If a Program/Erase Suspend instruction was previously executed, the program/erase operation may be resumed by issuing the command D0h. The status register bit b2/b6 is cleared when program/erase resumes. Read operations output the status register after the program/erase is resumed.

The suggested flow charts for programs that use the programming, erasure and program/erase suspend/resume features of the memories are shown from Figures 10, 11, 12, 13 and 14.

Table 11. Program, Erase Times and Program/Erase Endurance Cycles
(T_A = 0 to 70°C or –40 to 85°C; V_{DD} = 2.7V to 3.6V)

Parameter	Test Conditions	M28W160B			Unit
		Min	Typ (1)	Max	
Word Program	$V_{PP} = V_{DD}$		10	200	µs
Double Word Program	V_{PP} = 12V ±5%		10	200	µs
Main Block Program	V_{PP} = 12V ±5%		0.16	5	sec
	$V_{PP} = V_{DD}$		0.32	5	sec
Parameter Block Program	V_{PP} = 12V ±5%		0.02	4	sec
	$V_{PP} = V_{DD}$		0.04	4	sec
Main Block Erase	V_{PP} = 12V ±5%		1	10	sec
	$V_{PP} = V_{DD}$		1	10	sec
Parameter Block Erase	V_{PP} = 12V ±5%		0.8	10	sec
	$V_{PP} = V_{DD}$		0.8	10	sec
Program/Erase Cycles (per Block)		100,000			cycles

Note: T_A = 25 °C.

BLOCK PROTECTION

Two parameter blocks (#0 and #1) can be protected against Program or Erase to ensure extra data security. Unprotected blocks can be programmed or erased.

$\overline{WP}$ tied to V_{IL} protects the two lockable blocks. V_{PP} below V_{PPLK} protects all the blocks. Any program or erase operation on protected blocks is aborted. The Status Register tracks when the event occurs.

Table 9 defines the protection methods.

POWER CONSUMPTION

The M28W160B puts itself in one of four different modes depending on the status of the control signals: Active Power, Automatic Stand-by, Stand-by and Reset define decreasing levels of current consumption. These allow the memory power to be minimised, in turn decreasing the overall system power consumption. As different recovery time are linked to the different modes, please refer to the AC timing table to design your system.

Active Power

When $\overline{E}$ is at V_{IL} and $\overline{RP}$ is at V_{IH}, the device is in active mode. Refer to DC Characteristics to get the values of the current supply consumption.

Automatic Stand-by

Automatic Stand-by provides a low power consumption state during read mode. Following a read operation, after a delay close to the memory access time, the device enters Automatic Stand-by: the Supply Current is reduced to I_{CC1} values. The device keeps the last output data stable, till a new location is accessed.

Stand-by or Reset

Refer to the Device Operations section.

Power Up

The Supply voltage V_{DD} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{DD} is above V_{LKO}. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled if $\overline{RP}$ is at V_{IL}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{DD} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{DD} and V_{PP} pins. The PCB trace widths should be sufficient to carry the required V_{PP} program and erase currents.

COMMON FLASH INTERFACE (CFI)

The Common Flash Interface (CFI) specification is a JEDEC approved, standardised data structure that can be read from the Flash memory device. CFI allows a system software to query the flash device to determine various electrical and timing parameters, density information and functions supported by the device. CFI allows the system to easily interface to the Flash memory, to learn about its features and parameters, enabling the software to configure itself when necessary.

Tables 12, 13, 14, 15, 16 and 17 show the address used to retrieve each data.

The CFI data structure gives information on the device, such as the sectorization, the command set and some electrical specifications. Tables 12, 13, 14 and 15 show the addresses used to retrieve each data. The CFI data structure contains also a security area; in this section, a 64 bit unique security number is written, starting at address 80h. This area can be accessed only in read mode by the final user and there are no ways of changing the code after it has been written by ST. Write a read instruction to return to Read mode. Refer to the CFI Query instruction to understand how the M28W160B enters the CFI Query mode.

Table 12. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Note: The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in Tables 13, 14, 15, 16 and 17. Query data are always presented on the lowest order data outputs.

Table 13. CFI Query Identification String

Offset	Data	Description
00h	0020h	Manufacturer Code
01h	0090h - top 0091h - bottom	Device Code
02h-0Fh	reserved	Reserved
10h	0051h	Query Unique ASCII String "QRY"
11h	0052h	Query Unique ASCII String "QRY"
12h	0059h	Query Unique ASCII String "QRY"
13h 14h	0003h 0000h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm
15h 16h	offset = P = 0035h 0000h	Address for Primary Algorithm extended Query table
17h 18h	0000h 0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists)
19h 1Ah	value = A = 0000h 0000h	Address for Alternate Algorithm extended Query table note: 0000h means none exists

Note: Query data are always presented on the lowest - order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 14. CFI Query System Interface Information

Offset	Data	Description
1Bh	0027h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV
1Ch	0036h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV
1Dh	00B4h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV Note: This value must be 0000h if no V_{PP} pin is present
1Eh	00C6h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV Note: This value must be 0000h if no V_{PP} pin is present
1Fh	0004h	Typical timeout per single byte/word program (multi-byte program count = 1), 2^n µs (if supported; 0000h = not supported)
20h	0000h	Typical timeout for maximum-size multi-byte program or page write, 2^n µs (if supported; 0000h = not supported)
21h	000Ah	Typical timeout per individual block erase, 2^n ms (if supported; 0000h = not supported)
22h	0000h	Typical timeout for full chip erase, 2^n ms (if supported; 0000h = not supported)
23h	0004h	Maximum timeout for byte/word program, 2^n times typical (offset 1Fh) (0000h = not supported)
24h	0000h	Maximum timeout for multi-byte program or page write, 2^n times typical (offset 20h) (0000h = not supported)
25h	0003h	Maximum timeout per individual block erase, 2^n times typical (offset 21h) (0000h = not supported)
26h	0000h	Maximum timeout for chip erase, 2^n times typical (offset 22h) (0000h = not supported)

Table 15. Device Geometry Definition

Offset Word Mode	Data	Description
27h	0015h	Device Size = 2^n in number of bytes
28h	0001h	Flash Device Interface Code description: Asynchronous x16
29h	0000h	
2Ah	0000h	Maximum number of bytes in multi-byte program or page = 2^n
2Bh	0000h	
2Ch	0002h	Number of Erase Block Regions within device bit 7 to 0 = x = number of Erase Block Regions Note:1. x = 0 means no erase blocking, i.e. the device erases at once in "bulk." 2. x specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size. For example, a 128KB device (1Mb) having blocking of 16KB, 8KB, four 2KB, two 16KB, and one 64KB is considered to have 5 Erase Block Regions. Even though two regions both contain 16KB blocks, the fact that they are not contiguous means they are separate Erase Block Regions. 3. By definition, symmetrically block devices have only one blocking region.
M28W160BT	M28W160BT	Erase Block Region Information
2Dh	001Eh	bit 31 to 16 = z, where the Erase Block(s) within this Region are (z) times 256 bytes in size. The value z = 0 is used for 128 byte block size. e.g. for 64KB block size, z = 0100h = 256 => 256 * 256 = 64K
2Eh	0000h	
2Fh	0000h	
30h	0001h	bit 15 to 0 = y, where y+1 = Number of Erase Blocks of identical size within the Erase Block Region: e.g. y = D15-D0 = FFFFh => y+1 = 64K blocks [maximum number] y = 0 means no blocking (# blocks = y+1 = "1 block") Note: y = 0 value must be used with number of block regions of one as indicated by (x) = 0
31h	0007h	
32h	0000h	
33h	0020h	
34h	0000h	
M28W160BB	M28W160BB	
2Dh	0007h	
2Eh	0000h	
2Fh	0020h	
30h	0000h	
31h	001Eh	
32h	0000h	
33h	0000h	
34h	0001h	

Table 16. Primary Algorithm-Specific Extended Query Table

Offset	Data	Description
(P)h = 35h	0050h 0052h 0049h	Primary Algorithm extended Query table unique ASCII string "PRI"
(P+3)h = 38h	0031h	Major version number, ASCII
(P+4)h = 39h	0030h	Minor version number, ASCII
(P+5)h = 3Ah (P+7)h (P+8)h	0006h 0000h 0000h 0000h	Extended Query table contents for Primary Algorithm bit 0 Chip Erase supported (1 = Yes, 0 = No) bit 1 Erase Suspend supported (1 = Yes, 0 = No) bit 2 Program Suspend (1 = Yes, 0 = No) bit 3 Lock/Unlock supported (1 = Yes, 0 = No) bit 4 Quequed Erase supported (1 = Yes, 0 = No) bit 31 to 5 Reserved; undefined bits are '0'
(P+9)h = 3Eh	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query are always supported during Erase or Program operation bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No) bit 7 to 1 Reserved; undefined bits are '0'
(P+A)h = 3Fh (P+B)h	0000h 0000h	Block Lock Status Defines which bits in the Block Status Register section of the Query are implemented. bit 0 Block Lock Status Register Lock/Unlock bit active (1 = Yes, 0 = No) bit 1 Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No) bit 15 to 2 Reserved for future use; undefined bits are '0'
(P+C)h = 41h	0027h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV
(P+D)h = 42h	00C0h	V_{PP} Supply Optimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV
(P+E)h	0000h	Reserved

Table 17. Security Code Area

Offset	Data	Description
81h	XXXX	64 bits unique device number.
82h	XXXX	
83h	XXXX	
84h	XXXX	

Table 18. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{DD} = V_{DDQ} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ V_{DDQ}			±1	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤V_{DDQ}			±10	µA
I_{CC}	Supply Current (Read)	$\overline{E}$ = V_{SS}, $\overline{G}$ = V_{IH}, f = 5MHz		10	20	mA
I_{CC1}	Supply Current (Stand-by or Automatic Stand-by)	$\overline{E}$ = V_{DDQ} ± 0.2V, $\overline{RP}$ = V_{DDQ} ± 0.2V		15	50	µA
I_{CC2}	Supply Current (Reset)	$\overline{RP}$ = V_{SS} ± 0.2V		15	50	µA
I_{CC3}	Supply Current (Program)	Program in progress V_{PP} = 12V ± 5%		10	20	mA
		Program in progress V_{PP} = V_{DD}		10	20	mA
I_{CC4}	Supply Current (Erase)	Erase in progress V_{PP} = 12V ± 5%		5	20	mA
		Erase in progress V_{PP} = V_{DD}		5	20	mA
I_{CC5}	Supply Current (Program/Erase Suspend)	$\overline{E}$ = V_{DDQ} ± 0.2V, Erase suspended			50	µA
I_{PP}	Program Current (Read or Stand-by)	V_{PP} > V_{DD}			400	µA
I_{PP1}	Program Current (Read or Stand-by)	V_{PP} ≤ V_{DD}			5	µA
I_{PP2}	Program Current (Reset)	$\overline{RP}$ = V_{SS} ± 0.2V			5	µA
I_{PP3}	Program Current (Program)	Program in progress V_{PP} = 12V ± 5%			10	mA
		Program in progress V_{PP} = V_{DD}			5	µA
I_{PP4}	Program Current (Erase)	Erase in progress V_{PP} = 12V ± 5%			10	mA
		Erase in progress V_{PP} = V_{DD}			5	µA
V_{IL}	Input Low Voltage		–0.5		0.4	V
		V_{DDQ} ≥ 2.7V	–0.5		0.8	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} +0.4	V
		V_{DDQ} ≥ 2.7V	0.7 V_{DDQ}		V_{DDQ} +0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA, V_{DD} = V_{DD} min, V_{DDQ} = V_{DDQ} min			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA, V_{DD} = V_{DD} min, V_{DDQ} = V_{DDQ} min	V_{DDQ} –0.1			V
V_{PP1}	Program Voltage (Program or Erase operations)		1.65		3.6	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4		12.6	V
V_{PPLK}	Program Voltage (Program and Erase lock-out)				1	V
V_{LKO}	V_{DD} Supply Voltage (Program and Erase lock-out)				2	V

Table 19. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to V_{DDQ}
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$

Figure 5. AC Testing Load Circuit

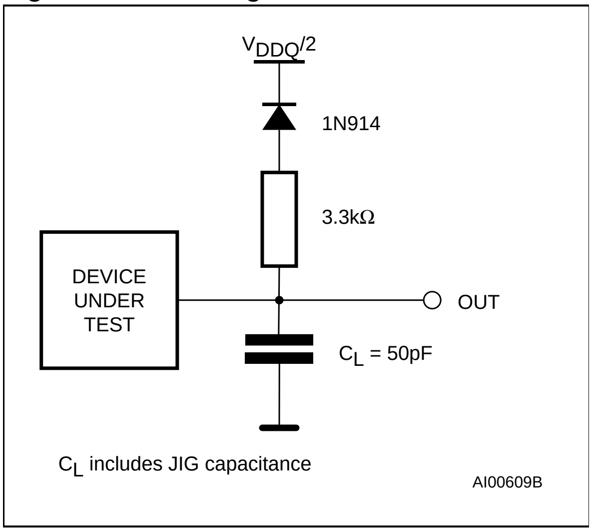


Figure 4. AC Testing Input Output Waveform

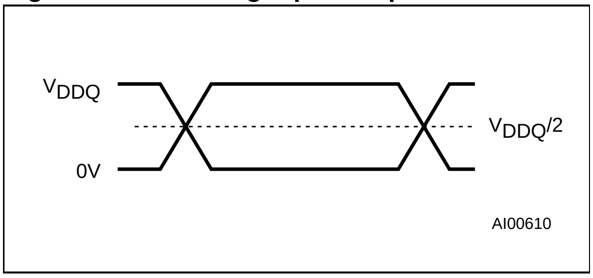


Table 20. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

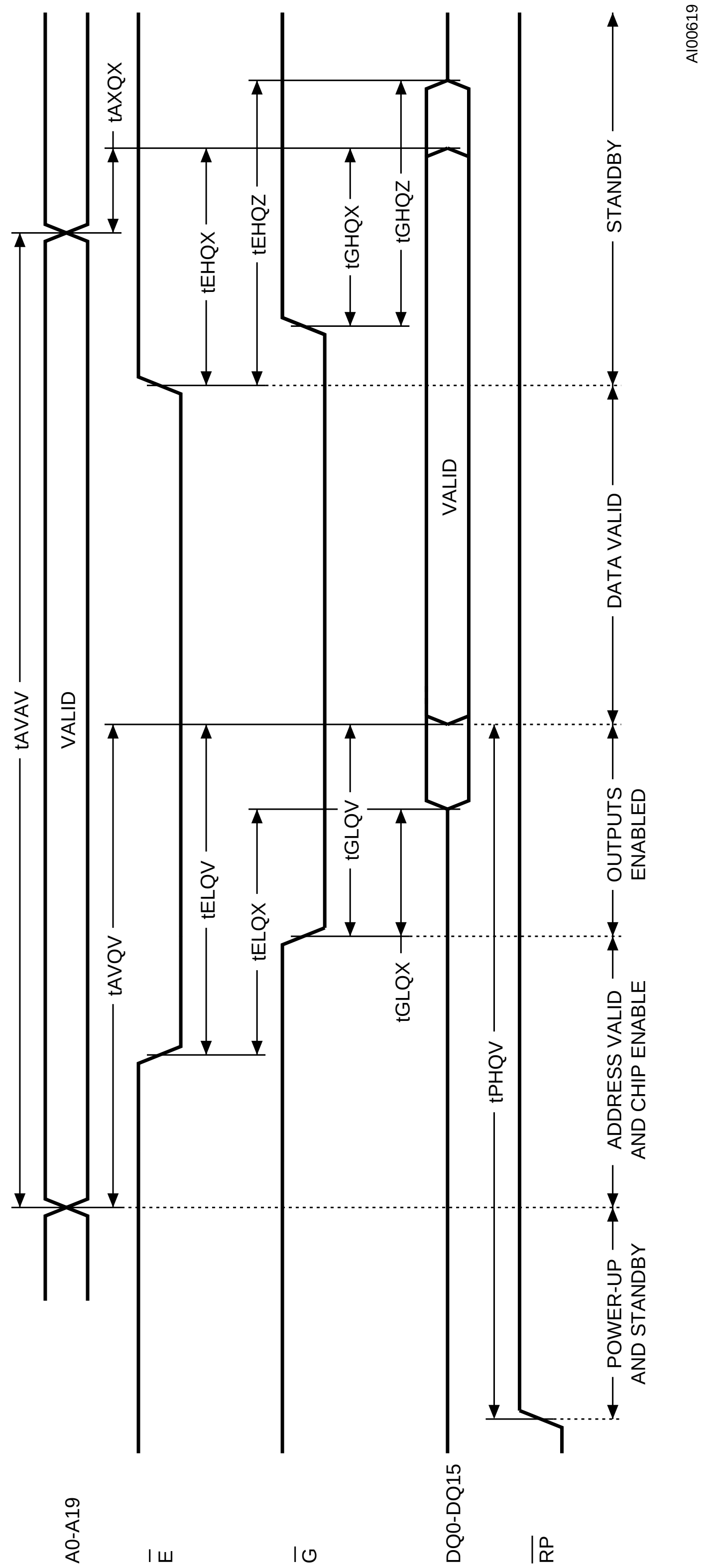
Note: 1. Sampled only, not 100% tested.

Table 21. Read AC Characteristics [1]
(T_A = 0 to 70°C or –40 to 85°C)

Symbol	Alt	Parameter	M28W160B				Unit
			90		100		
			V_{DD} = 2.7V to 3.6V V_{DDQ} = 2.7V min		V_{DD} = 2.7V to 3.6V V_{DDQ} = 1.65V min		
			Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	90		100		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		90		100	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		25		30	ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		90		100	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		25		30	ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		30		35	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{PHQV}	t_{PWH}	Reset High to Output Valid		150		150	ns
t_{PLPH} (2,4)	t_{RP}	Reset Pulse Width	100		100		ns

Note: 1. See AC Testing Measurement conditions for timing measurements.
2. Sampled only, not 100% tested.
3. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
4. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.

Figure 6. Read AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Table 22. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C or –40 to 85°C)

Symbol	Alt	Parameter	M28W160B				Unit
			90		100		
			V_{DD} = 2.7V to 3.6V V_{DDQ} = 2.7V min		V_{DD} = 2.7V to 3.6V V_{DDQ} = 1.65V min		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	90		100		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		50		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{PHWL}	t_{PS}	Reset High to Write Enable Low	90		100		ns
t_{PLPH} (2, 3)	t_{RP}	Reset Pulse Width	100		100		ns
t_{PLRH} (2, 4)		Reset Low to Program/Erase Abort		30		30	µs
t_{QVVPL} (2, 5)		Output Valid to V_{PP} Low	0		0		ns
t_{QVWPL}		Data Valid to Write Protect Low	0		0		ns
t_{VPHWH} (2)	t_{VPS}	V_{PP} High to Write Enable High	200		200		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	0		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHGL}		Write Enable High to Output Enable Low	30		30		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{WPHWH}		Write Protect High to Write Enable High	50		50		ns

Note: 1. See AC Testing Measurement conditions for timing measurements.
2. Sampled only, not 100% tested.
3. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
4. The reset will complete within 100ns if $\overline{RP}$ is asserted while not in Program nor in Erase mode.
5. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled

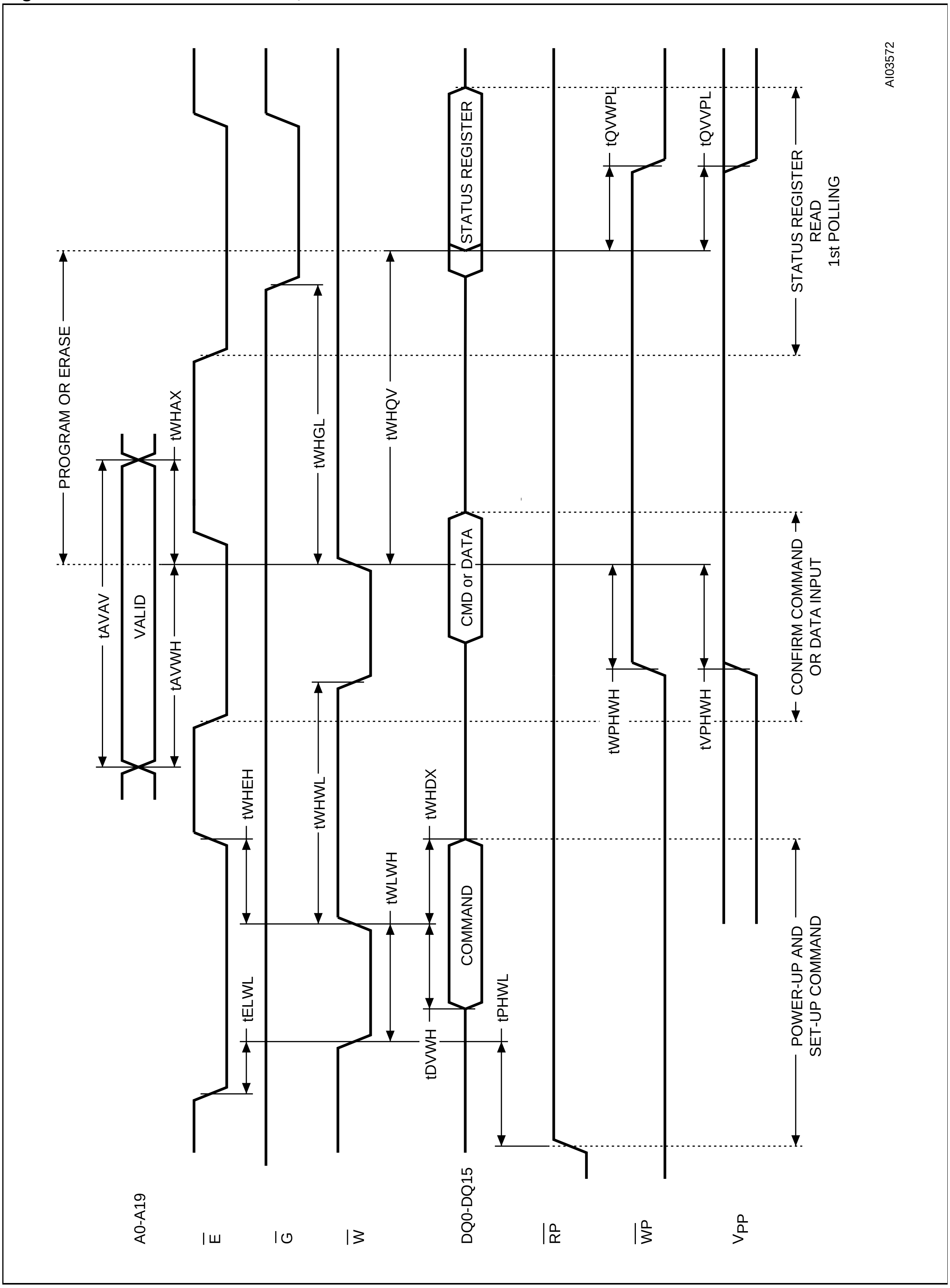


Table 23. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C or –40 to 85°C)

Symbol	Alt	Parameter	M28W160B				Unit
			90		100		
			V_{DD} = 2.7V to 3.6V V_{DDQ} = 2.7V min		V_{DD} = 2.7V to 3.6V V_{DDQ} = 1.65V min		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	90		100		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		50		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	0		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{EHGL}		Chip Enable High to Output Enable Low	30		30		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{PHEL}	t_{PS}	Reset High to Chip Enable Low	90		100		ns
t_{PLPH} (2, 3)	t_{RP}	Reset Pulse Width	100		100		ns
t_{PLRH} (2, 4)		Reset Low to Program/Erase Abort		30		30	µs
t_{QVVPL} (2, 5)		Output Valid to V_{PP} Low	0		0		ns
t_{QVWPL}		Data Valid to Write Protect Low	0		0		ns
t_{VPHEH} (2)	t_{VPS}	V_{PP} High to Chip Enable High	200		200		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{WPHEH}		Write Protect High to Chip Enable High	50		50		ns

Note: 1. See AC Testing Measurement conditions for timing measurements.
2. Sampled only, not 100% tested.
3. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
4. The reset will complete within 100ns if $\overline{RP}$ is asserted while not in Program nor in Erase mode.
5. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled

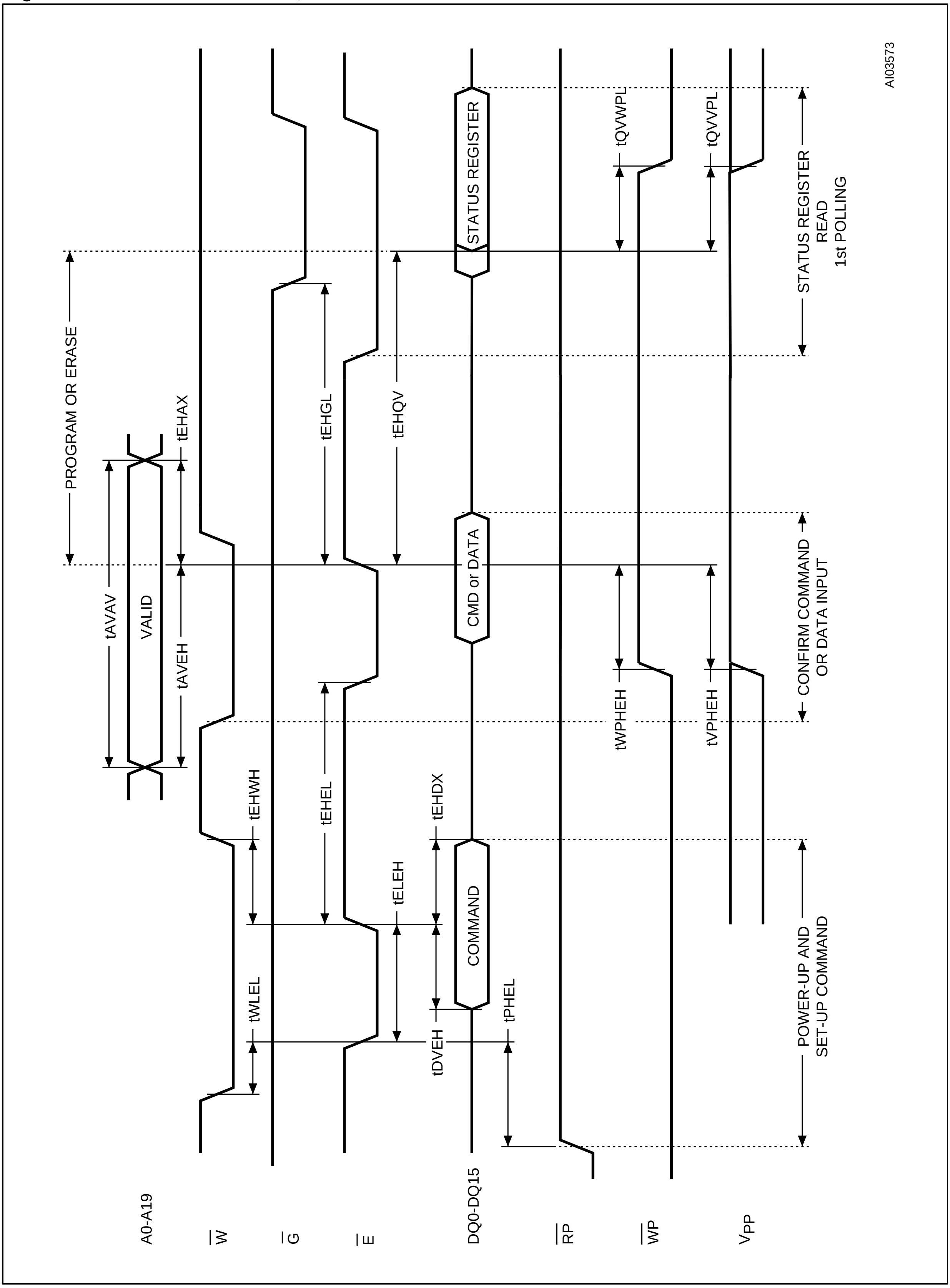


Figure 9. Reset AC Waveform

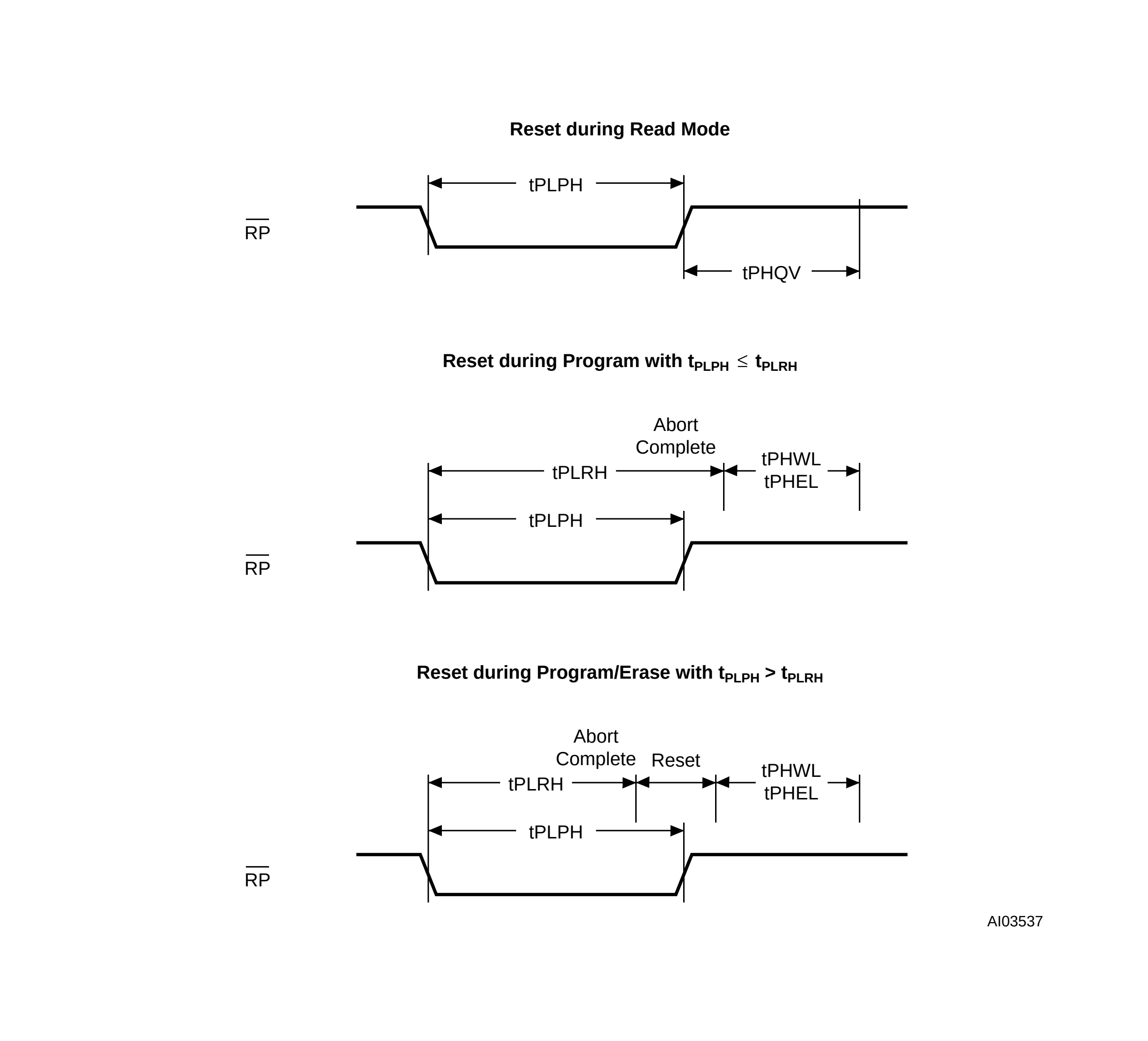
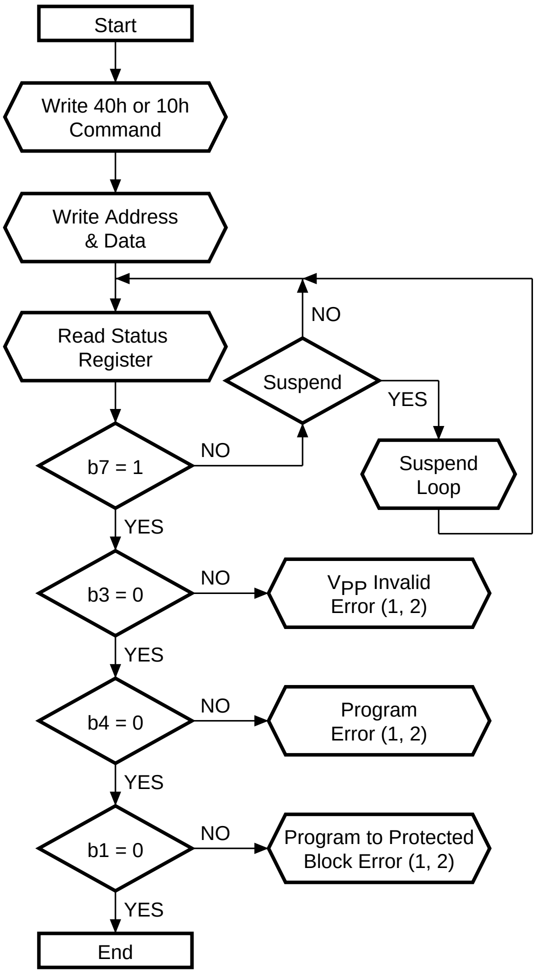


Figure 10. Program Flowchart and Pseudo Code



Program instruction:
– write 40h or 10h command
– write Address & Data
(memory enters read status state after the Program instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled) if PES instruction given execute suspend program loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4 = 1, Program error:
– error handler

If b1 = 1, Program to protected block error:
– error handler

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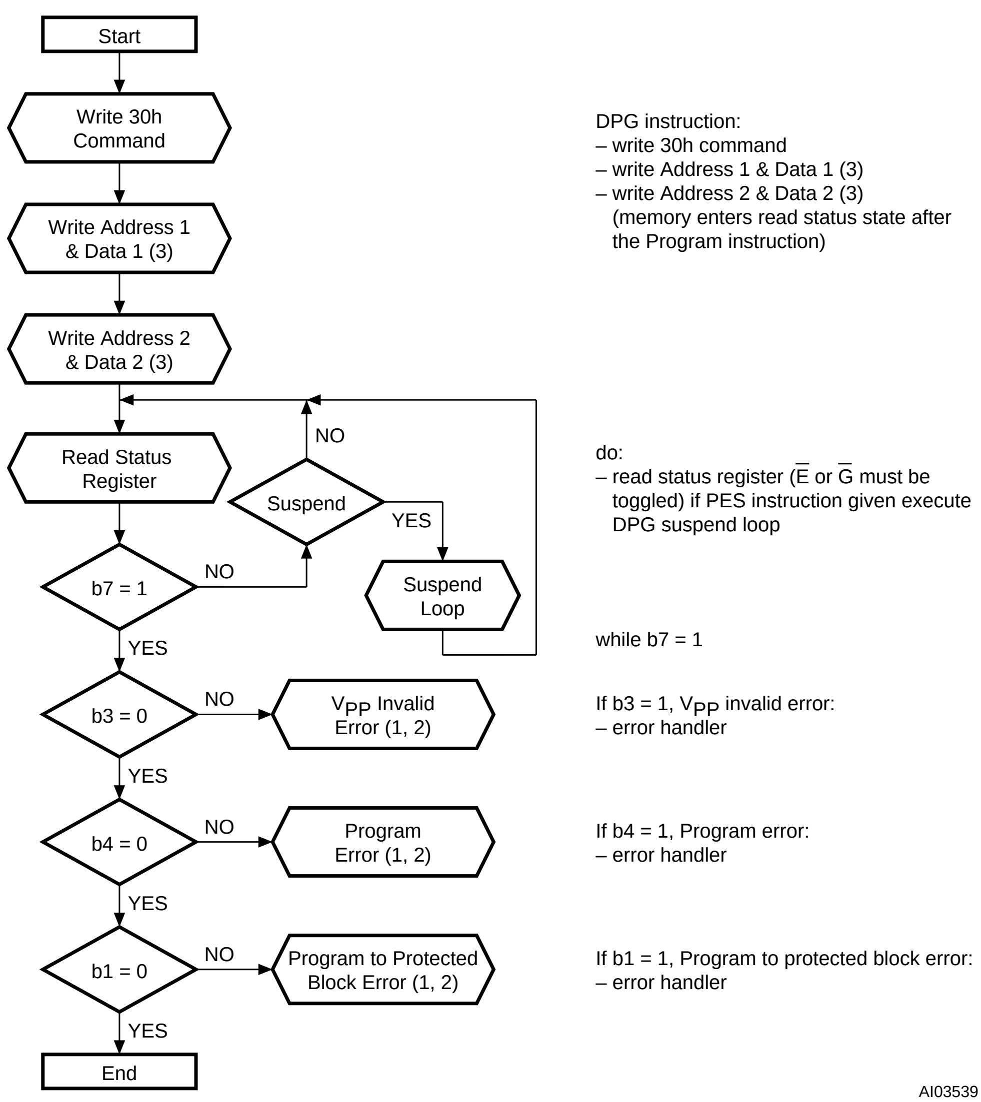
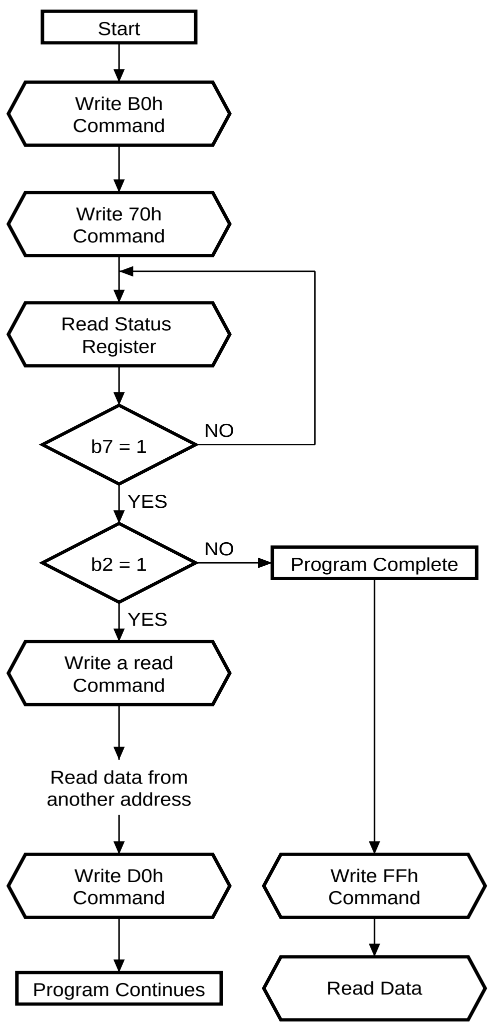
Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operationor after a sequence.
2. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 11. Double Word Program Flowchart and Pseudo Code



Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.
3. Address 1 and Address 2 must be consecutive addresses differing only for bit A0.

Figure 12. Program or DPG Suspend & Resume Flowchart and Pseudo Code



PES instruction:
– write B0h command
do:
– read status register
  ($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b2 = 0 Program completed

PER instruction:
– write D0h command to resume the program
– if the program operation completed then this is not necessary.
  The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

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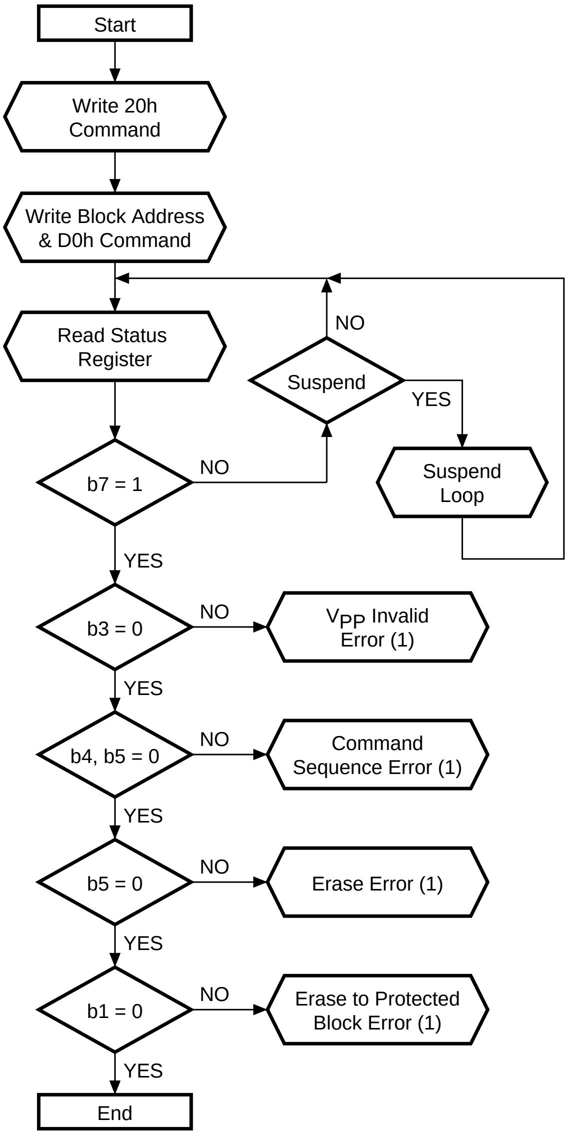
Figure 13. Erase Flowchart and Pseudo Code



EE instruction:
– write 20h command
– write Block Address (A12-A20) & command D0h (memory enters read status state after the EE instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled) if PES instruction given execute suspend erase loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4, b5 = 1, Command sequence error:
– error handler

If b5 = 1, Erase error:
– error handler

If b1 = 1, Erase to protected block error:
– error handler

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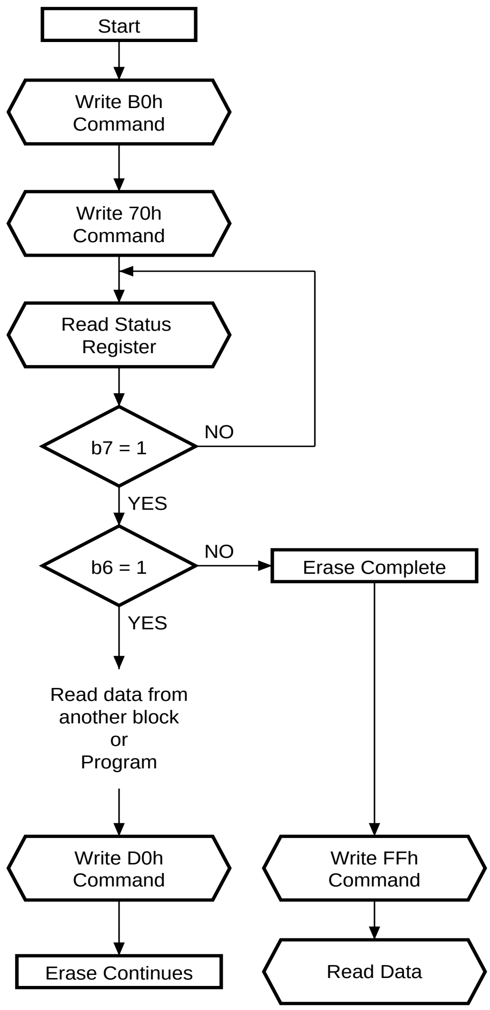
Note: 1. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 14. Erase Suspend & Resume Flowchart and Pseudo Code



PES instruction:
– write B0h command
do:
– read status register
(Ē or Ḡ must be toggled)

while b7 = 1

If b6 = 0, Erase completed

PER instruction:
– write D0h command to resume erasure
– if the erase operation completed then this is not necessary.
The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

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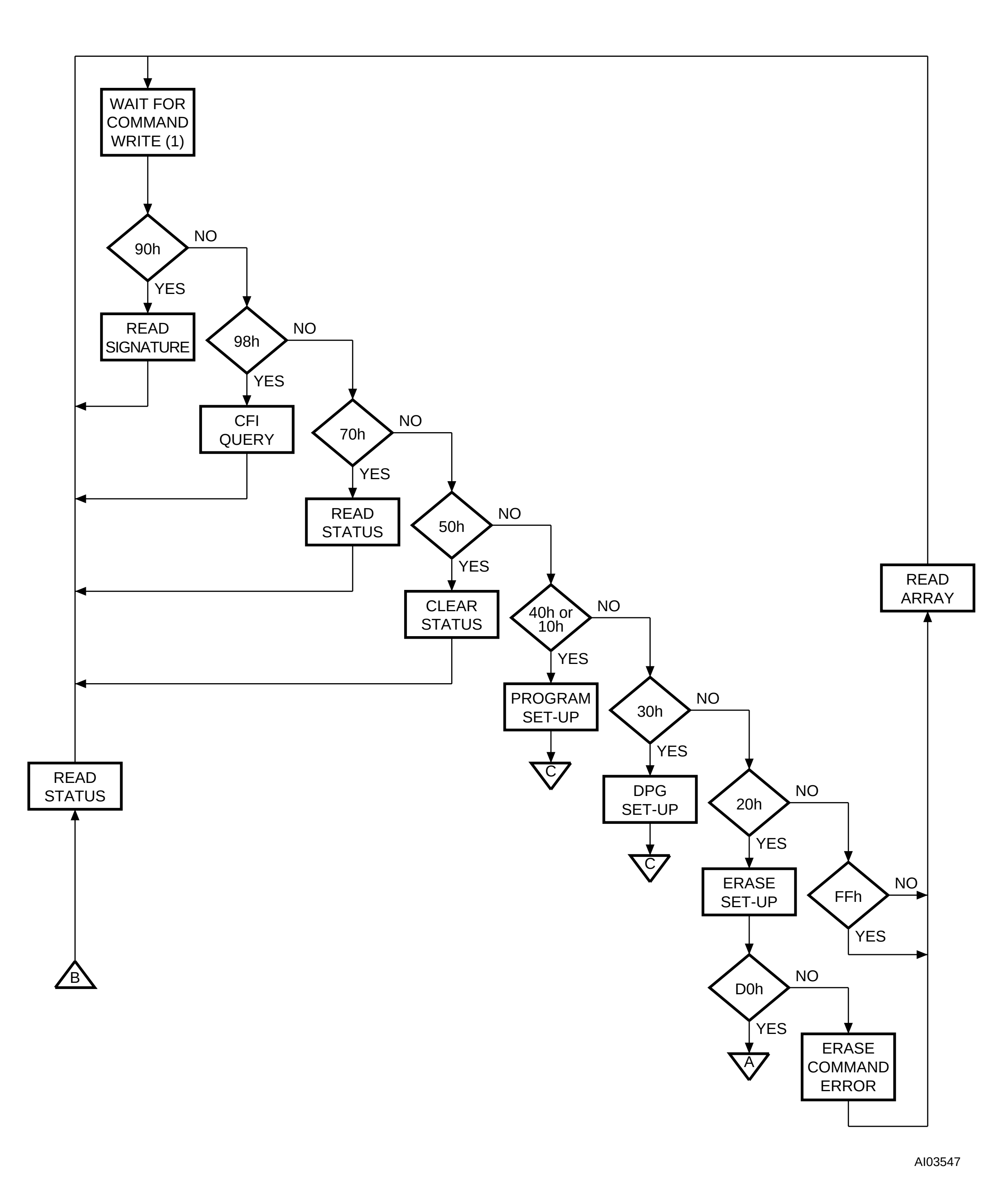
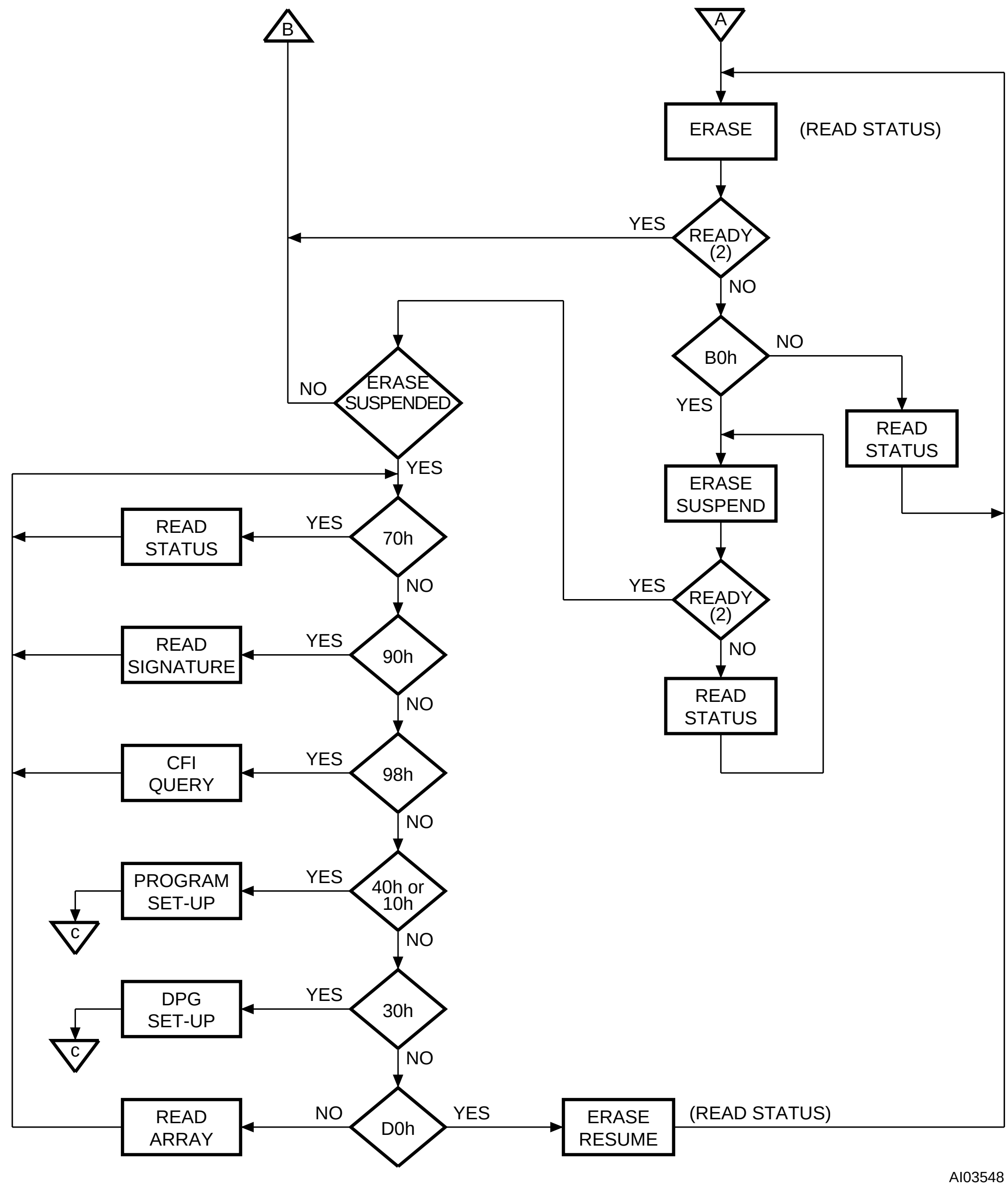
Figure 15. Command Interface and Program Erase Controller Flowchart (a)



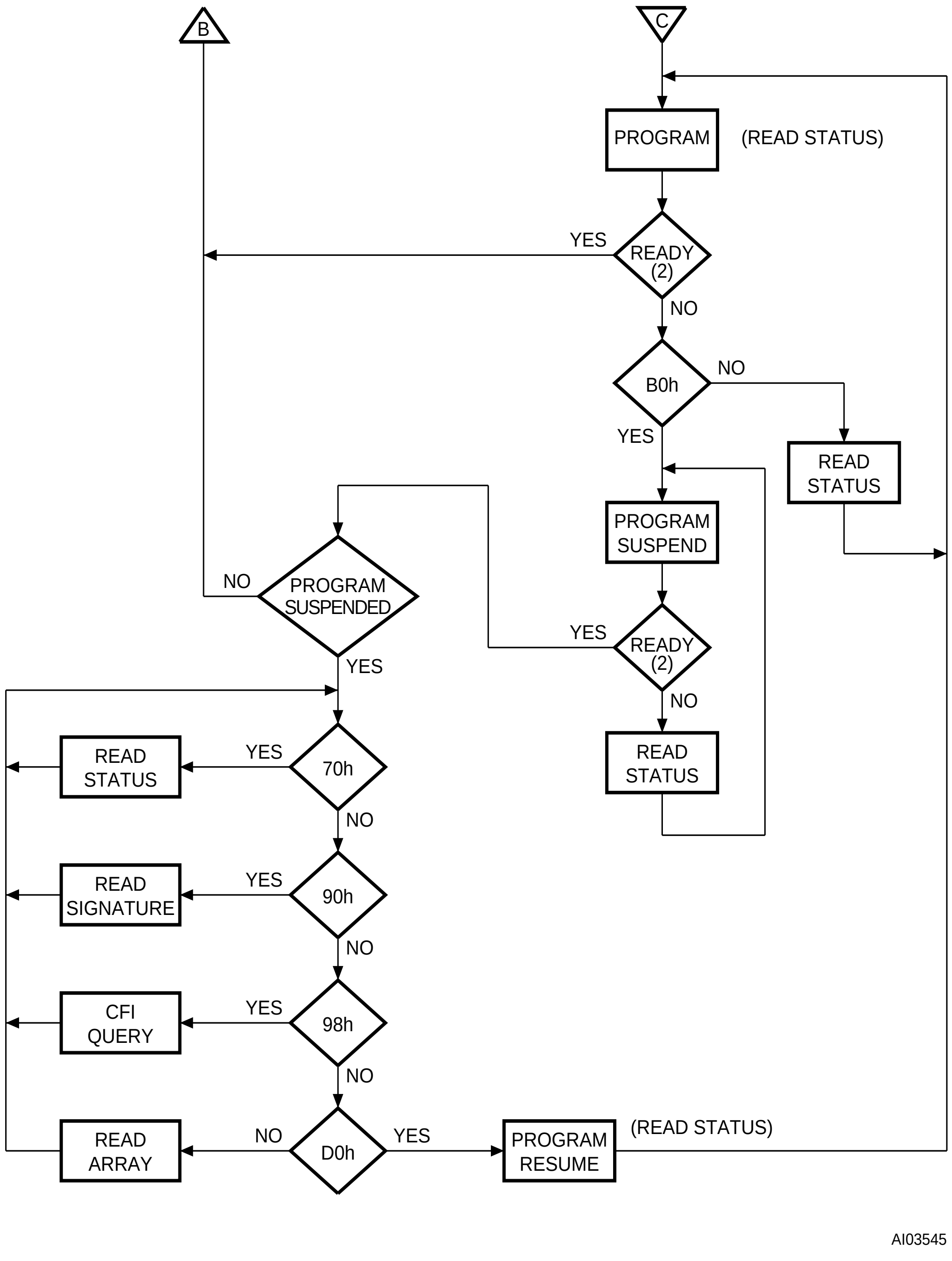
Note: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{DD} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 16. Command Interface and Program Erase Controller Flowchart (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 17. Command Interface and Program Erase Controller Flowchart (c)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Table 24. Ordering Information Scheme

Example: M28W160BT 90 N 6 T

Device Type
M28

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = 1.65V or 2.7V

Device Function
160B = 16 Mbit (1Mb x16), Boot Block

Array Matrix
T = Top Boot
B = Bottom Boot

Random Speed
90 = 90 ns
100 = 100 ns

Package
N = TSOP48: 12 x 20 mm
GB = µBGA46: 0.75 mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

Table 25. Daisy Chain Ordering Scheme

Example: M28W160B -GB T

Device Type
M28W160B

Daisy Chain
-GB = µBGA46: 0.75 mm pitch

Option
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

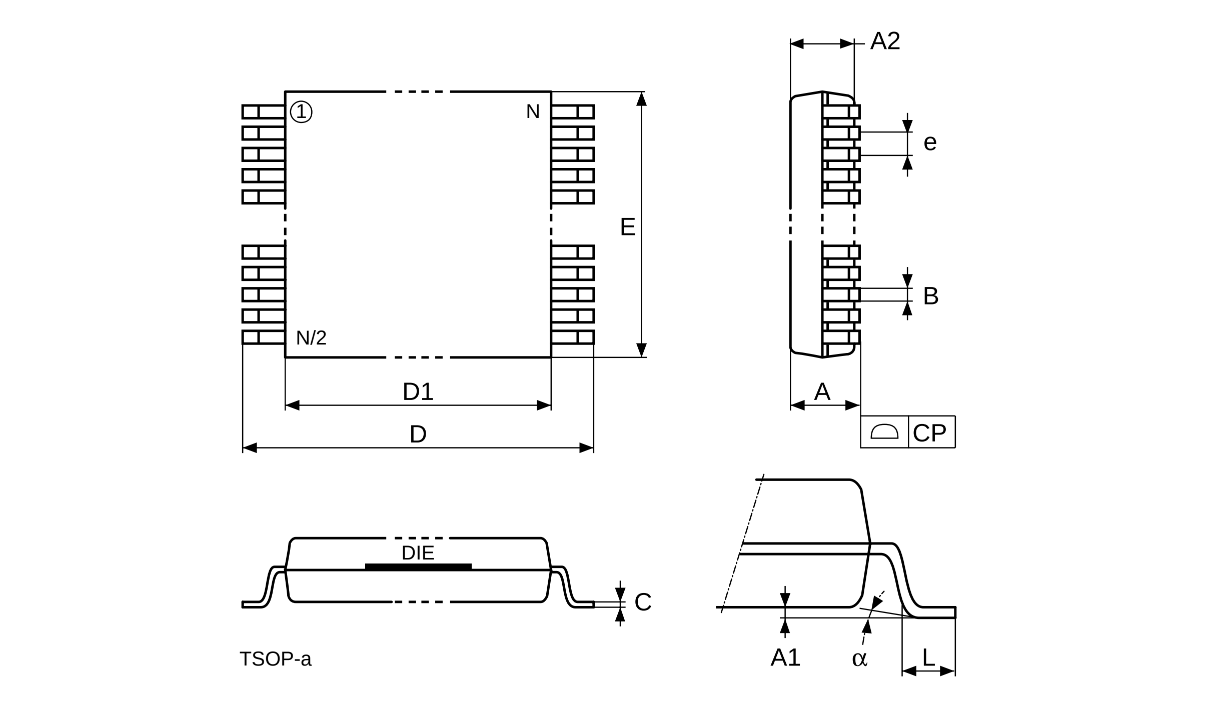
Table 26. Revision History

Date	Revision Details
July 1999	First Issue
09/21/99	Parameter Block Erase Typ. specification change (Table 11) Added t_{WHGL} and t_{EHGL} (Tables 22, 23 and Figures 7, 8)
10/20/99	µBGA Package Mechanical Data change (Table 27) Daisy Chain diagrams, Package and PCB Connections, added (Figures 20, 21)
02/09/00	Access Time conditions change Reset mode function change to remove Power Down mode Instructions description clarification Change of Parameter Block Erase value (Table 11) Block Protections description clarification Security Code Area definition change (Table 17) I_{CC2} and I_{CC3} value change (Table 18) t_{PLRH} value change (Tables 22, 23) Program, Erase, Command Interface flowcharts clarification (Figures 10, 11, 12, 13, 14, 15, 16, 17) µBGA Package Mechanical Data change (Table 28) µBGA Package Outline diagram change (Figure 19)
04/19/00	Document type: from Preliminary Data to Data Sheet Daisy Chain part numbering defined µBGA Daisy Chain diagrams, Package and PCB Connections re-designed (Figure 20, 21)
05/17/00	µBGA Package Outline diagram change (Figure 19)

Table 27. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		11.90	12.10		0.4685	0.4764
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.0039

Figure 18. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Outline

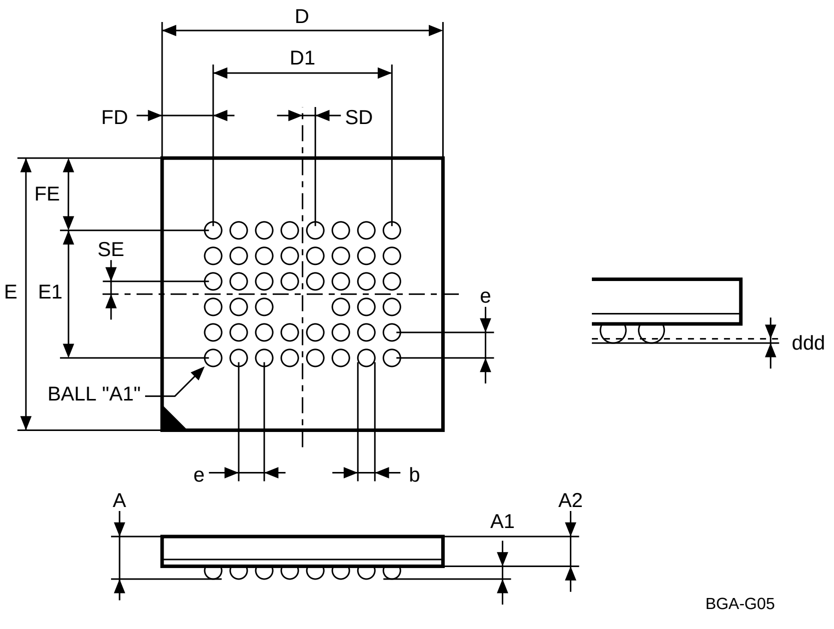


Drawing is not to scale.

Table 28. µBGA46 - 8 x 6 balls, 0.75 mm pitch, Package Mechanical Data

Symbol	mm			inch		
	Typ	Min	Max	Typ	Min	Max
A			1.000			0.0394
A1		0.180			0.0071	
A2	0.700	–	–	0.0276	–	–
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	6.390	6.340	6.440	0.2516	0.2496	0.2535
D1	5.250	–	–	0.2067	–	–
ddd			0.008			0.0003
e	0.750	–	–	0.0295	–	–
E	6.370	6.320	6.420	0.2508	0.2488	0.2528
E1	3.750	–	–	0.1476	–	–
FD	0.570	–	–	0.0224	–	–
FE	1.310	–	–	0.0516	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

Figure 19. µBGA46 - 8 x 6 balls, 0.75 mm pitch, Bottom View Package Outline



Drawing is not to scale.

Figure 20. µBGA46 Daisy Chain - Package Connections (Top view through package)

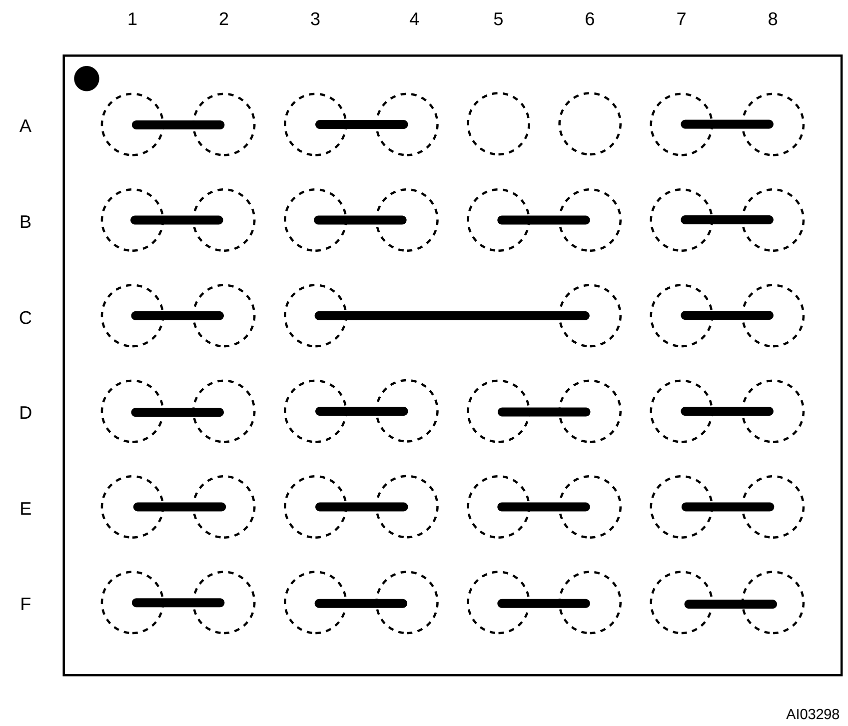


Figure 21. µBGA46 Daisy Chain - PCB Connections (Top view through package)