



# M24256-A

## 256 Kbit Serial I<sup>2</sup>C Bus EEPROM With Two Chip Enable Lines

PRELIMINARY DATA

- Compatible with I<sup>2</sup>C Extended Addressing
- Two Wire I<sup>2</sup>C Serial Interface  
Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24256-A
  - 2.5V to 5.5V for M24256-AW
  - 1.8V to 3.6V for M24256-AR
- 2 Chip Enable Inputs: up to four memories can be connected to the same I<sup>2</sup>C bus
- Hardware Write Control
- BYTE and PAGE WRITE (up to 64 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 100,000 Erase/Write Cycles
- More than 40 Year Data Retention

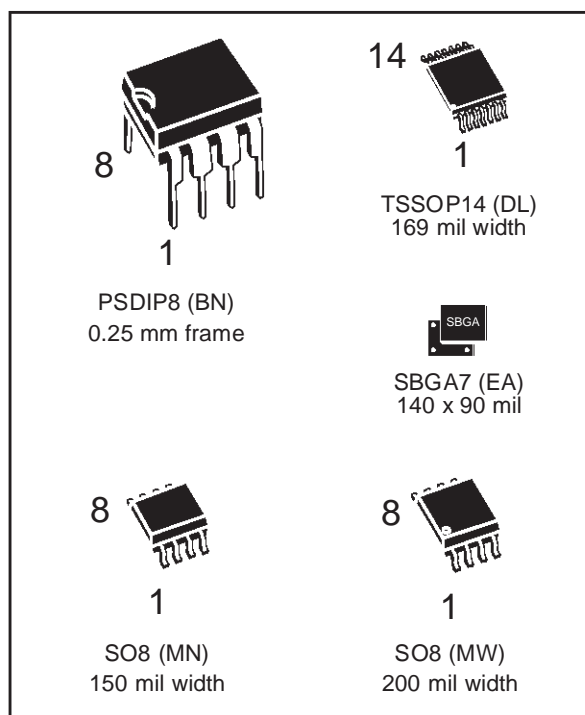
### DESCRIPTION

These I<sup>2</sup>C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 32Kx8 bits, and operate down to 2.5 V (for the M24256-AW), and down to 1.8 V (for the M24256-AR).

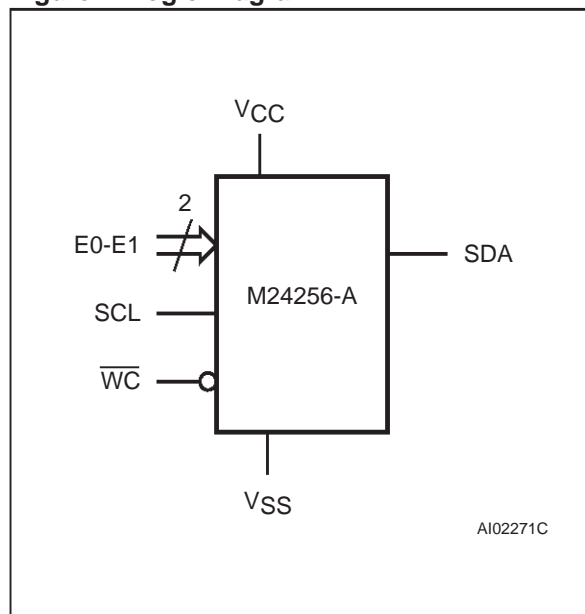
The M24256-A is available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages. The M24256-A is also available in a chip-scale (SBGA) package.

**Table 1. Signal Names**

E0, E1	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground

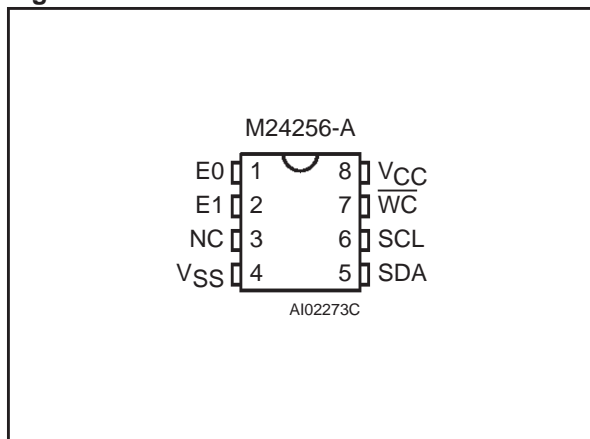


**Figure 1. Logic Diagram**



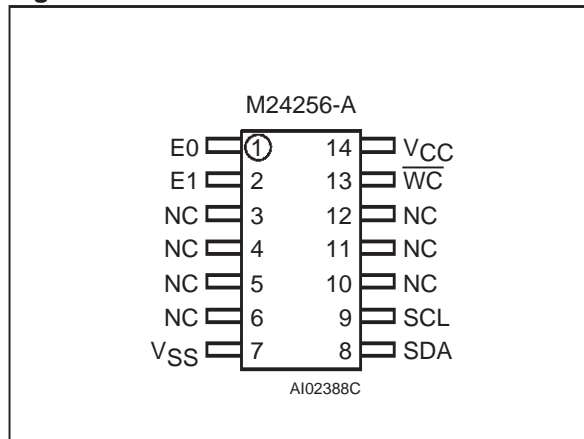
## M24256-A

**Figure 2A. DIP Connections**



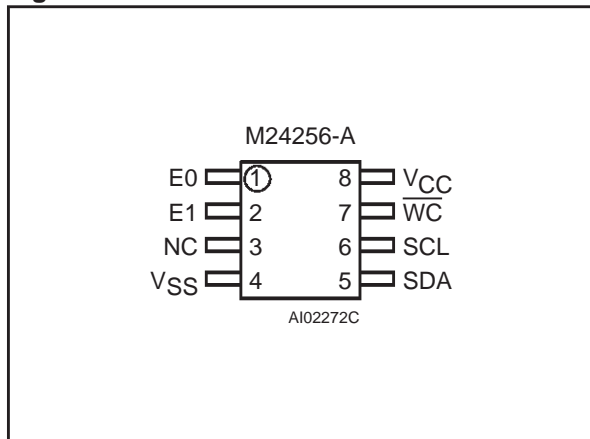
Note: 1. NC = Not Connected

**Figure 2C. TSSOP Connections**



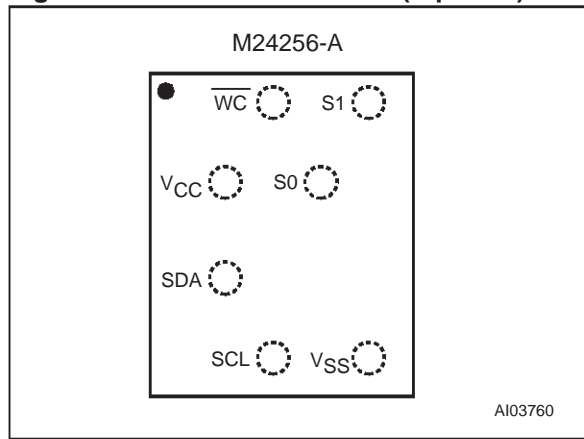
Note: 1. NC = Not Connected

**Figure 2B. SO Connections**



Note: 1. NC = Not Connected

**Figure 2D. SBGA Connections (top view)**



**Table 2. Absolute Maximum Ratings <sup>1</sup>**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	-40 to 125	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
T <sub>LEAD</sub>	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c. °C
V <sub>IO</sub>	Input or Output range	-0.6 to 6.5	V
V <sub>CC</sub>	Supply Voltage	-0.3 to 6.5	V
V <sub>ESD</sub>	Electrostatic Discharge Voltage (Human Body model) <sup>2</sup>	4000	V
	Electrostatic Discharge Voltage (Machine model) <sup>3</sup>	200	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.

2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

3. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

These memory devices are compatible with the I<sup>2</sup>C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I<sup>2</sup>C bus definition.

The memory behaves as a slave device in the I<sup>2</sup>C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R $\bar{W}$  bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9<sup>th</sup> bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

#### Power On Reset: V<sub>CC</sub> Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V<sub>CC</sub> voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V<sub>CC</sub> drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V<sub>CC</sub> must be applied before applying any logic signal.

## SIGNAL DESCRIPTION

### Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V<sub>CC</sub>. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

### Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V<sub>CC</sub>. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

### Chip Enable (E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the two least significant bits (b2, b1) of the 7-bit device select code. These inputs must be tied to V<sub>CC</sub> or V<sub>SS</sub> to establish the device select code. When unconnected, the E1 and E0 inputs are internally read as V<sub>IL</sub> (see Table 7 and Table 8)

### Write Control ( $\overline{WC}$ )

The hardware Write Control pin ( $\overline{WC}$ ) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ( $\overline{WC}=V_{IL}$ ) or disable ( $\overline{WC}=V_{IH}$ ) write instructions to the entire memory area. When

Figure 3. Maximum R<sub>L</sub> Value versus Bus Capacitance (C<sub>BUS</sub>) for an I<sup>2</sup>C Bus

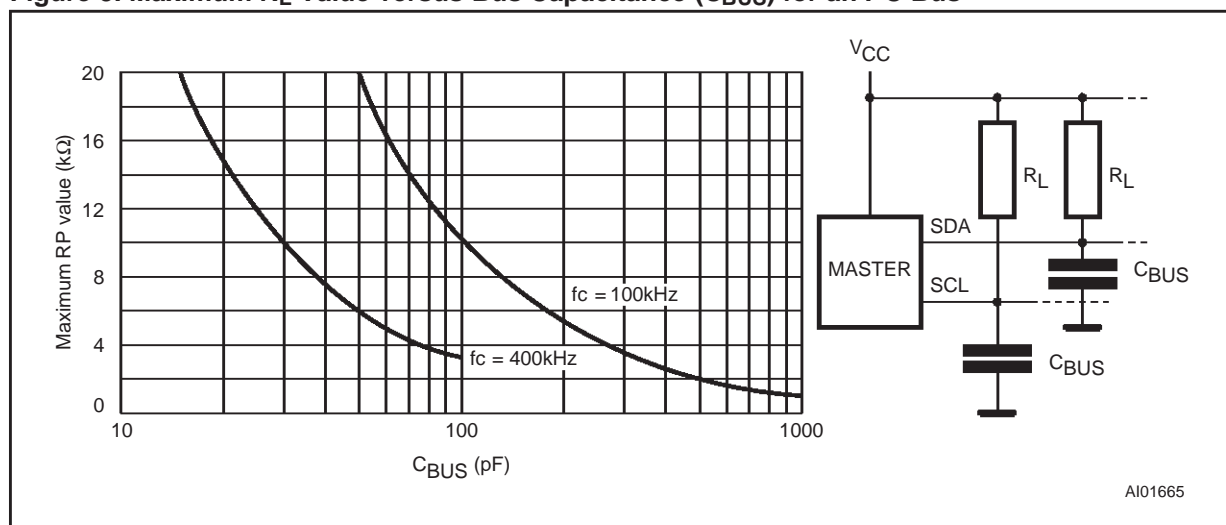
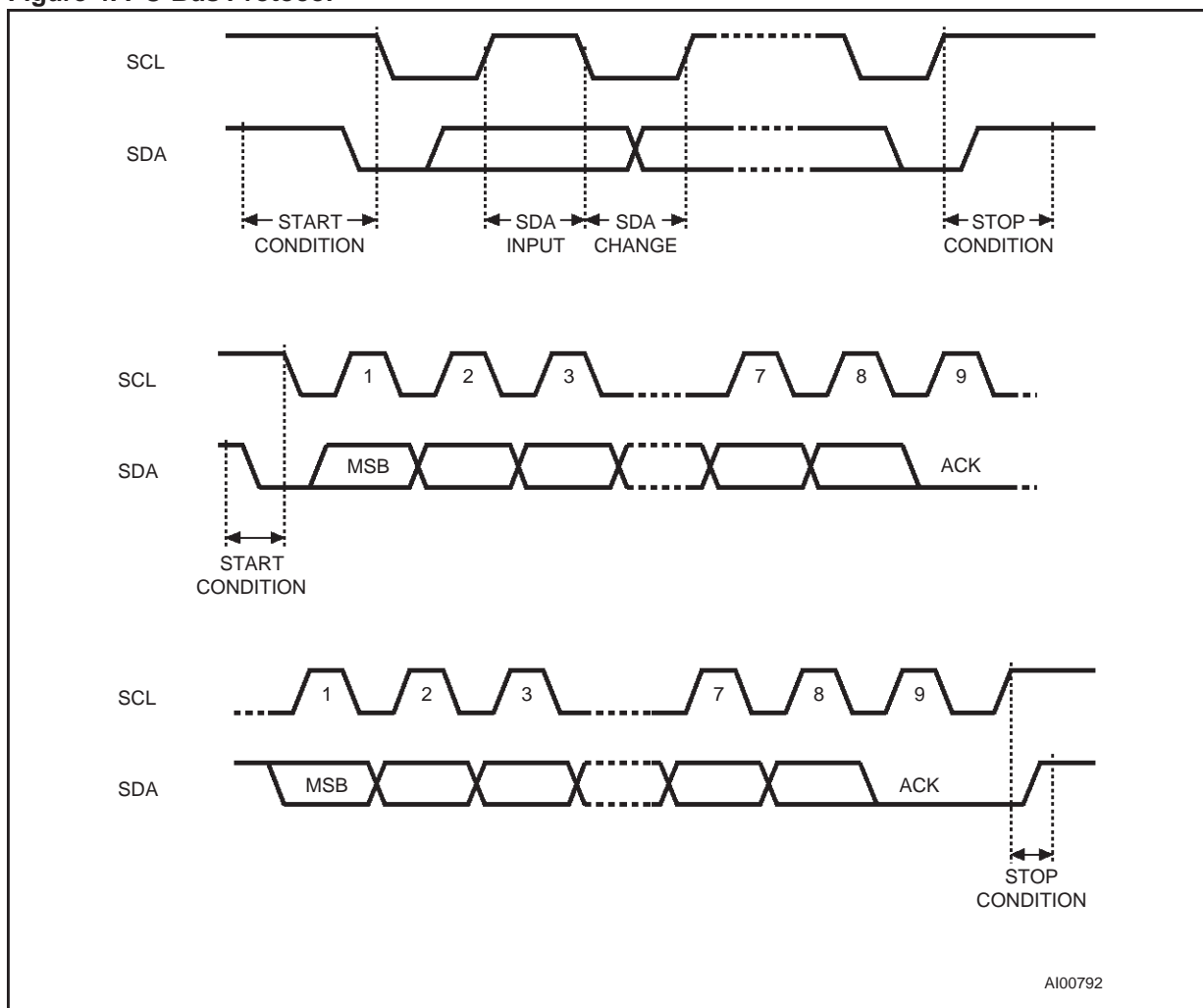


Figure 4. I<sup>2</sup>C Bus Protocol

unconnected, the  $\overline{WC}$  input is internally read as  $V_{IL}$ , and write operations are allowed.

When  $\overline{WC}=1$ , Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

#### DEVICE OPERATION

The memory device supports the I<sup>2</sup>C protocol. This is summarized in Figure 4, and is compared with other serial bus protocols in Application Note *AN1001*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory

device is always a slave device in all communication.

#### Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

#### Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

**Table 3. Device Select Code**<sup>1</sup>

	Device Type Identifier				Chip Enable			R $\bar{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	0	E1	E0	R $\bar{W}$

Note: 1. The most significant bit, b7, is sent first.

### Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful byte transfer. The bus transmitter, whether it be master or slave, releases the SDA bus after sending eight bits of data. During the 9<sup>th</sup> clock pulse period, the receiver pulls the SDA bus low to acknowledge the receipt of the eight data bits.

### Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

### Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends the 8-bit byte, shown in Table 3, on the SDA bus line (most significant bit first). This consists of the 7-bit Device Select Code, and the 1-bit Read/Write Designator (R $\bar{W}$ ). The Device Select Code is further subdivided into: a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (0, E1, E0).

To address the memory array, the 4-bit Device Type Identifier is 1010b.

Up to four memory devices can be connected on a single I<sup>2</sup>C bus. Each one is given a unique 2-bit code on its Chip Enable inputs. When the Device Select Code is received on the SDA bus, the memory only responds if the Chip Select Code is the same as the pattern applied to its Chip Enable pins.

**Table 4. Most Significant Byte**

b15	b14	b13	b12	b11	b10	b9	b8
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Note: 1. b15 is treated as Don't Care on the M24256-A series.

**Table 5. Least Significant Byte**

b7	b6	b5	b4	b3	b2	b1	b0
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The 8<sup>th</sup> bit is the R $\bar{W}$  bit. This is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9<sup>th</sup> bit time. If the memory does not match the Device Select Code, it deselects itself from the bus, and goes into stand-by mode.

There are two modes both for read and write. These are summarized in Table 6 and described later. A communication between the master and the slave is ended with a STOP condition.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 4) is sent first, followed by the Least significant Byte (Table 5). Bits b15 to b0 form the address of the byte in memory. Bit b15 is treated as Don't Care bits on the M24256-A memory.

### Write Operations

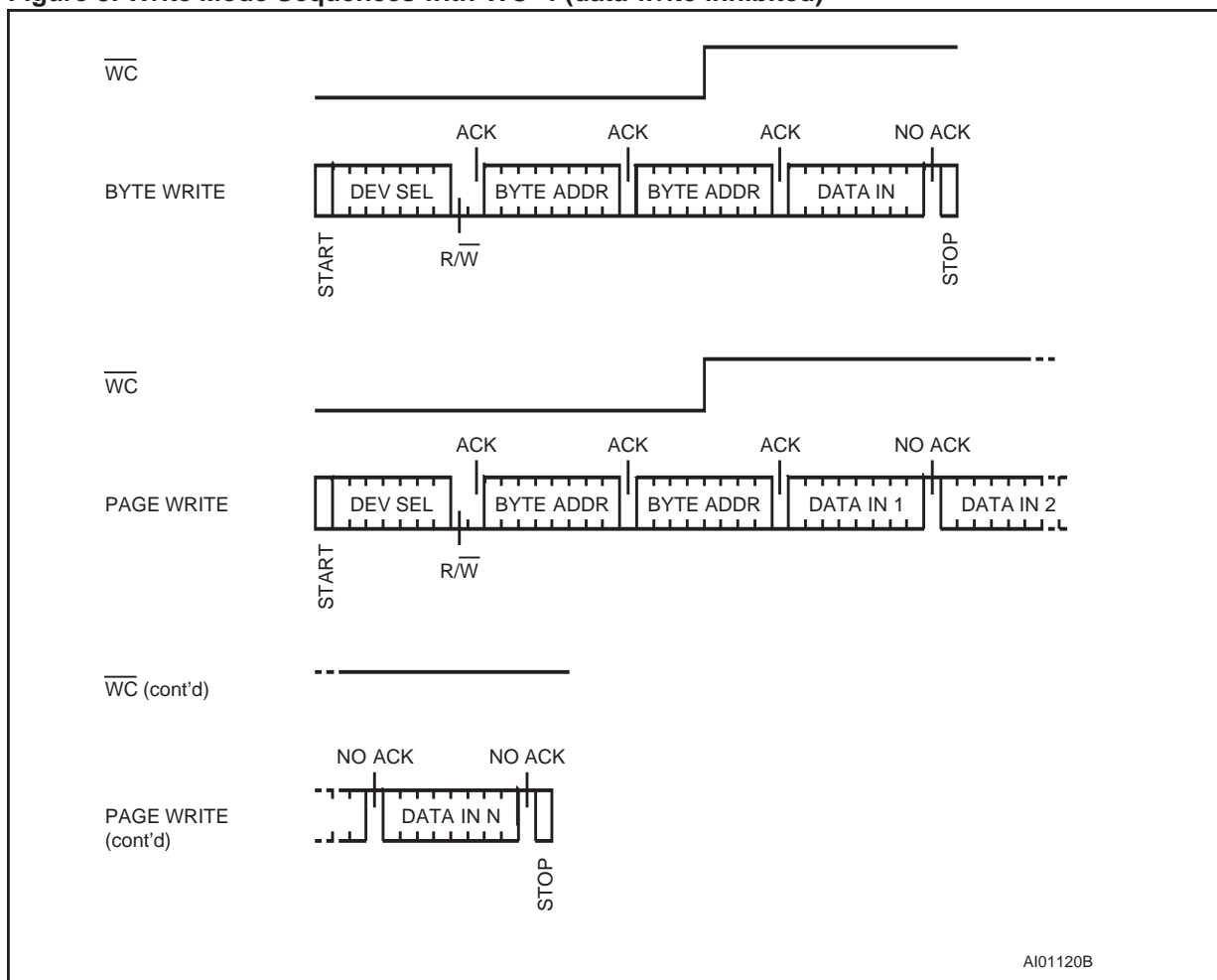
Following a START condition the master sends a Device Select Code with the R $\bar{W}$  bit set to '0', as shown in Table 6. The memory acknowledges this, and waits for two address bytes. The memory re-

**Table 6. Operating Modes**

Mode	R $\bar{W}$ bit	WC <sup>1</sup>	Data Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, R $\bar{W}$ = 1
Random Address Read	0	X	1	START, Device Select, R $\bar{W}$ = 0, Address
	1	X		reSTART, Device Select, R $\bar{W}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V <sub>IL</sub>	1	START, Device Select, R $\bar{W}$ = 0
Page Write	0	V <sub>IL</sub>	≤ 64	START, Device Select, R $\bar{W}$ = 0

Note: 1. X = V<sub>IH</sub> or V<sub>IL</sub>.

Figure 5. Write Mode Sequences with  $\overline{WC}=1$  (data write inhibited)



AI01120B

sponds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if the  $\overline{WC}$  input pin is taken high. Any write command with  $\overline{WC}=1$  (during a period of time from the START condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes will *not* be acknowledged, as shown in Figure 5.

**Byte Write**

In the Byte Write mode, after the Device Select Code and the address bytes, the master sends one data byte. If the addressed location is write protected by the  $\overline{WC}$  pin, the memory replies with a NoAck, and the location is not modified. If, instead, the  $\overline{WC}$  pin has been held at 0, as shown in Figure 6, the memory replies with an Ack. The master terminates the transfer by generating a STOP condition.

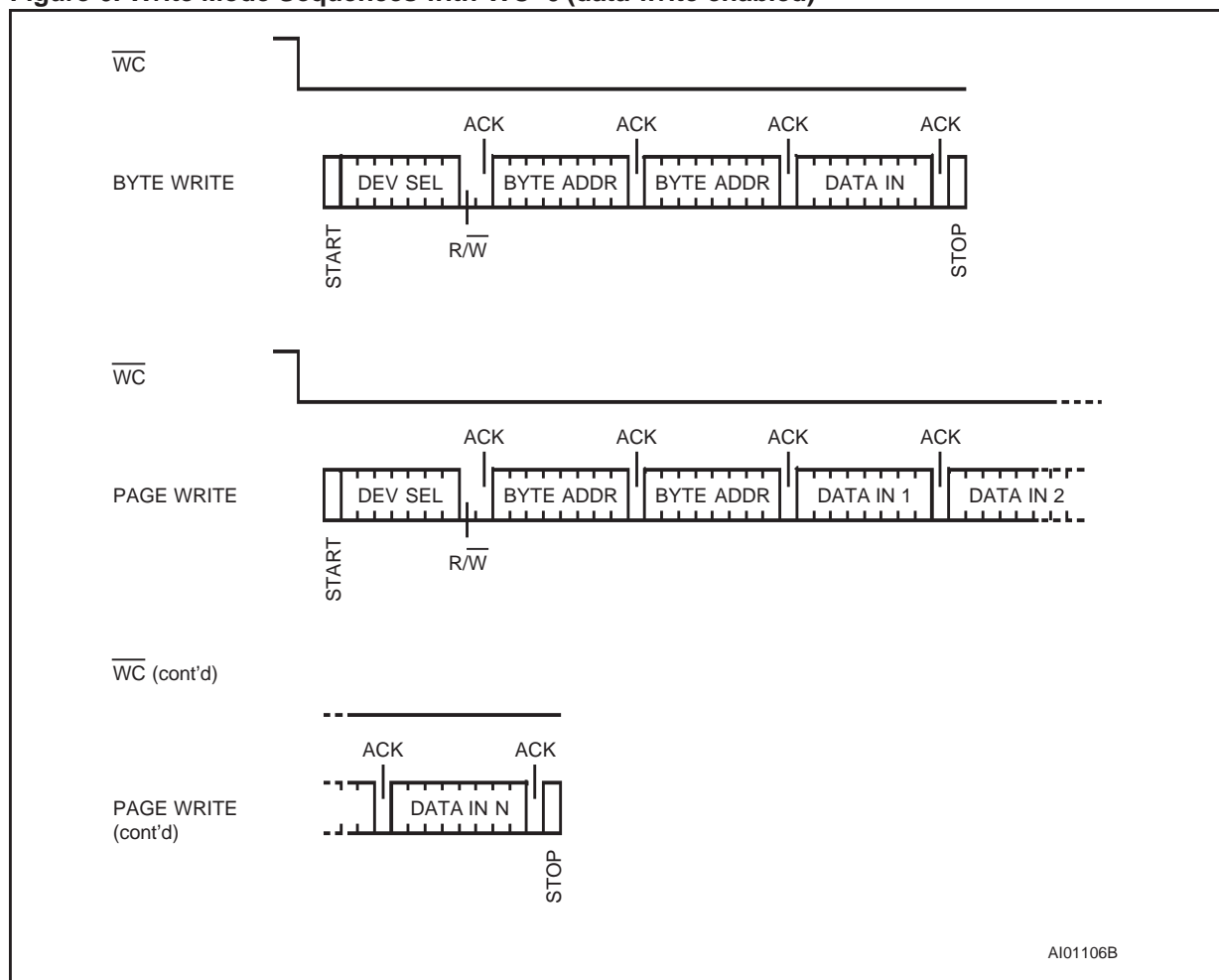
**Page Write**

The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b14-b6 for the M24256-A) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The master sends from one up to 64 bytes of data, each of which is acknowledged by the memory if the  $\overline{WC}$  pin is low. If the  $\overline{WC}$  pin is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 6 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

When the master generates a STOP condition immediately after the Ack bit (in the "10<sup>th</sup> bit" time

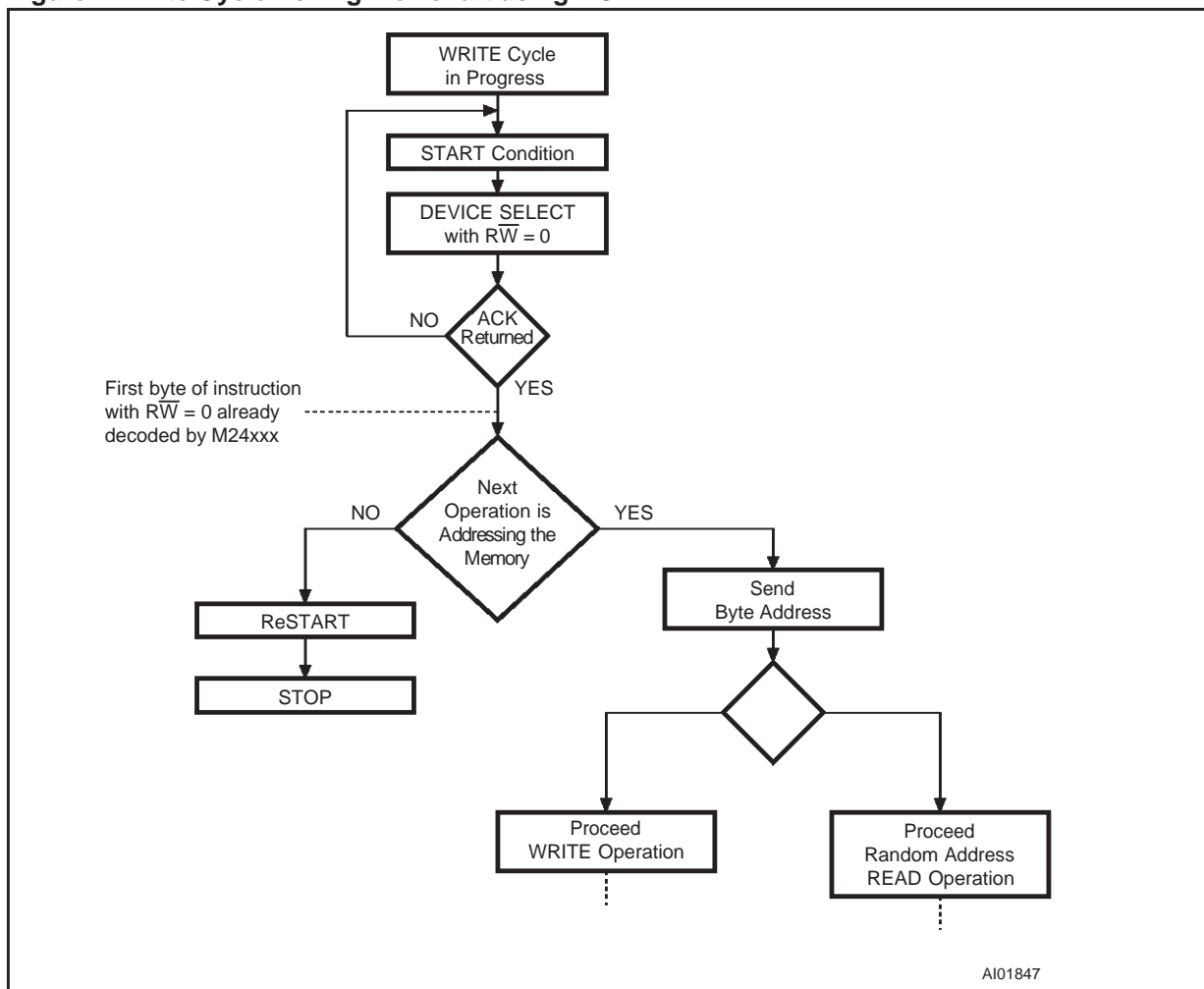


Figure 6. Write Mode Sequences with  $\overline{WC}=0$  (data write enabled)

slot), either at the end of a byte write or a page write, the internal memory write cycle is triggered. A STOP condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA input is disabled internally, and the device does not respond to any requests.

Figure 7. Write Cycle Polling Flowchart using ACK



### Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time ( $t_w$ ) is shown in Table 9, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the master.

The sequence, as shown in Figure 7, is:

- Initial condition: a Write is in progress.
- Step 1: the master issues a START condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no Ack will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

### Read Operations

Read operations are performed independently of the state of the  $\overline{WC}$  pin.

#### Random Address Read

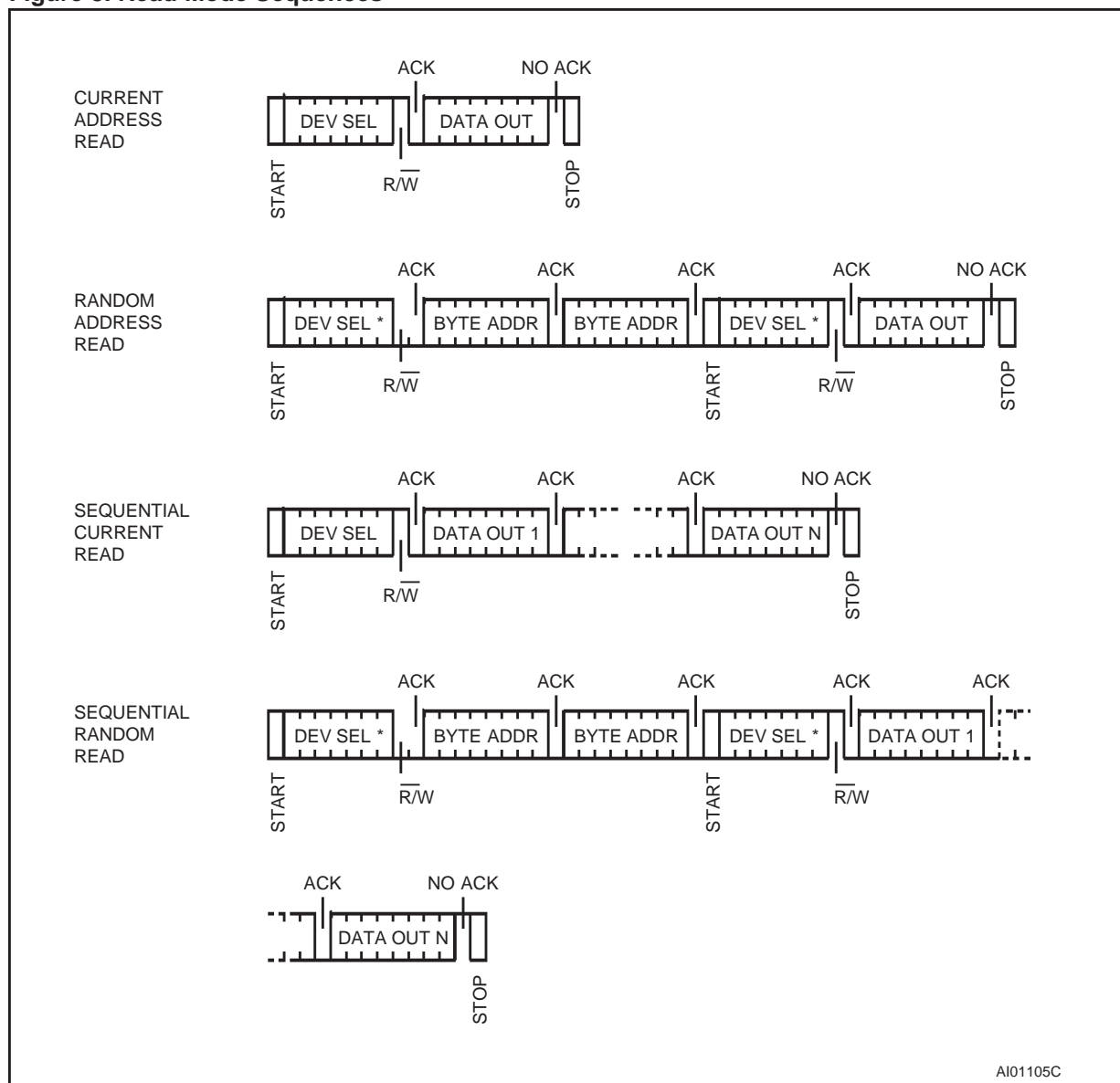
A dummy write is performed to load the address into the address counter, as shown in Figure 8. Then, *without* sending a STOP condition, the master sends another START condition, and repeats the Device Select Code, with the  $\overline{RW}$  bit set to '1'. The memory acknowledges this, and outputs the contents of the addressed byte. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

#### Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read mode, following a START condition, the master sends a Device Select Code with the  $\overline{RW}$  bit set to '1'. The memory acknowledges this, and outputs the byte addressed by the



Figure 8. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1<sup>st</sup> and 4<sup>th</sup> bytes) must be identical.

internal address counter. The counter is then incremented. The master terminates the transfer with a STOP condition, as shown in Figure 8, *without* acknowledging the byte output.

### Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. The master *does* acknowledge the data byte output in this case, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over' and the memory continues to output data from memory address 00h.

### Acknowledge in Read Mode

In all read modes, the memory waits, after each byte read, for an acknowledgment during the 9<sup>th</sup> bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its stand-by state.

**Table 7. DC Characteristics**

( $T_A = -40$  to  $85$  °C;  $V_{CC} = 4.5$  to  $5.5$  V or  $2.5$  to  $5.5$  V)

( $T_A = -20$  to  $85$  °C;  $V_{CC} = 1.8$  to  $3.6$  V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$I_{LI}$	Input Leakage Current (SCL, SDA)	$0\text{ V} \leq V_{IN} \leq V_{CC}$		$\pm 2$	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$0\text{ V} \leq V_{OUT} \leq V_{CC}$ , SDA in Hi-Z		$\pm 2$	$\mu\text{A}$
$I_{CC}$	Supply Current	-W series: $V_{CC}=5\text{V}$ , $f_c=400\text{kHz}$ (rise/fall time < 30ns)		2	mA
		-W series: $V_{CC}=2.5\text{V}$ , $f_c=400\text{kHz}$ (rise/fall time < 30ns)		1	mA
		-R series: $V_{CC}=1.8\text{V}$ , $f_c=100\text{kHz}$ (rise/fall time < 30ns)		$0.5^1$	mA
$I_{CC1}$	Supply Current (Stand-by)	-W series: $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 5\text{ V}$		10	$\mu\text{A}$
		-W series: $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 2.5\text{ V}$		2	$\mu\text{A}$
		-R series: $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 1.8\text{ V}$		$1^1$	$\mu\text{A}$
$V_{IL}$	Input Low Voltage (SCL, SDA)		-0.3	$0.3V_{CC}$	V
$V_{IH}$	Input High Voltage (SCL, SDA)		$0.7V_{CC}$	$V_{CC}+1$	V
$V_{IL}$	Input Low Voltage (E0, E1, $\overline{WC}$ )		-0.3	0.5	V
$V_{IH}$	Input High Voltage (E0, E1, $\overline{WC}$ )		$0.7V_{CC}$	$V_{CC}+1$	V
$V_{OL}$	Output Low Voltage	-W series: $I_{OL} = 3\text{ mA}$ , $V_{CC} = 5\text{ V}$		0.4	V
		-W series: $I_{OL} = 2.1\text{ mA}$ , $V_{CC} = 2.5\text{ V}$		0.4	V
		-R series: $I_{OL} = 0.7\text{ mA}$ , $V_{CC} = 1.8\text{ V}$		$0.2^1$	V

Note: 1. This is preliminary data.

**Table 8. Input Parameters<sup>1</sup>** ( $T_A = 25$  °C,  $f = 400$  kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$C_{IN}$	Input Capacitance (SDA)			8	pF
$C_{IN}$	Input Capacitance (other pins)			6	pF
$Z_L$	Input Impedance (E1, E0, $\overline{WC}$ )	$V_{IN} \leq 0.5\text{ V}$	50		k $\Omega$
$Z_H$	Input Impedance (E1, E0, $\overline{WC}$ )	$V_{IN} \geq 0.7V_{CC}$	500		k $\Omega$
$t_{NS}$	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. Sampled only, not 100% tested.

Table 9. AC Characteristics

Symbol	Alt.	Parameter	M24256-A						Unit
			V <sub>CC</sub> =4.5 to 5.5 V T <sub>A</sub> =-40 to 85°C		V <sub>CC</sub> =2.5 to 5.5 V T <sub>A</sub> =-40 to 85°C		V <sub>CC</sub> =1.8 to 3.6 V T <sub>A</sub> =-20 to 85°C <sup>4</sup>		
			Min	Max	Min	Max	Min	Max	
t <sub>CH1CH2</sub>	t <sub>R</sub>	Clock Rise Time		300		300		1000	ns
t <sub>CL1CL2</sub>	t <sub>F</sub>	Clock Fall Time		300		300		300	ns
t <sub>DH1DH2</sub> <sup>2</sup>	t <sub>R</sub>	SDA Rise Time	20	300	20	300	20	1000	ns
t <sub>DL1DL2</sub> <sup>2</sup>	t <sub>F</sub>	SDA Fall Time	20	300	20	300	20	300	ns
t <sub>CHDX</sub> <sup>1</sup>	t <sub>SU:STA</sub>	Clock High to Input Transition	600		600		4700		ns
t <sub>CHCL</sub>	t <sub>HIGH</sub>	Clock Pulse Width High	600		600		4000		ns
t <sub>DLCL</sub>	t <sub>HD:STA</sub>	Input Low to Clock Low (START)	600		600		4000		ns
t <sub>CLDX</sub>	t <sub>HD:DAT</sub>	Clock Low to Input Transition	0		0		0		μs
t <sub>CLCH</sub>	t <sub>LOW</sub>	Clock Pulse Width Low	1.3		1.3		4.7		μs
t <sub>DXCX</sub>	t <sub>SU:DAT</sub>	Input Transition to Clock Transition	100		100		250		ns
t <sub>CHDH</sub>	t <sub>SU:STO</sub>	Clock High to Input High (STOP)	600		600		4000		ns
t <sub>DHDL</sub>	t <sub>BUF</sub>	Input High to Input Low (Bus Free)	1.3		1.3		4.7		μs
t <sub>CLQV</sub> <sup>3</sup>	t <sub>AA</sub>	Clock Low to Data Out Valid	200	900	200	900	200	3500	ns
t <sub>CLQX</sub>	t <sub>DH</sub>	Data Out Hold Time After Clock Low	200		200		200		ns
f <sub>c</sub>	f <sub>SCL</sub>	Clock Frequency		400		400		100	kHz
t <sub>w</sub>	t <sub>WR</sub>	Write Time		10		10		10	ms

Note: 1. For a reSTART condition, or following a write cycle.

2. Sampled only, not 100% tested.

3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

4. This is preliminary data.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	0.2V <sub>CC</sub> to 0.8V <sub>CC</sub>
Input and Output Timing Reference Voltages	0.3V <sub>CC</sub> to 0.7V <sub>CC</sub>

Figure 9. AC Testing Input Output Waveforms

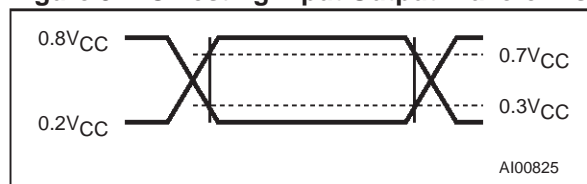
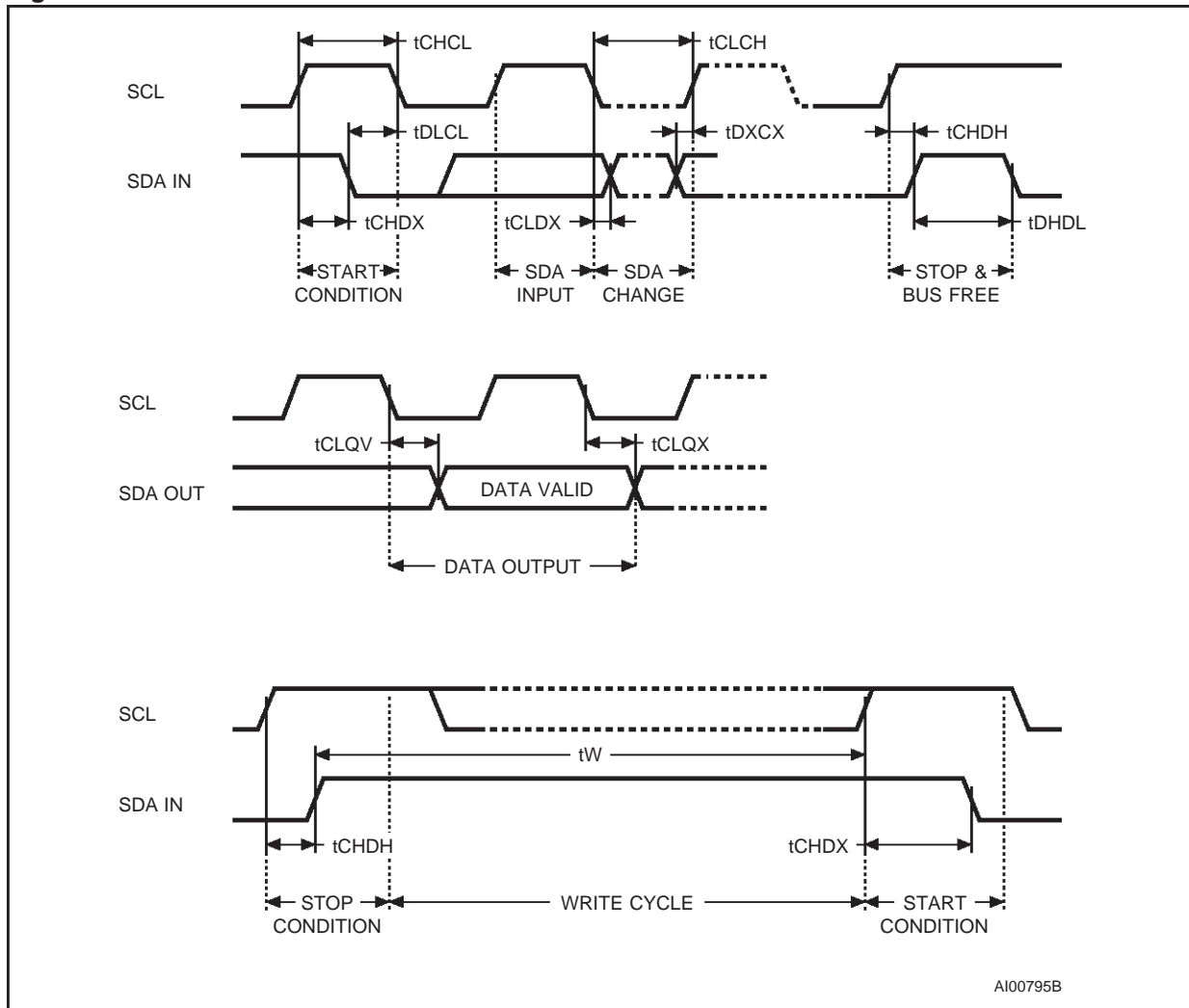


Figure 10. AC Waveforms



**Table 11. Ordering Information Scheme**

Example: M24256 – A W MN 6 T

Memory Capacity	Option	Temperature Range	Package
256 256 Kbit (32K x 8)	T Tape and Reel Packing	6 –40 °C to 85 °C 5 –20 °C to 85 °C	BN PSDIP8 (0.25 mm frame) MN SO8 (150 mil width) MW SO8 (200 mil width) DL TSSOP14 (169 mil width) EA SBGA7 <sup>1</sup>
Operating Voltage			
blank 4.5 V to 5.5 V W 2.5 V to 5.5 V R 1.8 V to 3.6 V			

Note: 1. SBGA7 package available only for the "M24256-A W EA 6 T"

### ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all 1s (FFh).

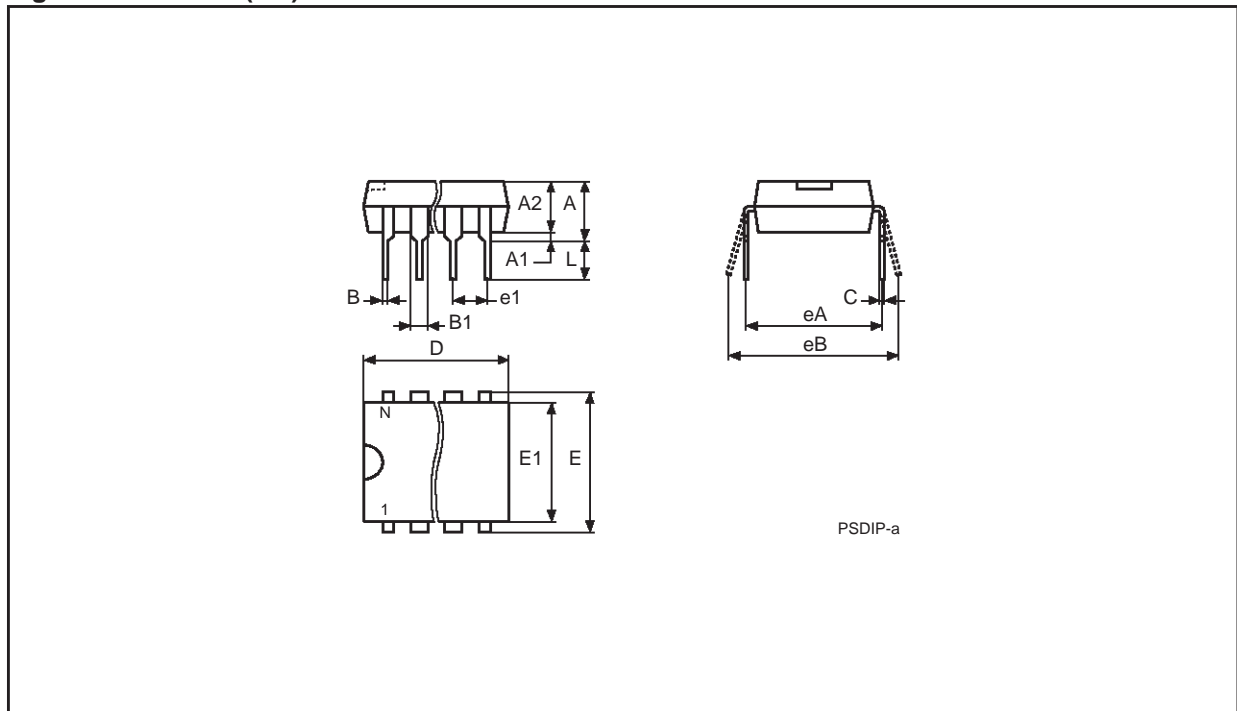
The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

**M24256-A**

**Table 12. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame**

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	

**Figure 11. PSDIP8 (BN)**

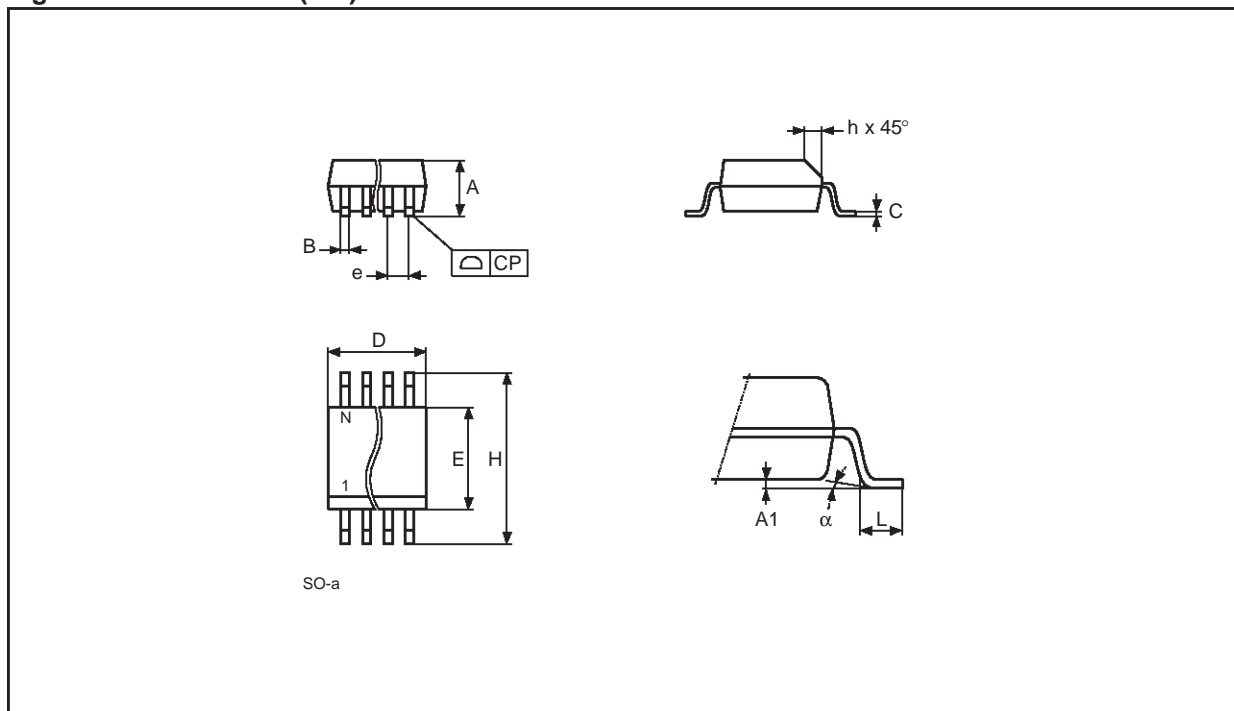


Note: 1. Drawing is not to scale.

Table 13. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
$\alpha$		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

Figure 12. SO8 narrow (MN)

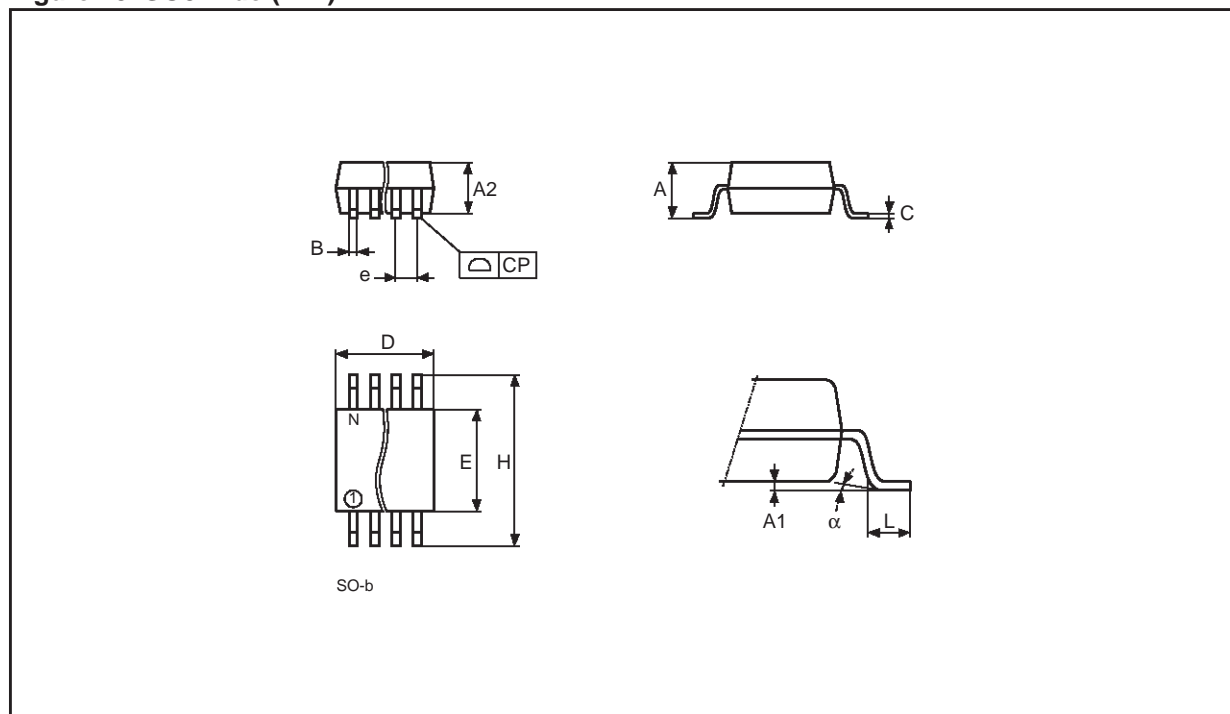


Note: 1. Drawing is not to scale.

Table 14. SO8 - 8 lead Plastic Small Outline, 200 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
$\alpha$		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

Figure 13. SO8 wide (MW)



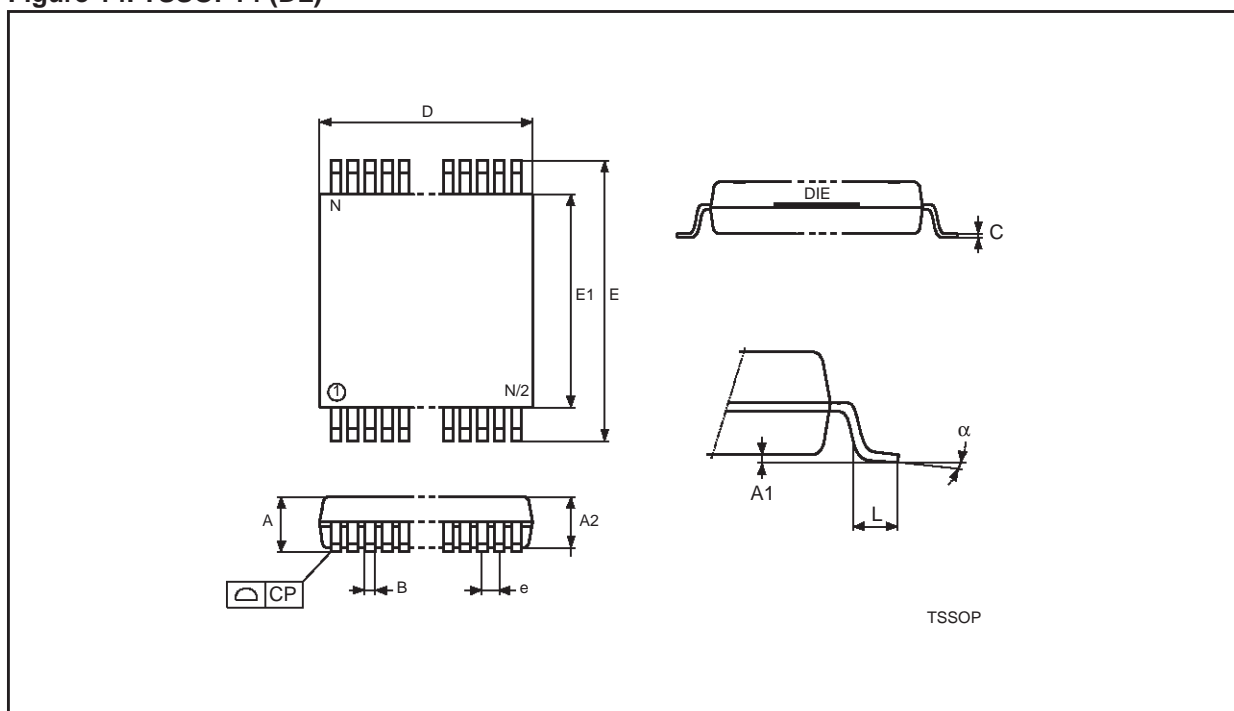
Note: 1. Drawing is not to scale.



Table 15. TSSOP14 - 14 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
$\alpha$		0°	8°		0°	8°
N	14			14		
CP			0.08			0.003

Figure 14. TSSOP14 (DL)



Note: 1. Drawing is not to scale.

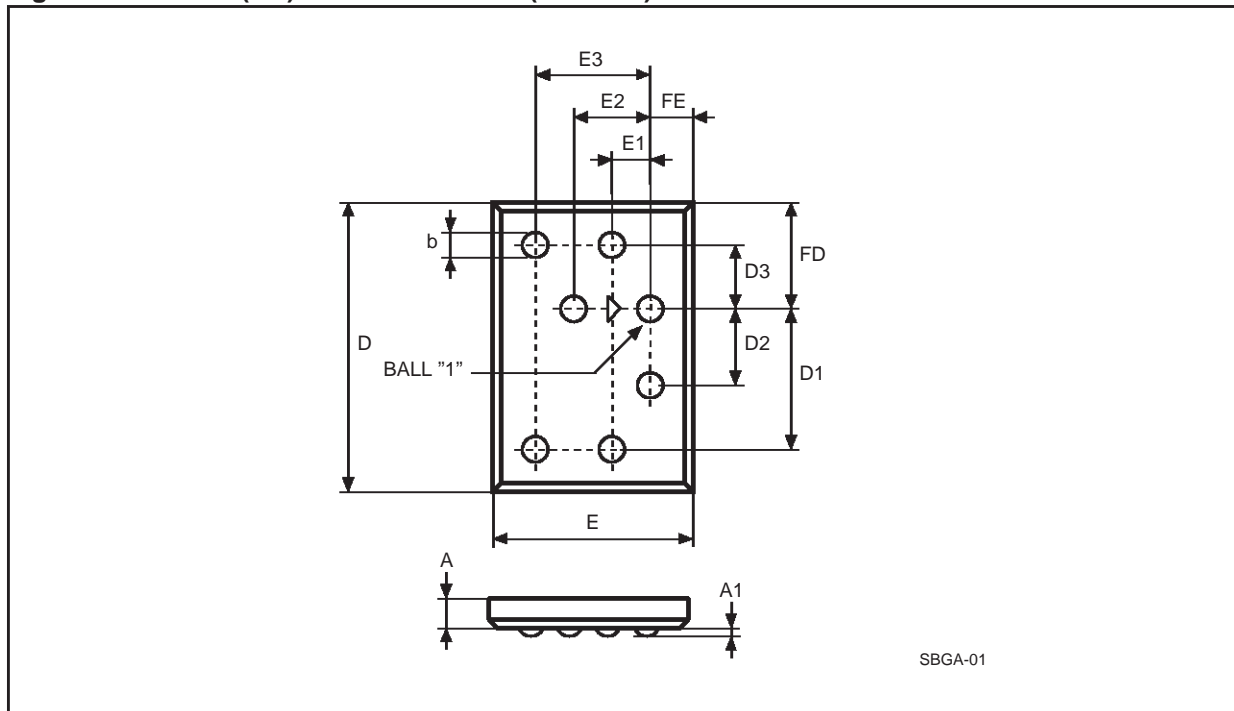
**M24256-A**

**Table 16. SBGA7 - 7 ball Shell Ball Grid Array**

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.430	0.380	0.480	0.017	0.015	0.019
A1	0.180	0.150	0.210	0.007	0.006	0.008
b	0.350	0.320	0.380	0.014	0.013	0.015
D	3.555	3.525	3.585	0.140	0.138	0.142
D2 <sup>1</sup>	1.000	0.970	1.030	0.039	0.038	0.041
E	2.275	2.245	2.305	0.090	0.088	0.091
FD	1.278	—	—	0.050	—	—
FE	0.388	—	—	0.015	—	—
N	7			7		

Note: 1. No ball is closer than D2 to any other ball, thus giving an arrangement of equilateral triangles in which:  
 $E1 = D2/2$  ;  $E2 = D2$  ;  $E3 = 3 \times D2/2$   
 $D3 = \sqrt{3} \times D2/2$  ;  $D1 = D2 + \sqrt{3} \times D2/2$

**Figure 15. SBGA7 (EA) – Underside view (ball side)**



Note: 1. Drawing is not to scale.

**Table 17. Revision History**

<b>Date</b>	<b>Description of Revision</b>
17-Apr-2000	SBGA7(EA) package added on pp 1, 2, OrderInfo, PackageData E1 and E0 are specified as having to be tied either to V <sub>CC</sub> or V <sub>SS</sub>

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