

8 BIT ADDRESSABLE LATCH

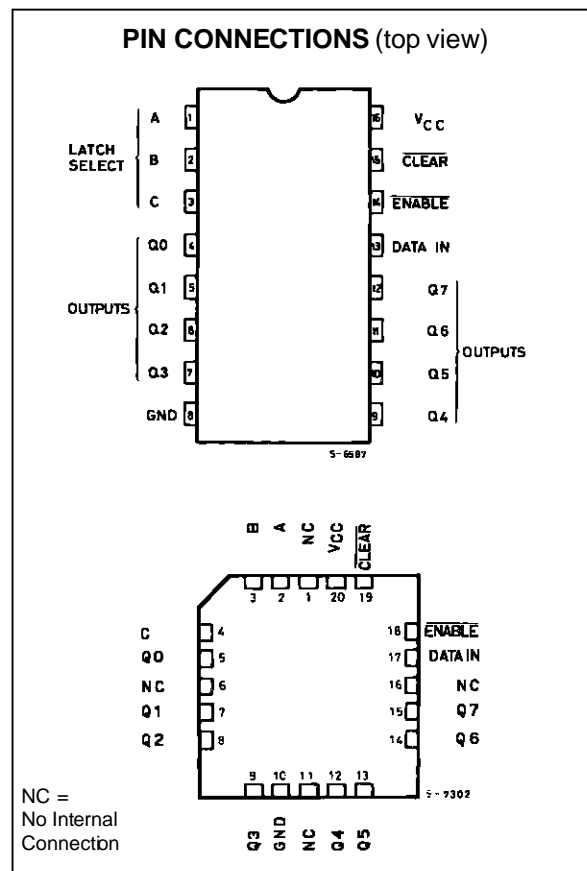
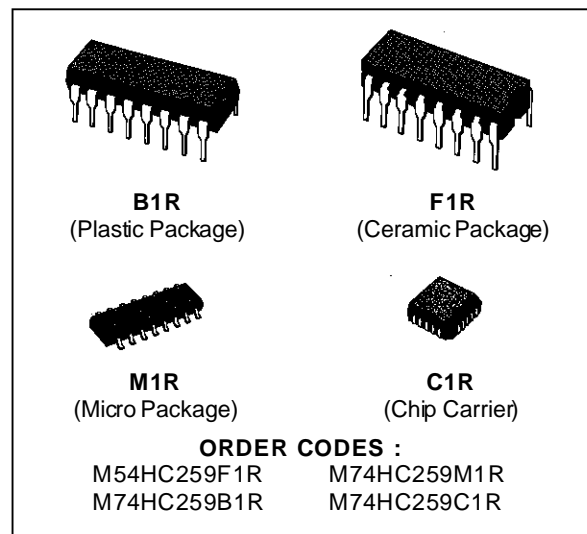
- HIGH SPEED  
 $t_{PD} = 15 \text{ ns (TYP.) at } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY  
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY  
 10 LSTTL LOADS
- SYMMETRICAL PROPAGATION DELAYS  
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PRORAGATION DELAYS  
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE  
 $V_{CC} \text{ (OPR)} = 2 \text{ V to } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE WITH  
 54/74LS259

**DESCRIPTION**

The M54/74HC259 is a high speed CMOS 8 BIT ADDRESSABLE LATCH fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54HC259/M74HC259 has single data input (D) 8 latch outputs (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addresses output. The data is stored on the positive-going edge of the ENABLE pulse. All unaddressed latches will remain unaffected. With ENABLE in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the ENABLE should be held high (inactive) while the address lines are changing. If ENABLE is held high and CLEAR is taken low all eight latches are cleared to the low state. If ENABLE is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to 8 line decoder.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.



# M54/M74HC259

## TRUTH TABLE

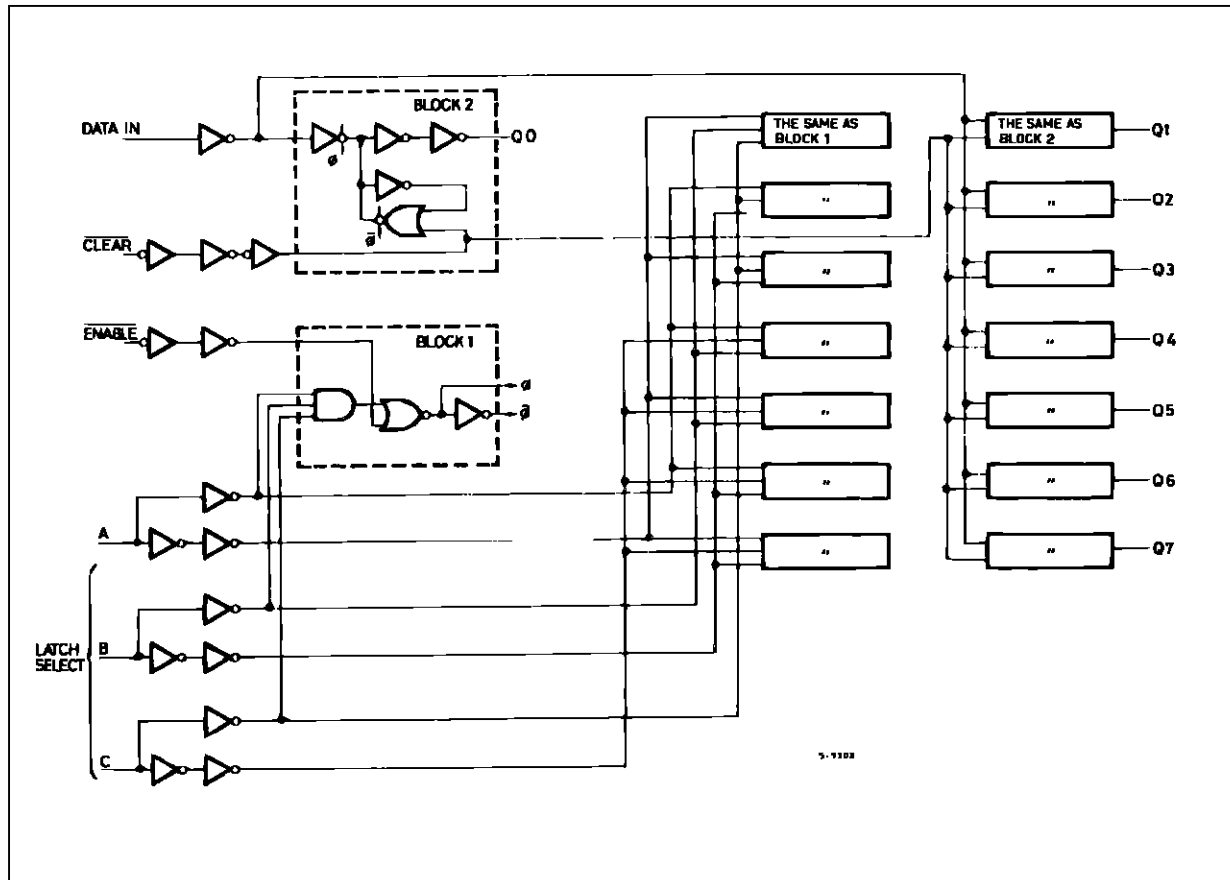
INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	ENABLE			
H	L	D	Q <sub>i0</sub>	ADDRESSABLE LATCH
H	H	Q <sub>i0</sub>	Q <sub>i0</sub>	MEMORY
L	L	D	L	8 LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO 'L'

D: The level at the data input

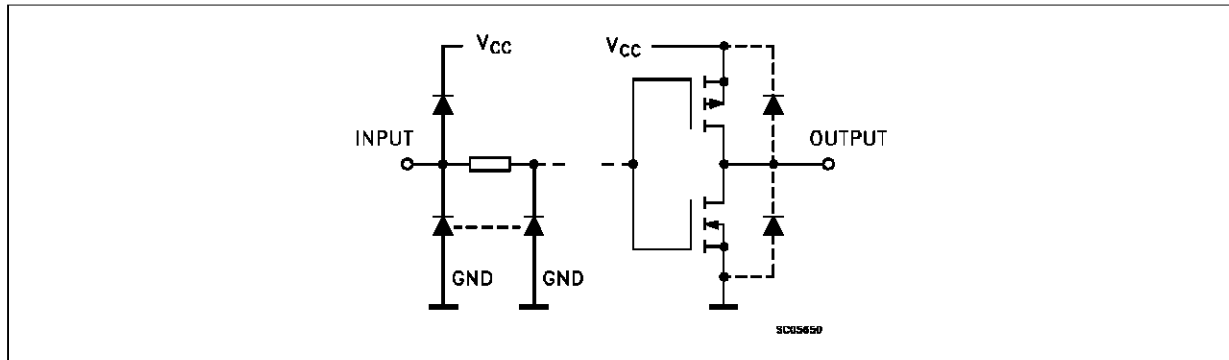
Q<sub>i0</sub>: The level before the indicated steady state input conditions were established, (i = 0, 1, ...,7).

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

## LOGIC DIAGRAM



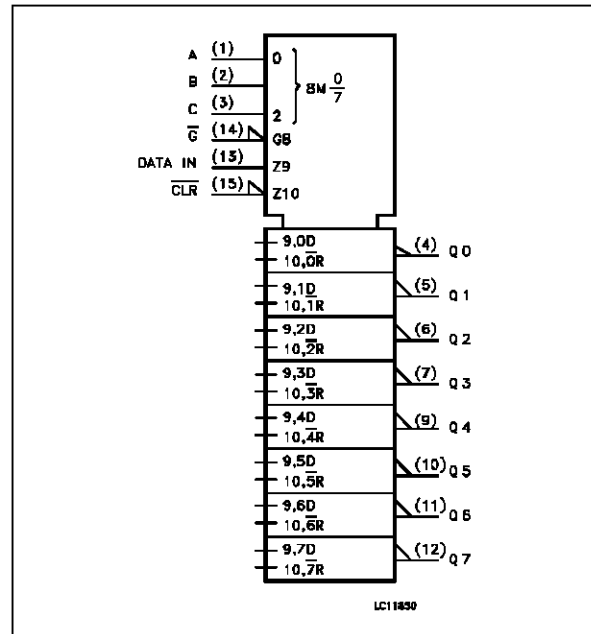
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5, 6, 7, 9, 10, 11, 12	Q0 to Q7	Latch Outputs
13	D	Data Input
14	ENABLE	Latch Enable Input (Active LOW)
15	CLEAR	Conditional Reset Input (Active LOW)
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Source Sink Current Per Output Pin	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW: ± 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

## M54/M74HC259

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature: <b>M54HC Series</b> <b>M74HC Series</b>	-55 to +125 -40 to +85	°C °C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2\text{ V}$	0 to 1000	ns
		$V_{CC} = 4.5\text{ V}$	0 to 500	
		$V_{CC} = 6\text{ V}$	0 to 400	

### DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value						Unit								
				$T_A = 25\text{ °C}$ 54HC and 74HC			$-40\text{ to }85\text{ °C}$ 74HC		$-55\text{ to }125\text{ °C}$ 54HC									
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.							
$V_{IH}$	High Level Input Voltage	$V_{CC}$ (V)								V								
											2.0	1.5			1.5		1.5	
											4.5	3.15			3.15		3.15	
$V_{IL}$	Low Level Input Voltage	$V_{CC}$ (V)								V								
											2.0		0.5		0.5		0.5	
											4.5		1.35		1.35		1.35	
$V_{OH}$	High Level Output Voltage	$V_{CC}$ (V)	$V_I = V_{IH}$ or $V_{IL}$	$I_O = -20\text{ }\mu\text{A}$						V								
											2.0	1.9	2.0		1.9		1.9	
											4.5	4.4	4.5		4.4		4.4	
$V_{OL}$	Low Level Output Voltage	$V_{CC}$ (V)	$V_I = V_{IH}$ or $V_{IL}$	$I_O = 20\text{ }\mu\text{A}$						V								
											2.0		0.0	0.1		0.1		0.1
											4.5		0.0	0.1		0.1		0.1
$I_I$	Input Leakage Current	$V_{CC}$ (V)	$V_I = V_{CC}$ or GND							$\mu\text{A}$								
											2.0			$\pm 0.1$		$\pm 1$		$\pm 1$
											4.5							
$I_{CC}$	Quiescent Supply Current	$V_{CC}$ (V)	$V_I = V_{CC}$ or GND							$\mu\text{A}$								
											2.0			4		40		80
											4.5							

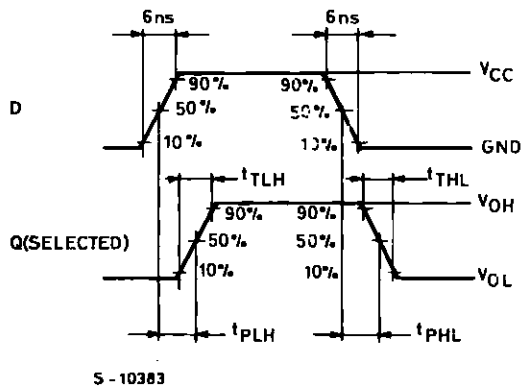
AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	Test Conditions		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (DATA - Q)	2.0			56	140		175		210	ns
		4.5			18	28		35		42	
		6.0			15	24		30		36	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (A, B, C - Q)	2.0			76	190		240		285	ns
		4.5			24	38		48		57	
		6.0			20	32		41		48	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (G - Q)	2.0			57	150		190		225	ns
		4.5			19	30		38		45	
		6.0			16	26		32		38	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLEAR - Q)	2.0			45	115		145		175	ns
		4.5			15	23		29		35	
		6.0			13	20		25		30	
t <sub>w(L)</sub>	Minimum Pulse Width (ENABLE)	2.0			28	75		90		115	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t <sub>w(L)</sub>	Minimum Pulse Width (CLEAR)	2.0			24	75		90		115	ns
		4.5			6	15		19		23	
		6.0			5	13		16		20	
t <sub>s</sub>	Minimum Set-up Time (DATA)	2.0			12	50		60		75	ns
		4.5			3	10		12		15	
		6.0			3	9		11		13	
t <sub>s</sub>	Minimum Set-up Time (A, B, C)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
t <sub>h</sub>	Minimum Hold Time (DATA)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
t <sub>h</sub>	Minimum Hold Time (A, B, C)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C <sub>IN</sub>	Input Capacitance				5	10		10		10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance				66						pF

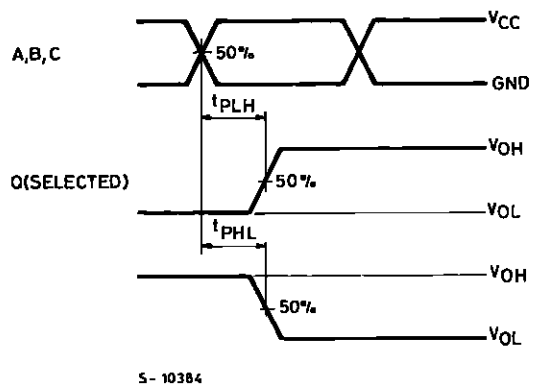
(\*) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

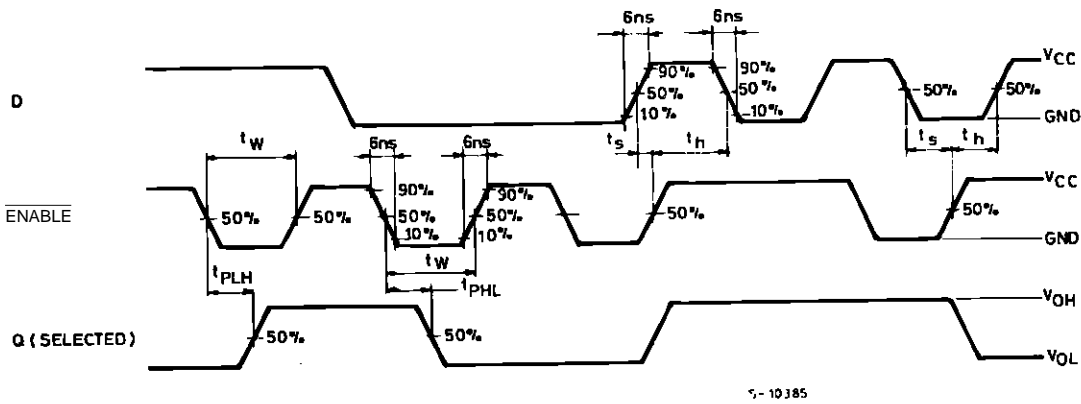
WAVEFORM 1. ( $\overline{\text{ENABLE}} = \text{L}$ ,  $\overline{\text{CLR}} = \text{H}$ , A ~ C =



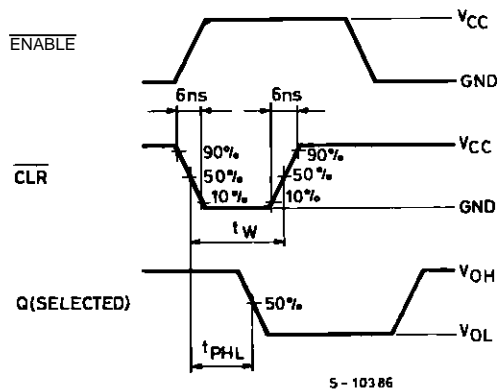
WAVEFORM 2. ( $\overline{\text{G}} = \text{L}$ )



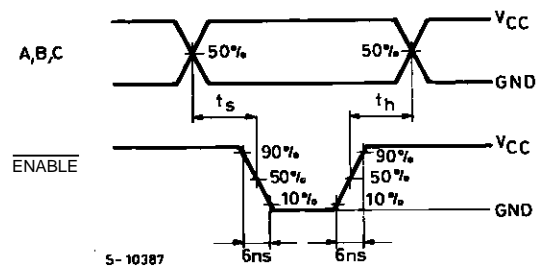
WAVEFORM 3. ( $\overline{\text{CLR}} = \text{H}$ , A ~ C = Stable)



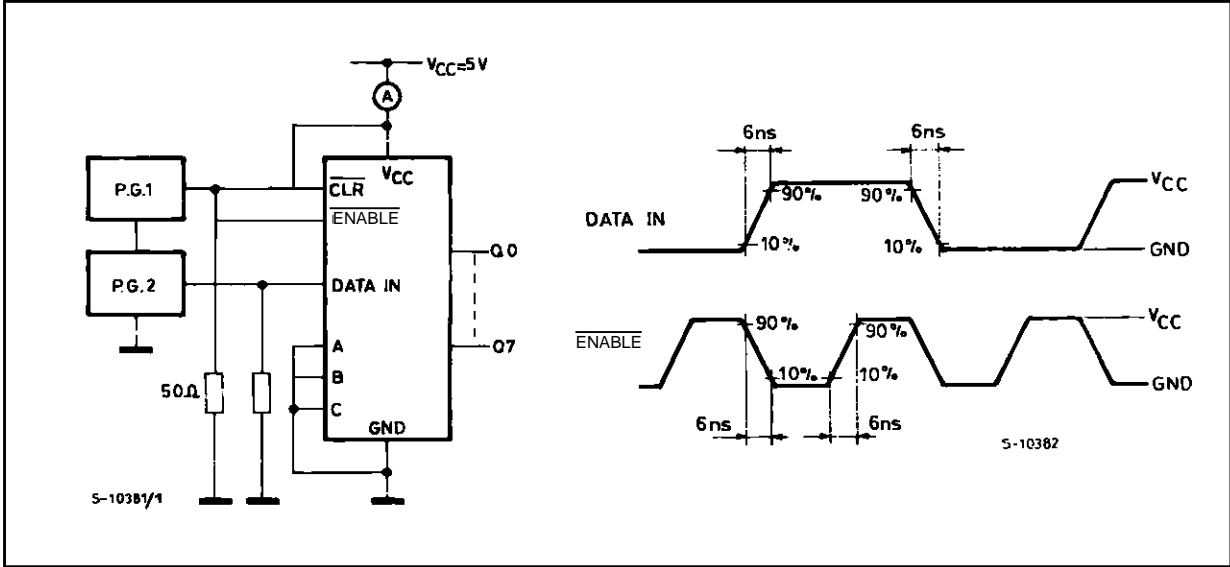
WAVEFORM 4. (D = H, A ~ C = Stable)



WAVEFORM 5. ( $\overline{\text{CLR}} = \text{H}$ )

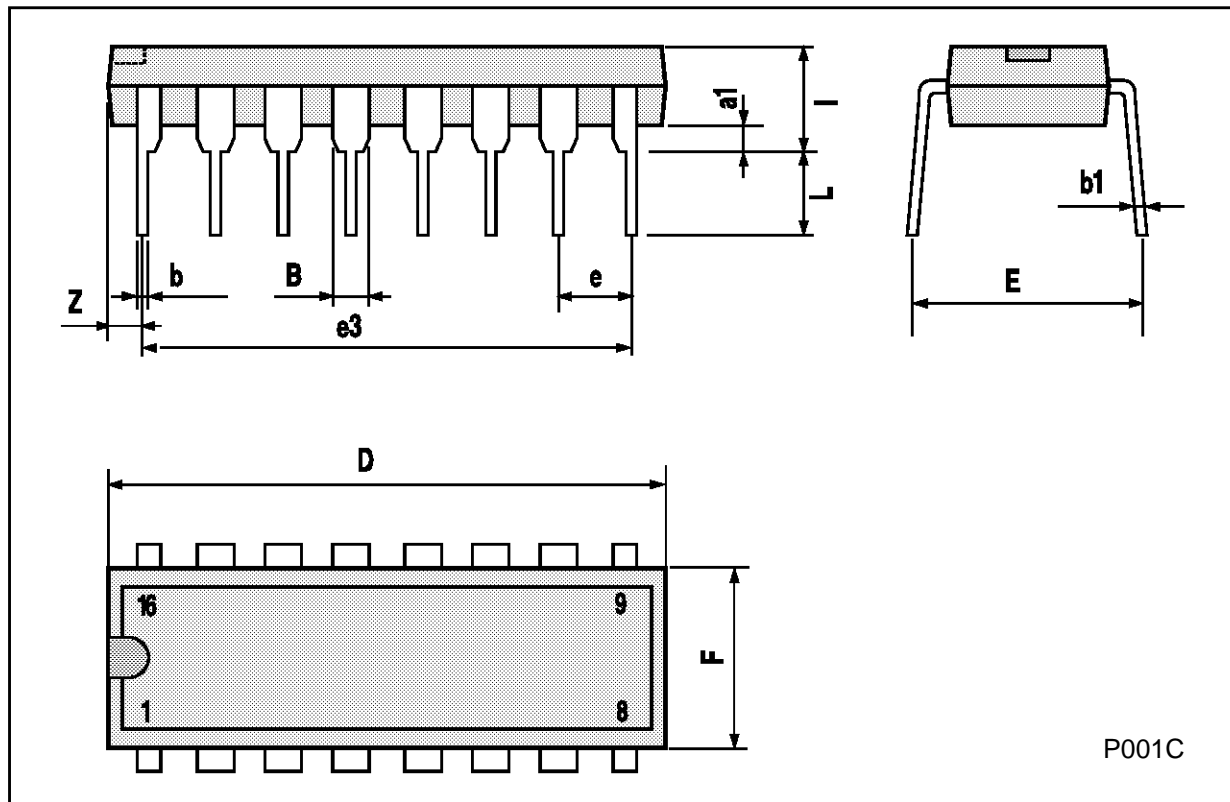


TEST CIRCUIT I<sub>CC</sub> (Opr.)



Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C



## Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

## PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



P027A

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