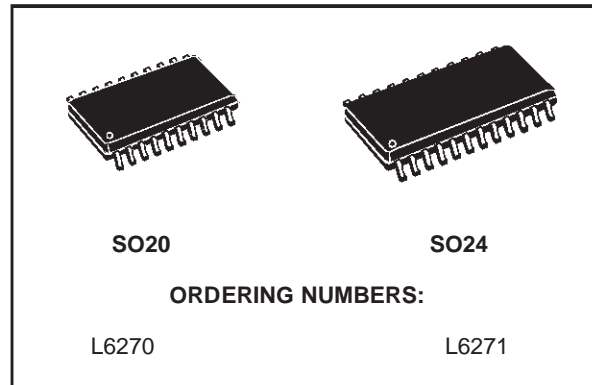


## MILLI-ACTUATOR DRIVER

PRODUCT PREVIEW

- 90V BCD MIXED TECHNOLOGY
- SO24 AND SO20 PLASTIC SMD PACKAGE
- 4.5 TO 13.2V OPERATIVE VOLTAGE
- $\pm 25$  TO  $\pm 40$ V OUTPUT VOLTAGE RANGE SELECTABLE BY EXTERNAL RESISTOR
- FULL-WAVE RESONANT DC-DC CONVERTER USING SINGLE COIL FOR DUAL HIGH VOLTAGE GENERATOR WITH OUTPUT SLEW RATE CONTROL AND SELF CURRENT LIMITING
- LINEAR MODE AND BANG-BANG MODE
- $\pm 40$ V OR  $0/+80$ V OPERATIVE VOLTAGE
- DRIVING CONFIGURATION MODES:
  1. SINGLE ENDED VOLTAGE MODE
  2. DIFFERENTIAL VOLTAGE MODE
  3. SINGLE ENDED CHARGE MODE
- DOUBLE OPERATIONAL AMPLIFIERS WITH 500KHZ GAIN BANDWIDTH PRODUCT AND LOAD DRIVING CAPABILITY FROM 0.4NF UP TO 24NF

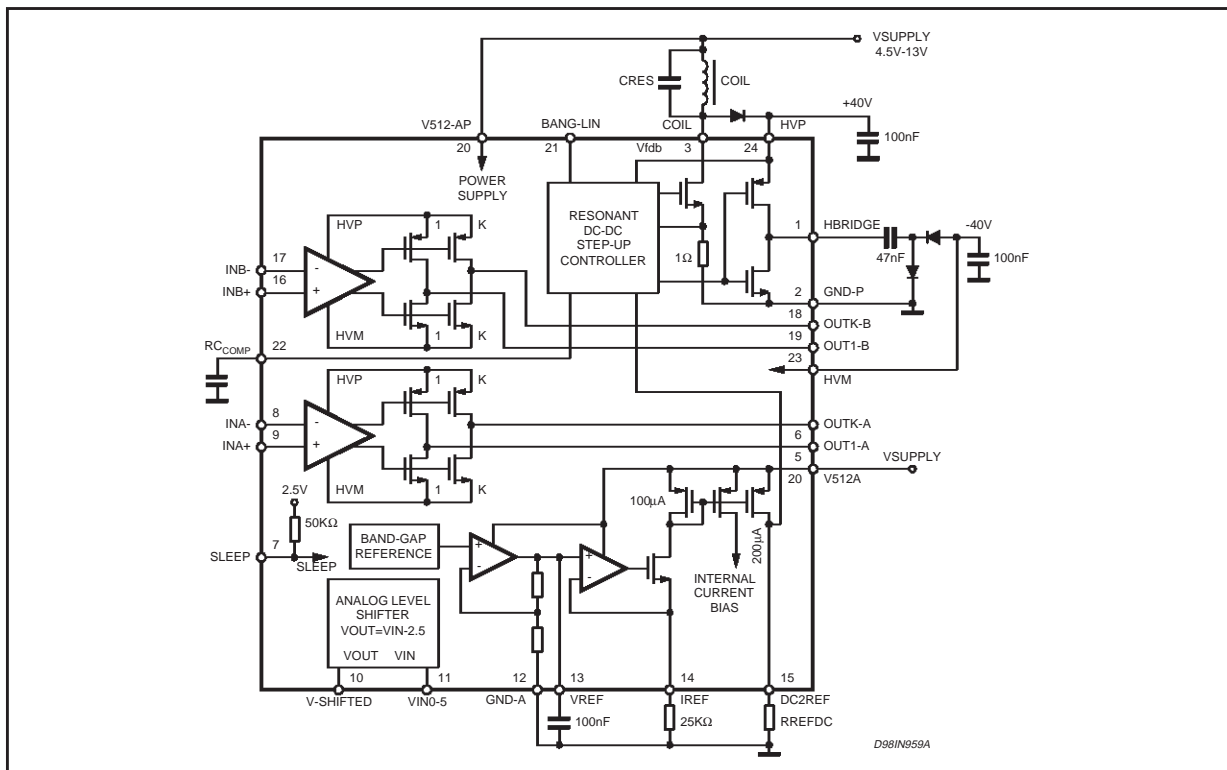


- 2.5V VOLTAGE REFERENCE
- 2.5V ANALOG SHIFTING CIRCUITRY
- POWER SAVING SLEEP MODE

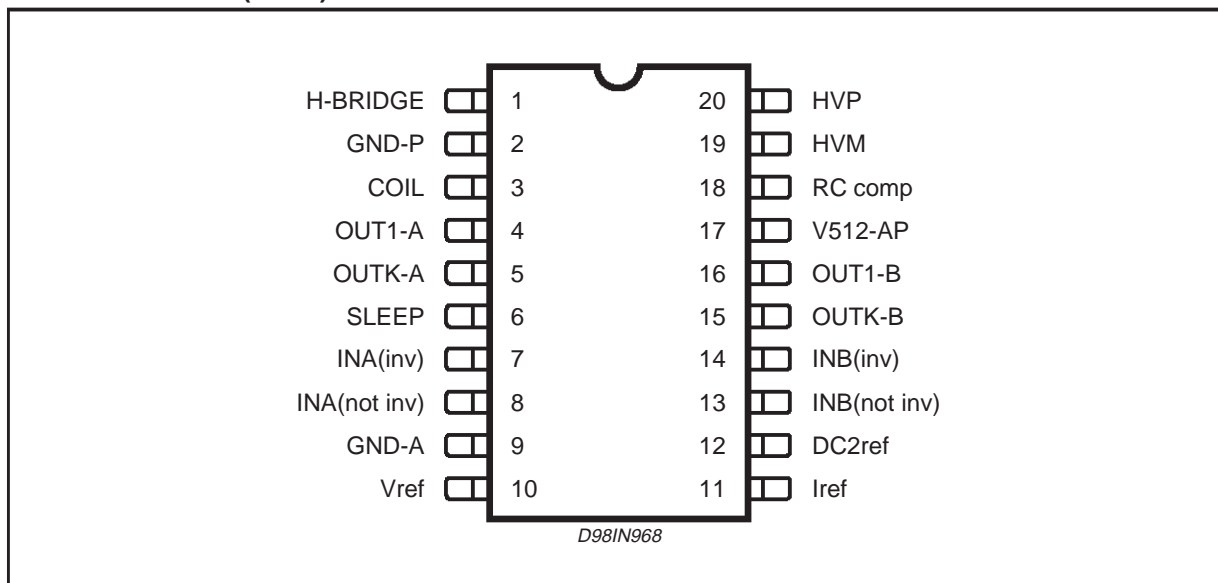
### DESCRIPTION

The L6270/1 is a piezoelectric actuator driver.

### BLOCK DIAGRAM



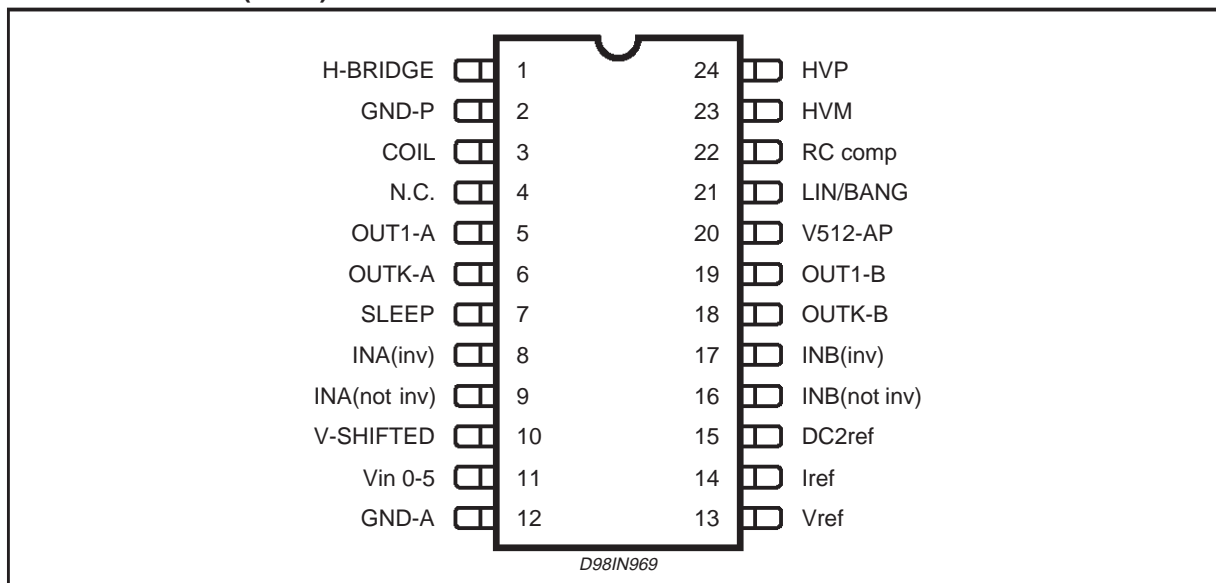
**PIN CONNECTION (SO20)**



**PIN FUNCTIONS (SO20)**

N.	Name	Description
1	H-BRIDGE	40V Half Bridge output for negative charge pump.
2	GND-P	Power ground.
3	COIL	Coil for positive step up.
4	OUT1-A	Output ampl.A.
5	OUTK-A	Hi current output ampl.A.
6	SLEEP	Sleep mode for stand-by condition (1=SLEEP 0=operative).
7	INA (inv)	Inverting input of A-amplifier.
8	INA (not inv)	Non Inverting input of A-amplifier.
9	GND-A	Analog ground.
10	V <sub>ref</sub>	Precise 2.5V reference voltage.
11	I <sub>ref</sub>	External resistor for precise internal current reference.
12	DC2ref	Reference voltage for DC-DC converter X20.
13	INB (not inv)	Non Inverting input of B-amplifier.
14	INB (inv)	Inverting input of B-amplifier.
15	OUTK-B	Hi current output ampl.B.
16	OUT1-B	Output ampl.B.
17	V512-AP	Analog&Power voltage supply 5 to 12V.
18	RC comp	DC-DC converter compensation network.
19	HVM	Negative High voltage generated op amp supplier.
20	HVP	Positive High voltage generated op amp supplier.

## PIN CONNECTION (SO24)



## PIN FUNCTIONS (SO24)

N.	Name	Description
1	H-BRIDGE	40V Half Bridge output for negative charge pump.
2	GND-P	Power ground.
3	COIL	Coil for positive step up.
4	N.C.	
5	OUT1-A	Output ampl.A.
6	OUTK-A	Hi current output ampl.A.
7	SLEEP	Sleep mode for stand-by condition (1=SLEEP 0=operative).
8	INA (inv)	Inverting input of A-amplifier.
9	INA (not inv)	Non Inverting input of A-amplifier.
10	V-SHIFTED	Analog level shifter output Vin-Vref (-2.5 to +2.5 dynamic range)
11	Vin 0-5	Input positive voltage
12	GND-A	Analog ground.
13	V <sub>ref</sub>	Precise 2.5V reference voltage.
14	I <sub>ref</sub>	External resistor for precise internal current reference.
15	DC2ref	Reference voltage for DC-DC converter X20.
16	INB (not inv)	Non Inverting input of B-amplifier.
17	INB (inv)	Inverting input of B-amplifier.
18	OUTK-B	Hi current output ampl.B.
19	OUT1-B	Output ampl.B.
20	V512-AP	Analog&Power voltage supply 5 to 12V.
21	LIN/BANG	Linear or Bang-bang select pin (V512 = BANG 0 = Linear)
22	RC comp	DC-DC converter compensation network.
23	HVM	Negative High voltage generated op amp supplier.
24	HVP	Positive High voltage generated op amp supplier.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V512	Supply voltage pin 20 referred to Ground	14	V
HVP	Positive high voltage referred to HVM	84	V
HVM	Negative high voltage referred to Ground	-42	V
IN A&B	Amplifier input voltage common mode	±6	V
V <sub>in o to 5</sub>	Level shifts input voltage	-0.5 to +5.5	V
T <sub>amb</sub>	Operative Ambient Temperature	-20 to +80	°C
T <sub>stg</sub>	Storage Temperature	-40 to +125	°C

All the voltage value are referred to ground.

**ELECTRICAL CHARACTERISTICS** (All the following parameters are specified @ 27°C and V512 = 12V, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>512</sub>	Main power supply		4.5		13.2	V
HVP <sup>(1)</sup>	Output positive Voltage	Double Supply Voltage	25	40		V
		Single Supply Voltage V <sub>512</sub> ≥ 8	30		80	V
		Single Supply Voltage V <sub>512</sub> ≤ 8	25		40	V
HVM	Output negative voltage		-40		-25	V
HVRipple	HVP, HVM ripple	External filter cap. 100nF Bang-Bang Mode Linear Mode			2.5 0.8	V V
DC-DC gain	Ratio of HVP and DC-DC ref. voltage PIN15		19	20	21	
I <sub>hvp</sub>	Output current (see figure 1a)					
I <sub>hvm</sub>						
T <sub>op</sub>	Time to operating condition				5	ms
F <sub>switch</sub> <sup>(2)</sup>	Switching Frequency		80		550	kHz
R <sub>ds,on</sub>	Boost transistor ON resistance				4	Ω
I <sub>boost</sub>	Boost transistor current limiting				700	mA
CP-slope	Charge Pump Slope			150		V/μs
I <sub>sleep</sub>	Total current in sleep mode				1	mA
V <sub>ref</sub>	Reference voltage at PIN13		2.4	2.5	2.6	V
I <sub>vref</sub>	Reference voltage output current		-1		1	mA
V <sub>ref,cap</sub>	Filter capacitor at PIN13		10		100	nF
I <sub>ref,res</sub>	Resistor at PIN14 for precise internal current (100μA)			25		kΩ
V <sub>sup</sub>	Minimum OpAmp supply Voltage (HVP if externally given)	Double Supply	V512 +4			V
		Single Supply	V512 +4			V
DC gain	OpAmp DC gain			130		dB
GBW	OpAmp Gain Bandwidth product	Cload 0.4nF to 24nF Double Supply Voltage		500		KHz
DCinp	OpAmp Input dynamic voltage	Double supply	-5		5	V
		Single supply	1.2		10	V
DC-DC OFF	DC-DC Converter switched-off when DC <sup>2</sup> REF voltage lower than				0.6	V

## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{out}$	OpAmp Output dynamic voltage	Capacitive load	HVM		HVP	V
DC, $I_{bias}$	OpAmp Bias supply current (both)				7	mA
$I_{out}$	OpAmp Dynamic Output current		-75		75	mA
PSRR,P	OpAmp Positive power supply rejection ratio	@ 50kHz	TBD			dB
PSRR,N	OpAmp Negative power supply rejection ratio	@ 50kHz	TBD			dB
$C_{load}$	OpAmp Load capacitance range	Voltage mode Gain min 20dB	0.4		24	nF
$C_{int}$	OpAmp Integration capacitance	Charge mode Gain min 20dB	0.4		24	nF
K	OpAmp Current ratio OUTK/OUT1		9.8	10	10.2	
$I_{err}^{(3)}$	OpAmp $I_{outk}$	$I_{out1} = 0$	-10		50	$\mu$ A
$V_{offset}$	OpAmp Input offset voltage				$\pm 10$	mV
DCShift range	Dynamic Shifter Input Range		1		4	V

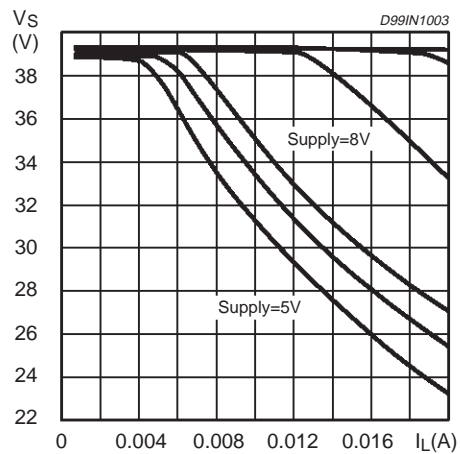
Note 1: Selectable by external resistor.

Note 2: Set by external Coil and Capacitor.

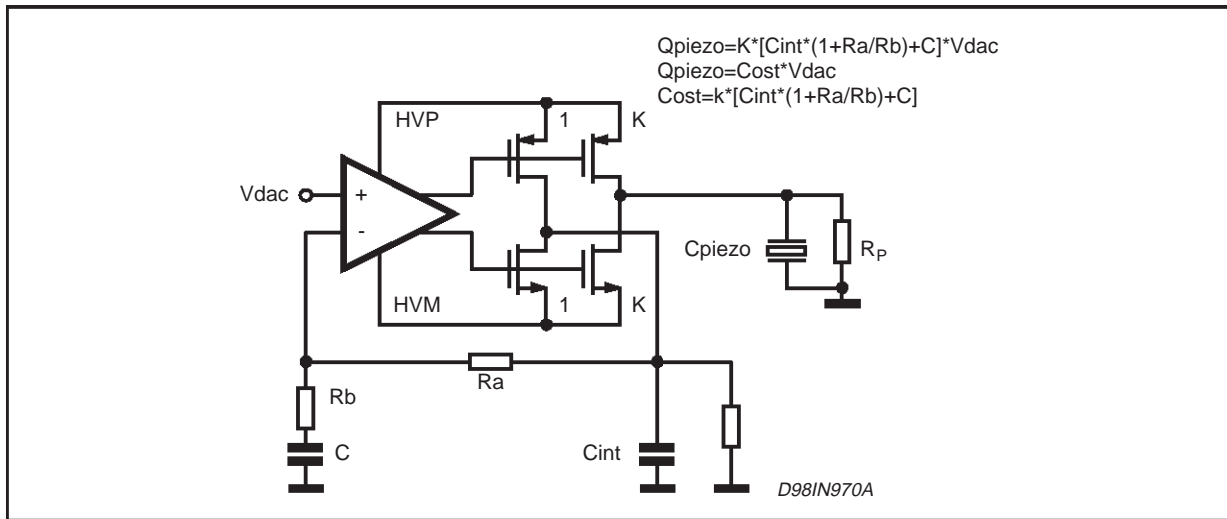
Note 3: It will be write after silicon characterization, it's designed for a maximum offset of a few mA.

In charge mode the Piezo is in openloop, and if  $C_{piezo} = 0.4nF$  with a maximum Current error of  $\pm 5\mu A$  the Maximum long time voltage drift is  $\pm 12mV/\mu s$

Figure 1a. HVP load regulation in single supply mode”.



**Figure 1. Charge Mode Configuration (only a suggestion, the application is completely free according with Electrical Characteristics).**



### OPERATIONAL AMPLIFIERS DESCRIPTION

Each driver has two output stages scaled in current by a factor  $K = 10$ .

In voltage mode configuration the two outputs are shorted.

In charge mode configuration OUT1 drives a capacitor  $C_{int}$  and is closed in feedback, while OUTK drives the piezo, mirroring the current supplied to  $C_{int}$ , with a current multiplied by a  $K$  factor (see Fig.1).

The supply voltage can be internally generated by the DC-DC converter, or external, maintaining the DC-DC converter in sleep mode (PIN15 shorted to ground), in this case the supply voltage can be 0 to  $V_{512+4}$  minimum value up to 80V in single supply or  $V_{512+4}$  to 40V symmetrical to ground.

The drivers have 130dB DC gain and the Bandwidth is 500KHz. Stability is granted with a minimum gain of 20dB, for a capacitive load in the range 0.4nF up to 24nF.

The drivers can be supplied with HVP-HVM (double supply mode) or with HVP-Ground (single supply mode). In both cases they can achieve a rail-to rail output dynamic range with a maximum load current of  $\pm 75\text{mA}$ .

In double supply mode the input stage has -5V/+5V dynamic range, while in single supply mode it has 1.2V up to 10V input dynamic range.

A 2.5V internal reference voltage is available at one pin ( $V_{ref}$ ) that can be used to close the feedback if the input signal is symmetrical around 2.5V.

In this case the output dynamic is symmetrical around 2.5V. It is present a 2.5V down level shifter that can be connected between the input signal and the input of the opamp, to work inter-

nally with a signal symmetrical to ground.

### DC-DC CONVERTER DESCRIPTION

The DC-DC converter inside the chip can be supplied from 5V up to 12V and has two parts, one to supply the positive and one to supply the negative voltage.

The positive one takes the reference from the pin  $DC^2REF$  and multiplies it by 20 to have the output voltage.

If  $DC^2REF$  is less than 0.6V the whole DC-DC converter is shut down and the high voltages have to be supplied from external. In Sleep Mode (sleep pin) HVM is shorted to GND. When in single supply, no load has to be connected to H-bridge output and HVM must be connected to GND.

The topology is a standard resonant full-wave boost one: the LC oscillation is kept running all the time and a set of comparators is used to synchronize turning on and off of the power MOS in order to have zero current and zero voltage switching and furthermore controlled rectification.

The step-up converter is designed to work in "Bang-Bang" mode and in Linear mode, in this case an AC compensation network is required (RC-comp) to guarantee the stability in a wide operative range (i.e. changing coil, load, output and input voltage...).

In **Bang-Bang mode** (Bang/Lin= $V_{512}$  high condition) whenever the output HVP goes down fixed threshold ( $V_{th,out} = 20 \cdot DC^2REF$ ), the next oscillation phase is more powerful and is used to transfer energy from the power supply to the output.

In **Linear mode**, according to the output voltage, the current loaded into the coil is changing like a

Voltage Loop-Current Controlled system, and in every pulse there is a regulated power transfer to the load.

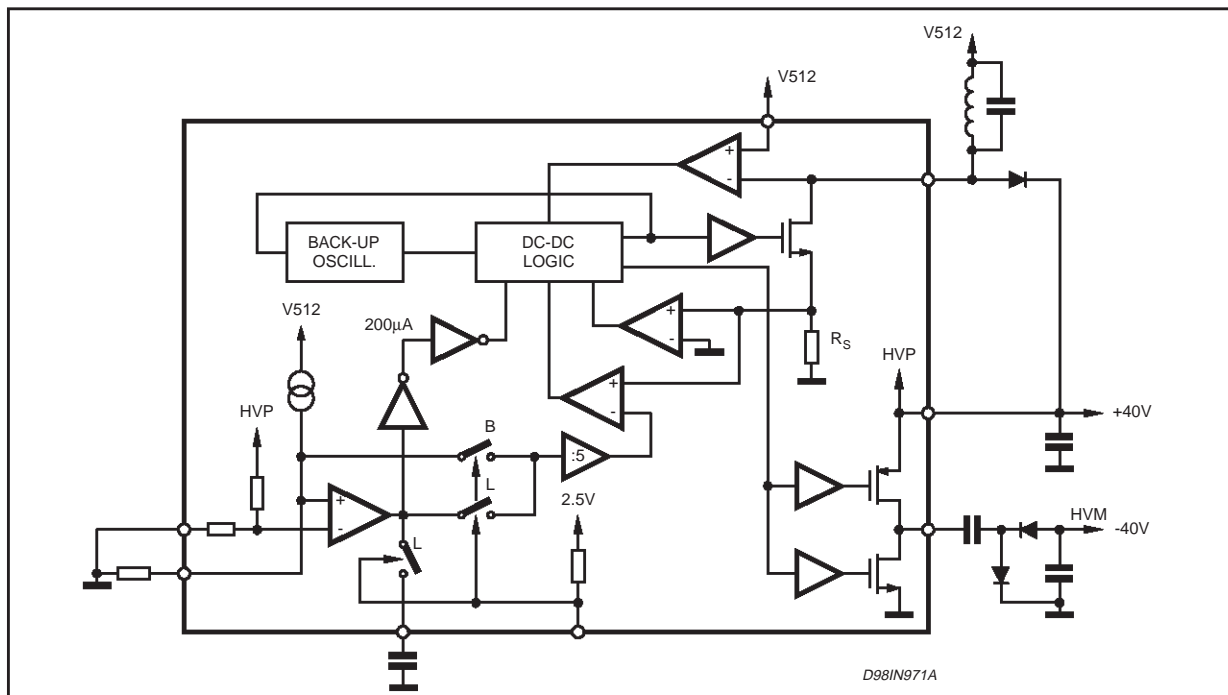
The resonant LC topology has been chosen in order to limit the voltage slew-rate across the coil within reasonable values and so, to minimize irradiation problems.

The negative converter is a simple charge transfer: it is supplied by the positive high voltage and it capacitively translates this positive voltage

down to a negative one, obviously to limit irradiation problems also the charge output has a limited slew-rate; moreover to reduce intermodulation phenomena the charge output is synchronized with the LC oscillations of the resonant boost.

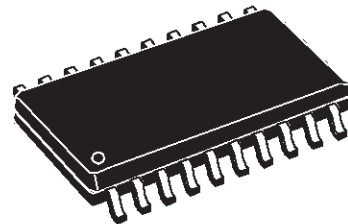
This negative voltage is (not counting drops on external rectification diodes) in tracking with the positive one and so the negative output controller is not required.

**Figure 3. DC-DC converter**

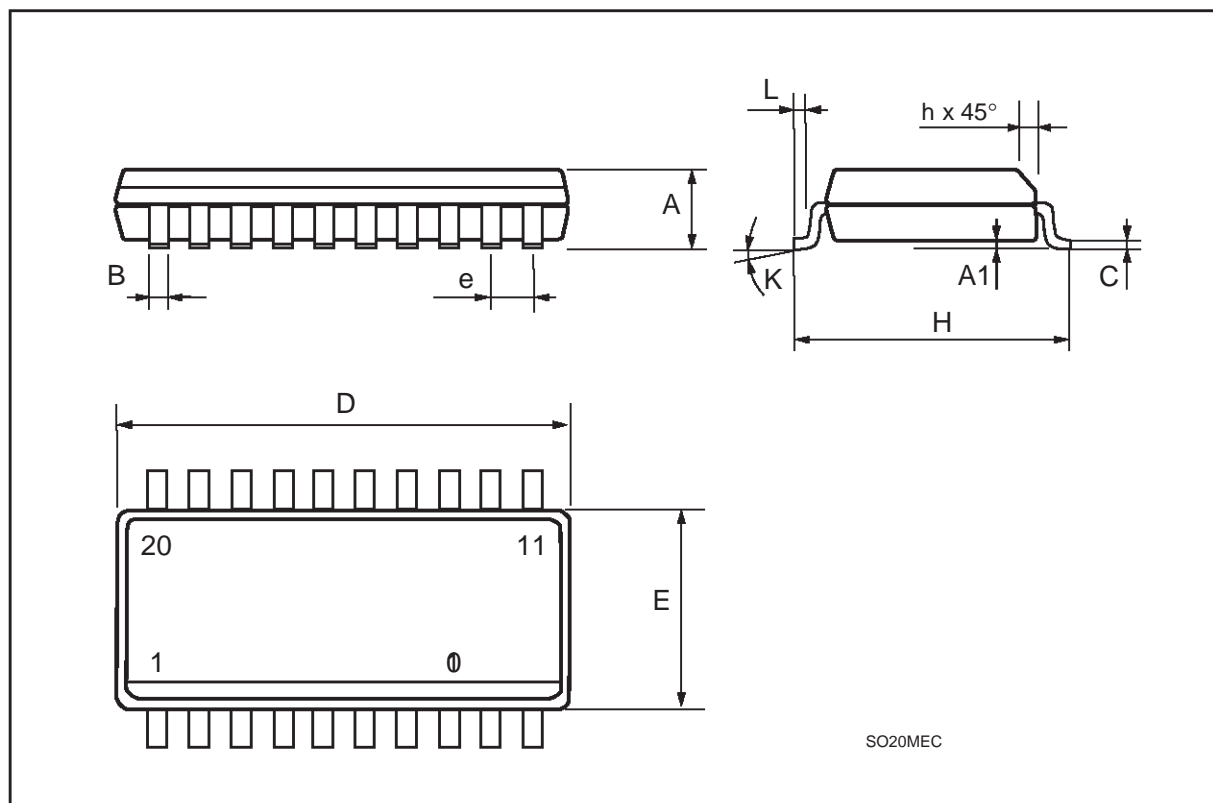


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SO20**

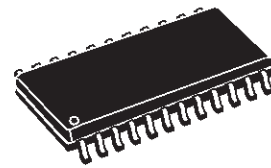


SO20MEC

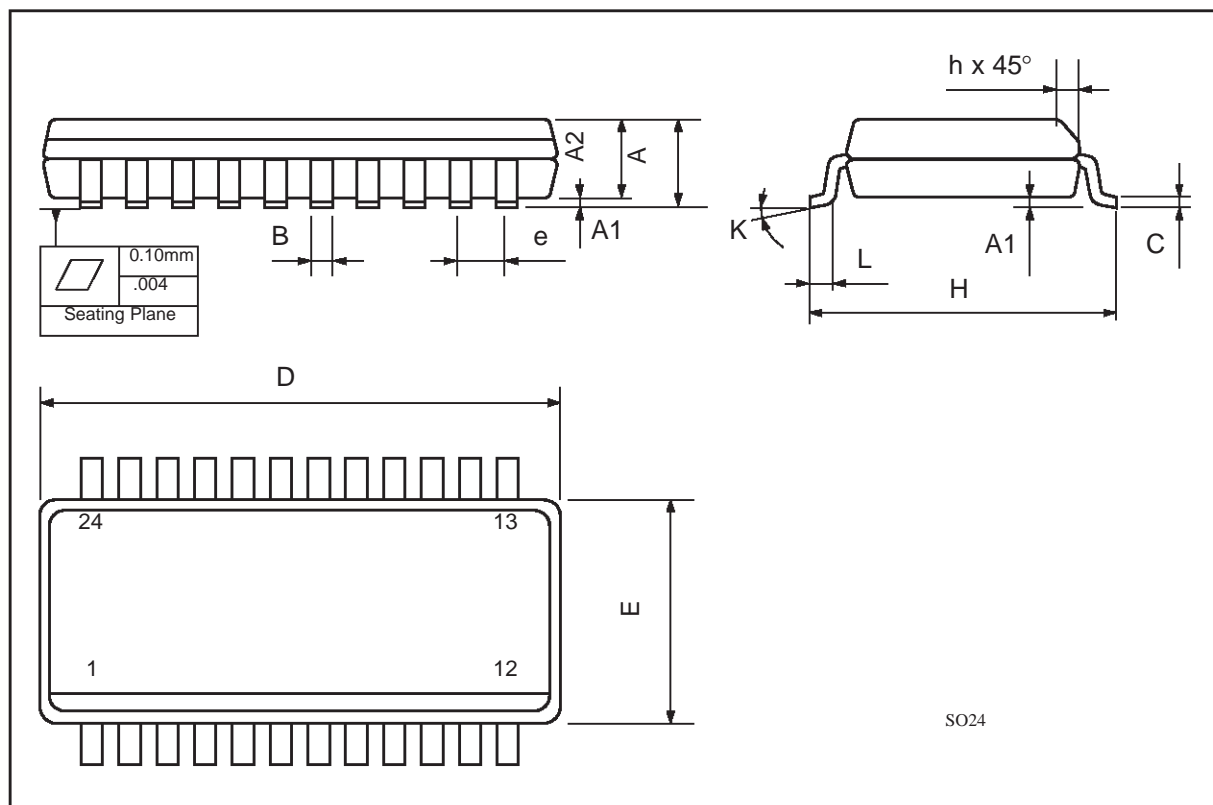


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.0200
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0,050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
k	0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050

## OUTLINE AND MECHANICAL DATA



**SO24**



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