



74AC299

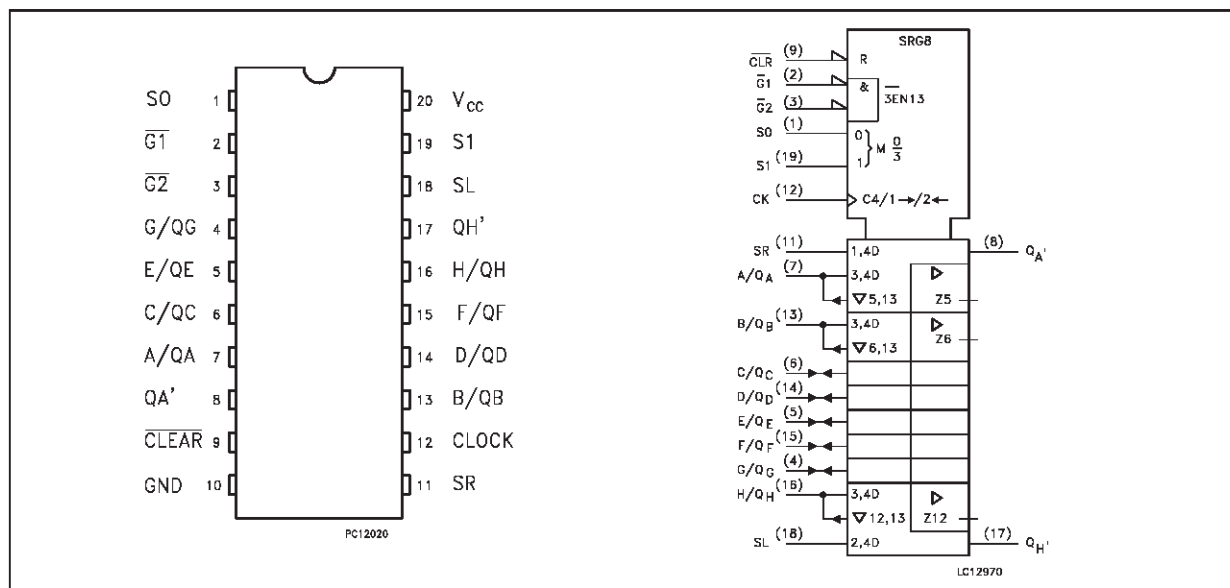
8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

- HIGH SPEED:
 $f_{MAX} = 170 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 8 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2\text{V to } 6\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 299
- IMPROVED LATCH-UP IMMUNITY

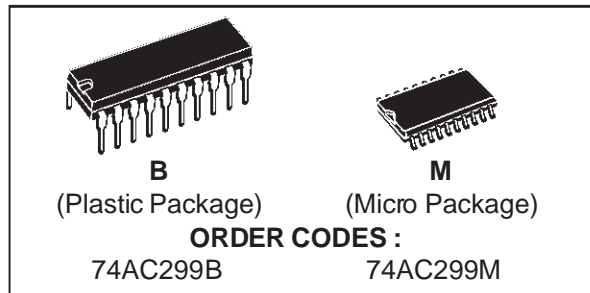
DESCRIPTION

The AC299 is an high-speed CMOS 8-BIT PIPO SHIFT REGISTERS (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power applications maintaining high speed operation similar to equivalent Bipolar Schottky

PIN CONNECTION AND IEC LOGIC SYMBOLS



PRELIMINARY DATA

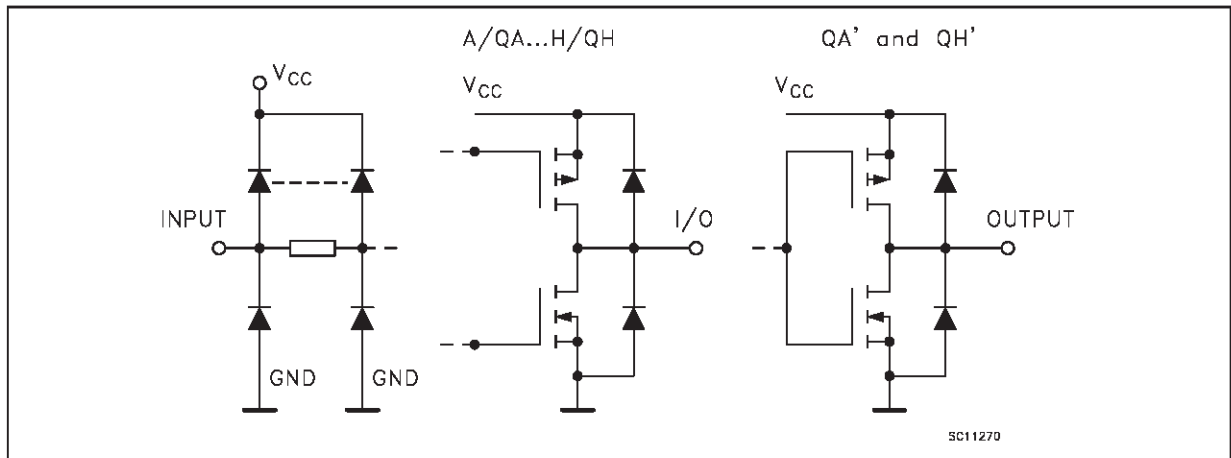


TTL.

These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1) as shown in the Truth Table.

When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected. Clear function is asynchronous to clock. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

| PIN No | SYMBOL | NAME AND FUNCTION |
|----------------------------|--------------------------------|---|
| 1, 19 | S0, S1 | Mode Select Inputs |
| 2, 3 | $\overline{G1}, \overline{G2}$ | 3 State Output Enable Inputs (Active LOW) |
| 7, 13, 6, 14, 5, 15, 4, 16 | A/QA to H/QH | Parallel Data Inputs or 3 State Parallel Outputs (Bus Driver) |
| 8, 17 | QA' to QH' | Serial Outputs (Standard Output) |
| 9 | \overline{CLEAR} | Asynchronous Master Reset Input (Active LOW) |
| 11 | SR | Serial Data Shift Right Input |
| 12 | CLOCK | Clock Input (LOW to HIGH, Edge-triggered) |
| 18 | SL | Serial Data Shift Left Input |
| 10 | GND | Ground (0V) |
| 20 | Vcc | Positive Supply Voltage |

TRUTH TABLE

| MODE | INPUTS | | | | | | INPUTS/OUTPUTS | | | | OUTPUTS | |
|-------------|--------------------|-------------------|----|-------------------|-------------------|-------|----------------|----|------|------|---------|-----|
| | \overline{CLEAR} | FUNCTION SELECTED | | OUTPUT CONTROL | | CLOCK | SERIAL | | A/QA | H/QH | QA' | QH' |
| | | S1 | S0 | $\overline{G1}^*$ | $\overline{G2}^*$ | | SL | SR | | | | |
| Z | L | H | H | X | X | X | X | X | Z | Z | L | L |
| CLEAR | L | L | X | L | L | X | X | X | L | L | L | L |
| | L | X | L | L | L | X | X | X | L | L | L | L |
| HOLD | H | L | L | L | L | X | X | X | QA0 | QH0 | QA0 | QH0 |
| SHIFT RIGHT | H | L | H | L | L | | X | H | H | QGn | H | QGn |
| | H | L | H | L | L | | X | L | L | QGn | L | QGn |
| SHIFT LEFT | H | H | L | L | L | | H | X | QBn | H | QBn | H |
| | H | H | L | L | L | | L | X | QBn | L | QBn | L |
| LOAD | H | H | H | X | X | | X | X | a | h | a | h |

* When one or both output controls are high, the eight, input/output terminals are the high impedance state; however sequential operation or clearing of the register is not affected.

Z : HIGH IMPEDANCE

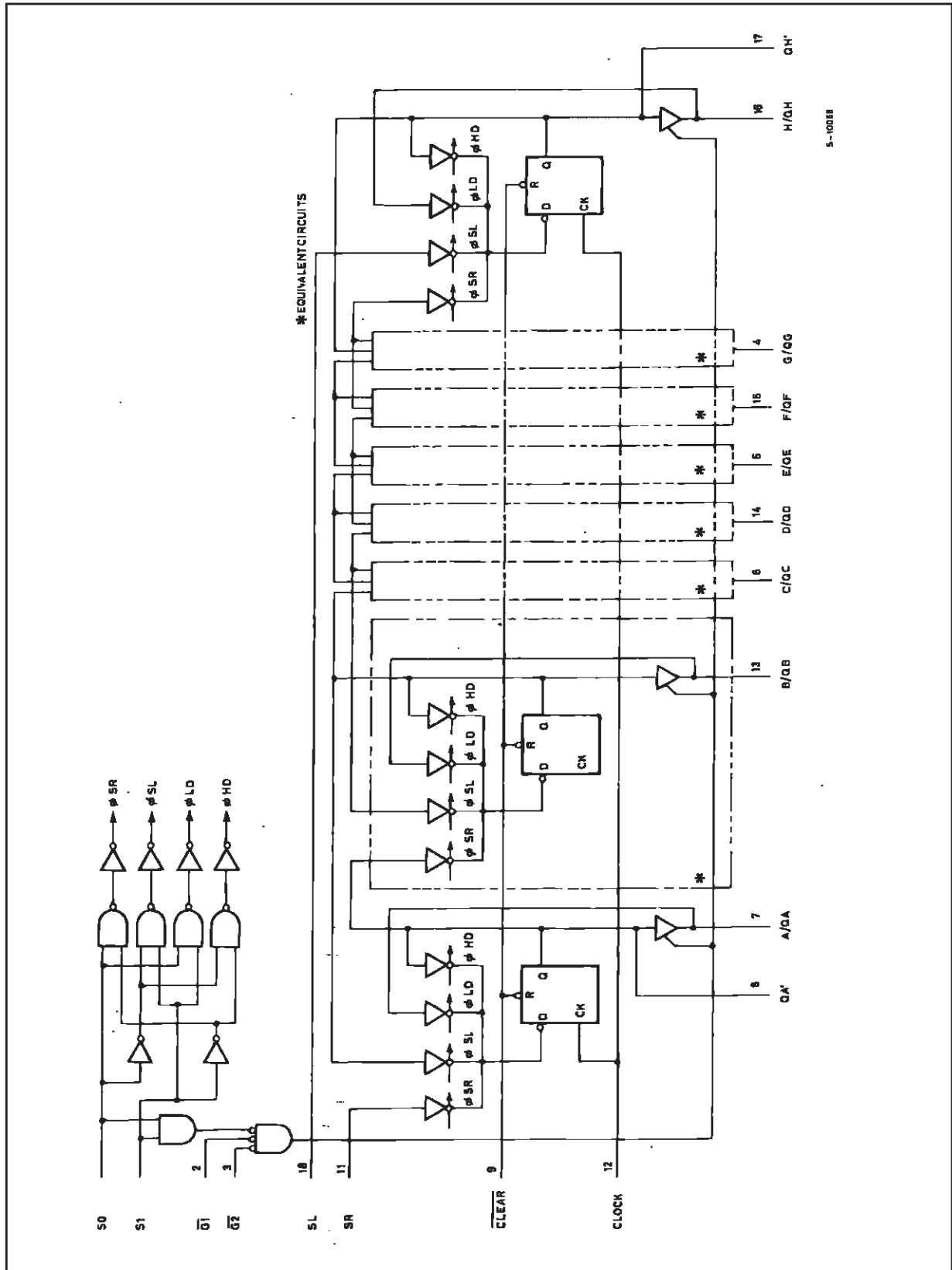
Qn0 : THE LEVEL OF An BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

Qnn : THE LEVEL OF Qn BEFORE THE MOST RECENT ACTIVE TRANSITION INDICATED BY OR

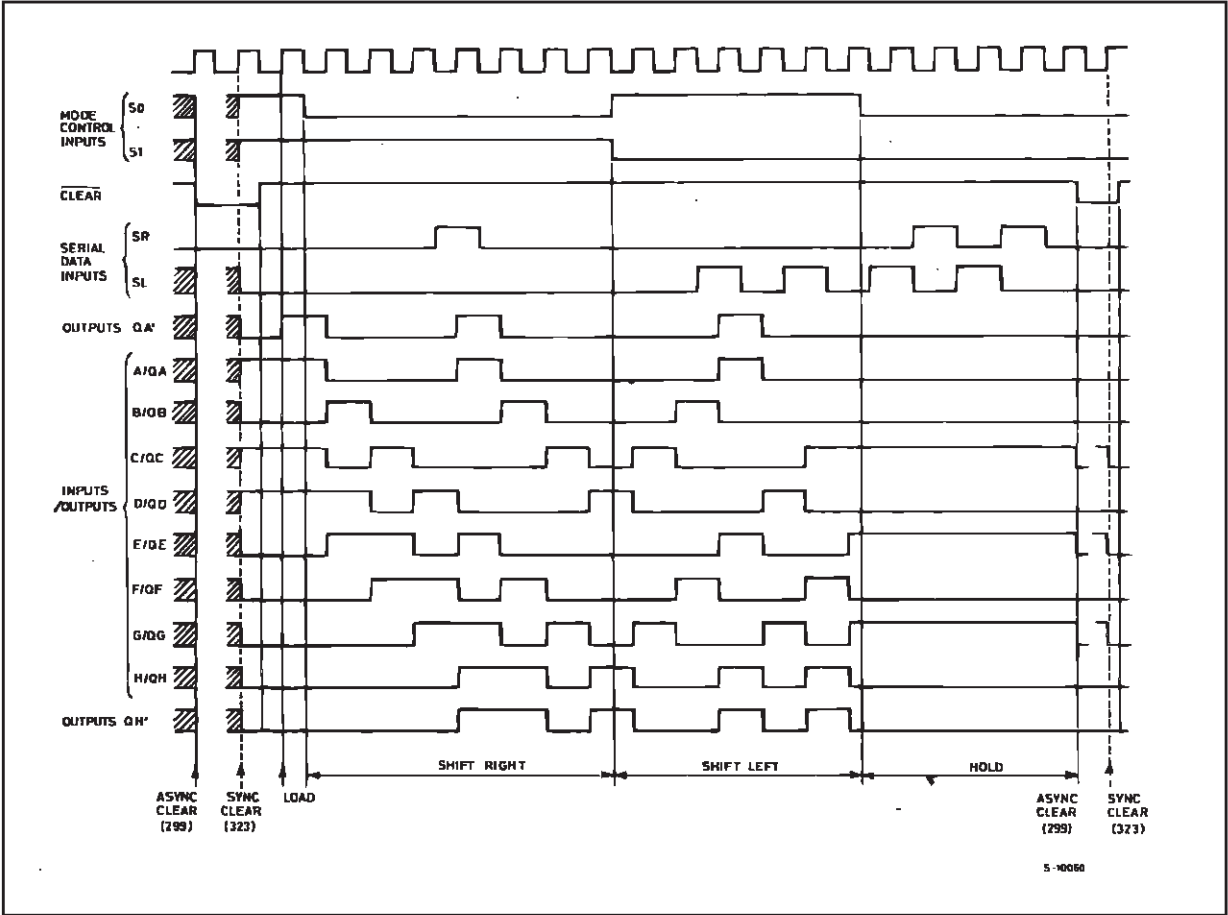
a, h : THE LEVEL OF THE STEADY STATE INPUTS A, H, RESPECTIVELY.

X : DONT CARE

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|-------------------------------|------------------------|-------------|
| V_{CC} | Supply Voltage | -0.5 to +7 | V |
| V_I | DC Input Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 20 | mA |
| I_O | DC Output Current | ± 50 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 400 | mA |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (10 sec) | 300 | $^{\circ}C$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|----------|---|---------------|-------------|
| V_{CC} | Supply Voltage | 2 to 6 | V |
| V_I | Input Voltage | 0 to V_{CC} | V |
| V_O | Output Voltage | 0 to V_{CC} | V |
| T_{op} | Operating Temperature: | -40 to +85 | $^{\circ}C$ |
| dt/dv | Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or 5.5 V(note 1) | 8 | ns/V |

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit | |
|------------------|---------------------------------------|------------------------|--|-------------------------|------|-------|--------------|------|------|---|
| | | V _{CC} (V) | | T _A = 25 °C | | | -40 to 85 °C | | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | | |
| V _{IH} | High Level Input Voltage | 3.0 | V _O = 0.1 V or V _{CC} - 0.1 V | 2.1 | 1.5 | | 2.1 | | V | |
| | | 4.5 | | 3.15 | 2.25 | | 3.15 | | | |
| | | 5.5 | | 3.85 | 2.75 | | 3.85 | | | |
| V _{IL} | Low Level Input Voltage | 3.0 | V _O = 0.1 V or V _{CC} - 0.1 V | | 1.5 | 0.9 | | 0.9 | V | |
| | | 4.5 | | | 2.25 | 1.35 | | 1.35 | | |
| | | 5.5 | | | 2.75 | 1.65 | | 1.65 | | |
| V _{OH} | High Level Output Voltage | 3.0 | V _I ^(*) = V _{IH} or V _{IL} | I _O = -50 μA | 2.9 | 2.99 | | 2.9 | V | |
| | | 4.5 | | I _O = -50 μA | 4.4 | 4.49 | | 4.4 | | |
| | | 5.5 | | I _O = -50 μA | 5.4 | 5.49 | | 5.4 | | |
| | | 3.0 | | I _O = -12 mA | 2.56 | | | 2.46 | | |
| | | 4.5 | | I _O = -24 mA | 3.86 | | | 3.76 | | |
| | | 5.5 | | I _O = -24 mA | 4.86 | | | 4.76 | | |
| V _{OL} | Low Level Output Voltage | 3.0 | V _I ^(*) = V _{IH} or V _{IL} | I _O = 50 μA | | 0.002 | 0.1 | | 0.1 | V |
| | | 4.5 | | I _O = 50 μA | | 0.001 | 0.1 | | 0.1 | |
| | | 5.5 | | I _O = 50 μA | | 0.001 | 0.1 | | 0.1 | |
| | | 3.0 | | I _O = 12 mA | | | 0.36 | | 0.44 | |
| | | 4.5 | | I _O = 24 mA | | | 0.36 | | 0.44 | |
| | | 5.5 | | I _O = 24 mA | | | 0.36 | | 0.44 | |
| I _I | Input Leakage Current | 5.5 | V _I = V _{CC} or GND | | | ±0.1 | | ±1 | μA | |
| I _{OZ} | 3 State Output Leakage Current | 5.5 | V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND | | | ±0.5 | | ±5 | μA | |
| I _{CC} | Quiescent Supply Current | 5.5 | V _I = V _{CC} or GND | | | 8 | | 80 | μA | |
| I _{OLD} | Dynamic Output Current (note 1, 2) | 5.5 | V _{OLD} = 1.65 V max | | | | | 75 | mA | |
| I _{OHD} | | | V _{OHD} = 3.85 V min | | | | | -75 | mA | |

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

| Symbol | Parameter | Test Condition | | Value | | | | | Unit | |
|--------------------------------------|--|---|--|------------------------|------------------------|--------------|------------|--------------|------|------|
| | | | | V _{CC} (V) | T _A = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | | Max. |
| t _{PLH} t _{PHL} | Propagation Delay Time CK to Q'A, Q'H | 3.3 ^(*) 5.0 ^(*) | | | 10.6 6.8 | 18.4 10.5 | 1.0 1.0 | 21.0 12.0 | ns | |
| t _{PLH} t _{PHL} | Propagation Delay Time CK to Q _A - Q _H | 3.3 ^(*) 5.0 ^(*) | | | 10.9 7.3 | 19.3 10.5 | 1.0 1.0 | 22.0 12.0 | ns | |
| t _{PLH} t _{PHL} | Propagation Delay Time CLEAR to Q'A, Q'H | 3.3 ^(*) 5.0 ^(*) | | | 8.1 6.1 | 14.0 9.2 | 1.0 1.0 | 16.0 10.5 | ns | |
| t _{PLH} t _{PHL} | Propagation Delay Time CLEAR to Q _A - Q _H | 3.3 ^(*) 5.0 ^(*) | | | 9.8 6.7 | 16.7 10.9 | 1.0 1.0 | 19.0 12.4 | ns | |
| t _{PZL} t _{PZH} | Output Enable Time | 3.3 ^(*) 5.0 ^(**) | | | 9.9 6.6 | 17.5 9.6 | 1.0 1.0 | 20.0 11.0 | ns | |
| t _{PLZ} t _{PHZ} | Output Disable Time | 3.3 ^(*) 5.0 ^(**) | | | 8.1 6.4 | 14.0 9.6 | 1.0 1.0 | 16.0 11.0 | ns | |
| t _w | CLEAR pulse Width, LOW | 3.3 ^(*) 5.0 ^(**) | | | | 7.0 5.0 | | 7.0 5.0 | ns | |
| t _w | CK pulse Width, LOW | 3.3 ^(*) 5.0 ^(**) | | | | 8.0 5.0 | | 8.0 5.0 | ns | |
| t _s | Setup Time HIGH or LOW (S0 or S1 to CK) | 3.3 ^(*) 5.0 ^(**) | | | | 11.9 7.0 | | 13.6 7.0 | ns | |
| t _h | Hold Time HIGH or LOW (S0 or S1 to CK) | 3.3 ^(*) 5.0 ^(**) | | | | 0.0 0.0 | | 0.0 0.0 | ns | |
| t _s | Setup Time HIGH or LOW (SR or SL to CK) | 3.3 ^(*) 5.0 ^(**) | | | | 6.0 4.0 | | 6.0 4.0 | ns | |
| t _h | Hold Time HIGH or LOW (SR or SL to CK) | 3.3 ^(*) 5.0 ^(**) | | | | 1.0 1.0 | | 1.0 1.0 | ns | |
| t _{REM} | Recovery Time CLR to Q | 3.3 ^(*) 5.0 ^(**) | | | | 5.0 3.0 | | 5.0 3.0 | ns | |
| f _{MAX} | Maximum Clock Frequency | 3.3 ^(*) 5.0 ^(**) | | | 45 80 | 90 140 | 45 80 | | MHz | |

(*) Voltage range is 3.3V ± 0.3V

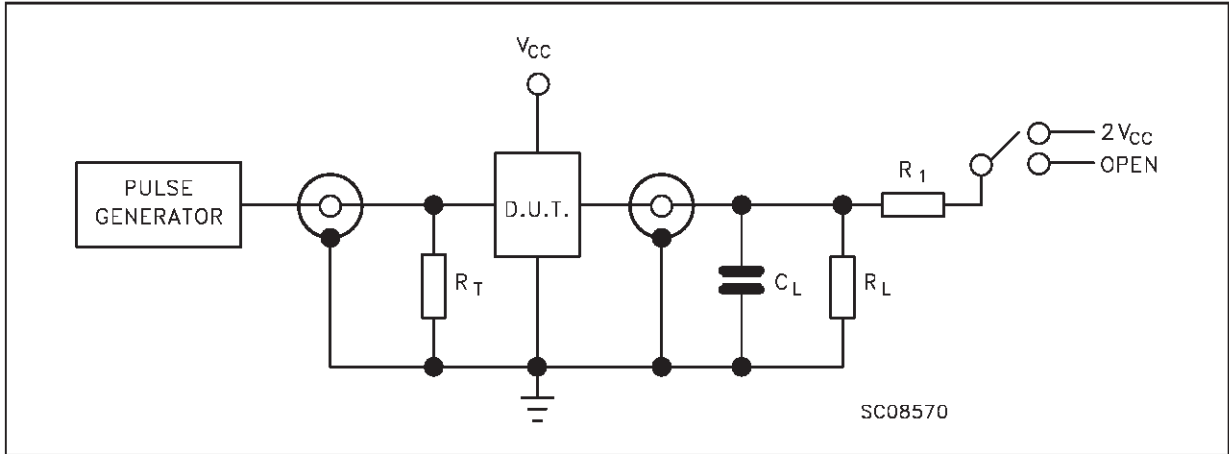
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit | |
|------------------|---|-----------------|--------------------------|------------------------|------------------------|------|------|--------------|------|------|
| | | | | V _{CC} (V) | T _A = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | | Max. |
| C _{IN} | Input Capacitance | 5.0 | | | 5 | 10 | | 10 | pF | |
| C _{I/O} | Bus Input Capacitance | 5.0 | | | 13 | | | | | |
| C _{PD} | Power Dissipation Capacitance (note 1) | 5.0 | f _{IN} = 10 MHz | | 137 | | | | pF | |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to

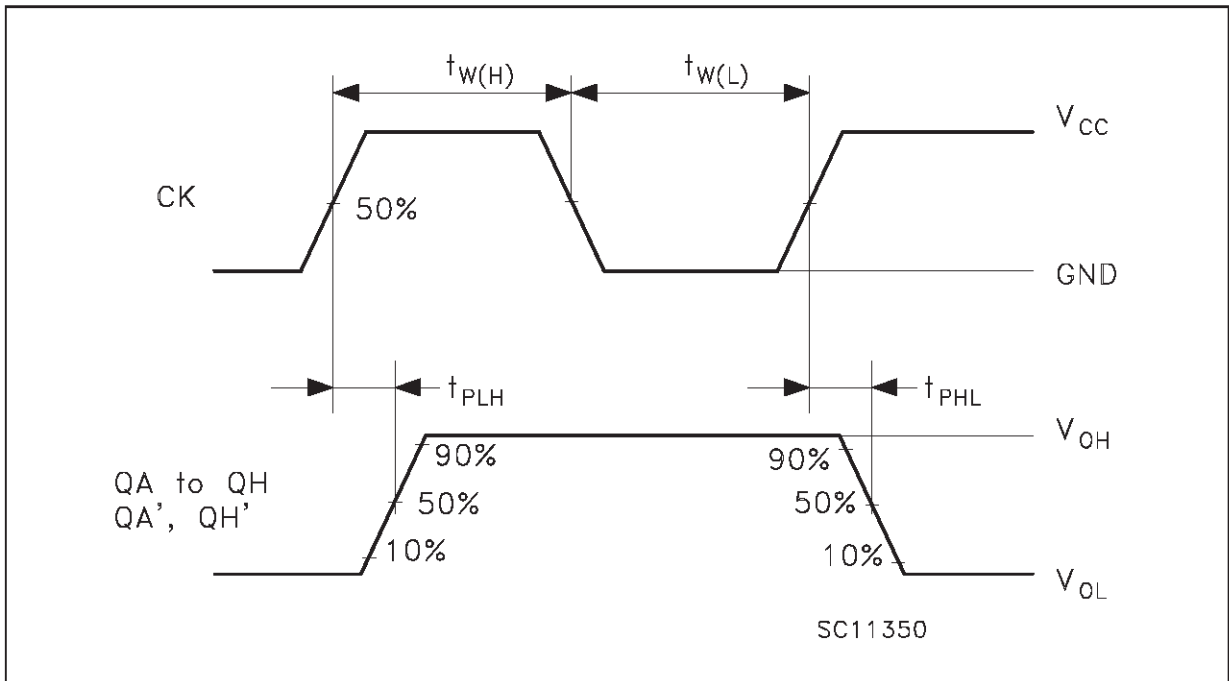
TEST CIRCUIT



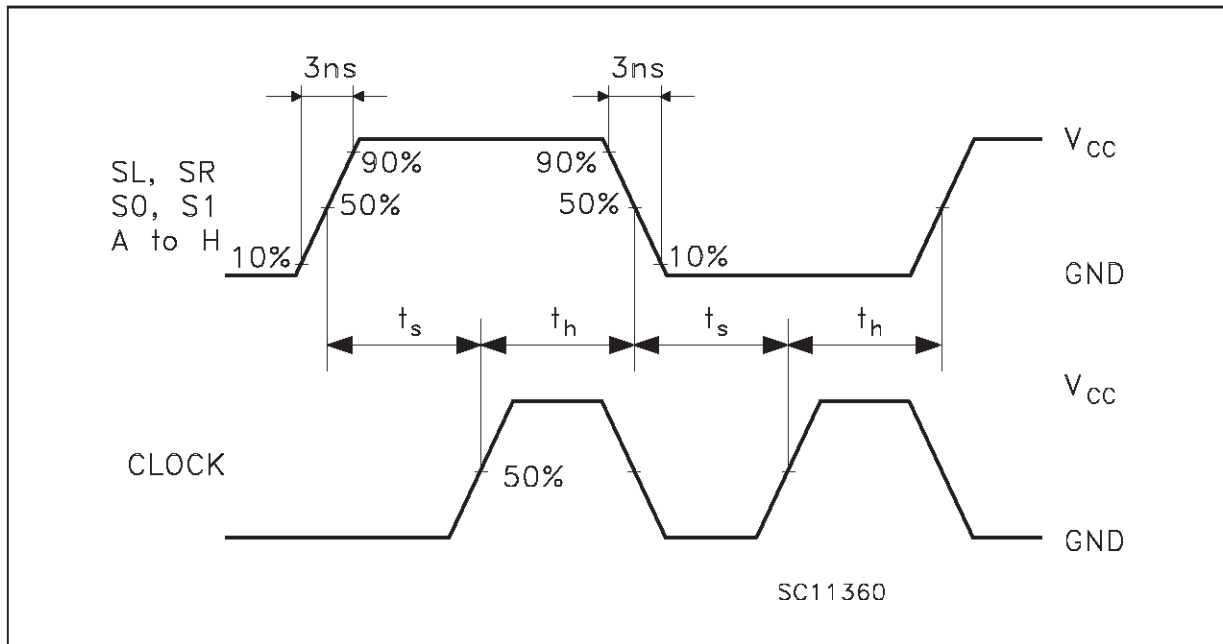
| TEST | SWITCH |
|-----------------------|-----------|
| t_{PLH} , t_{PHL} | Open |
| t_{PZL} , t_{PLZ} | $2V_{CC}$ |
| t_{PZH} , t_{PHZ} | Open |

C_L = 50 pF or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

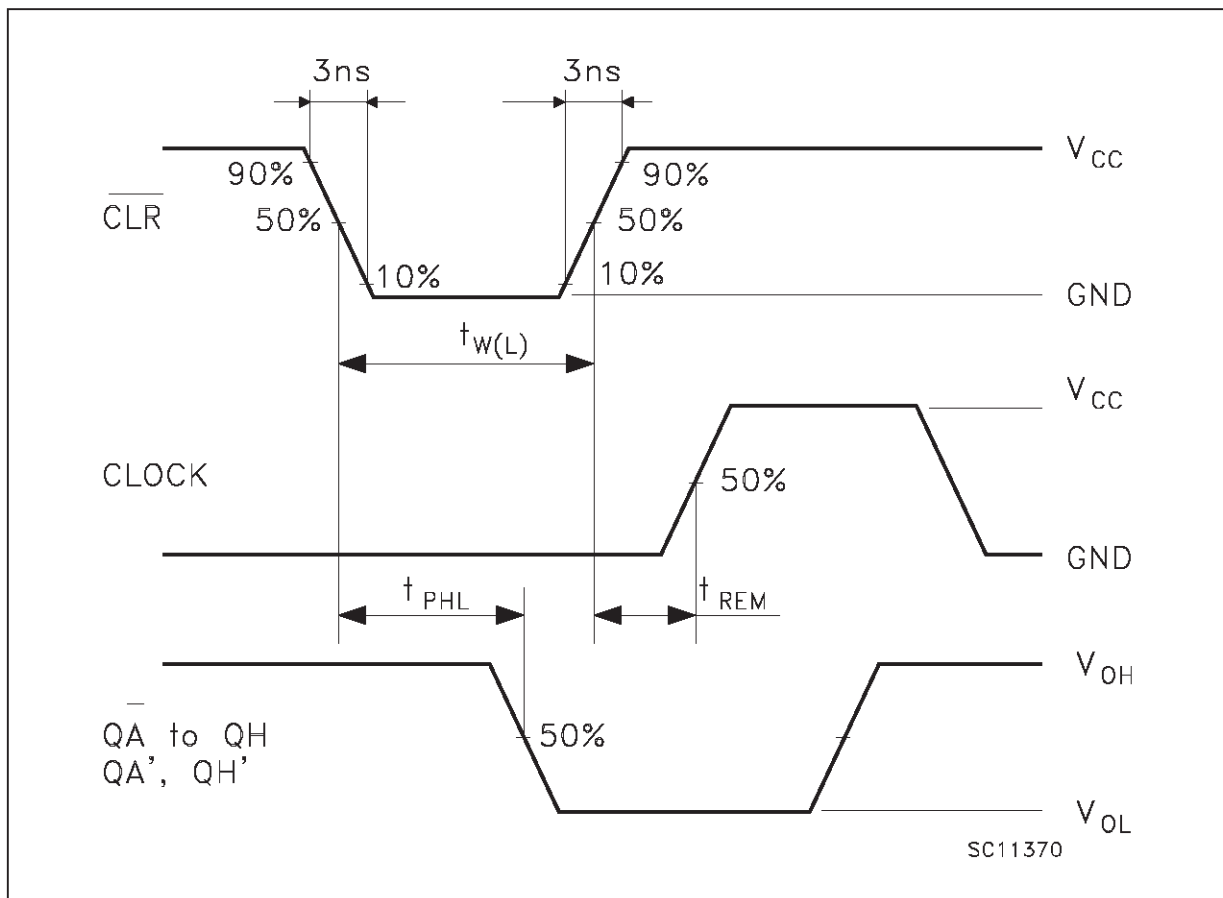
WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)



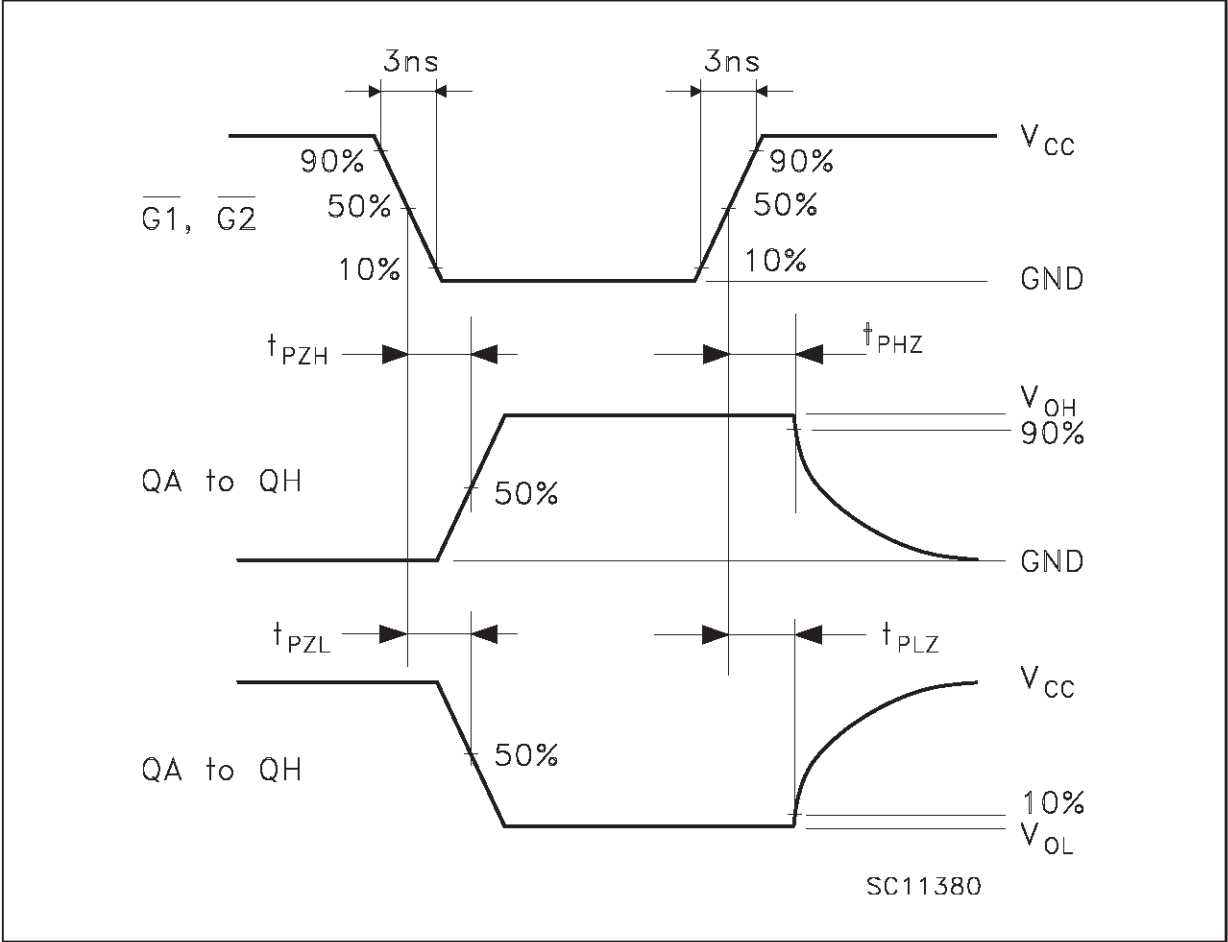
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

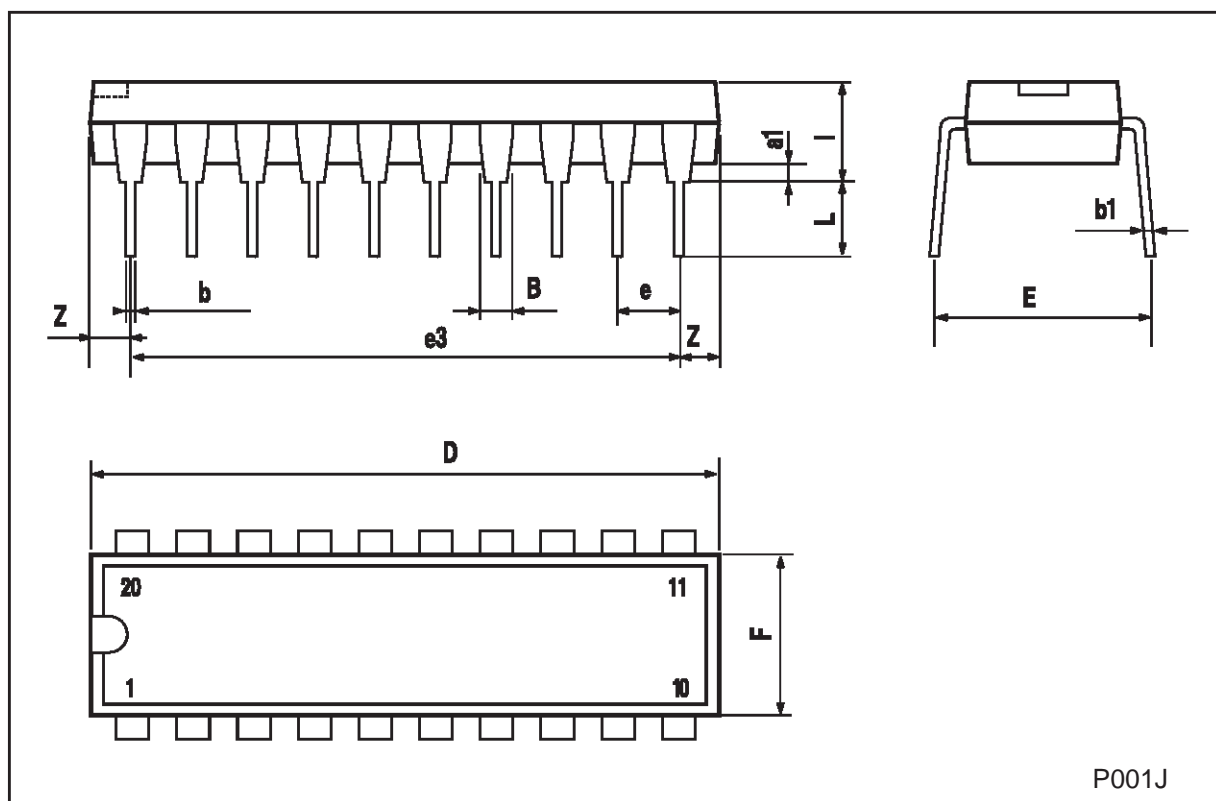


WAVEFORM 4: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



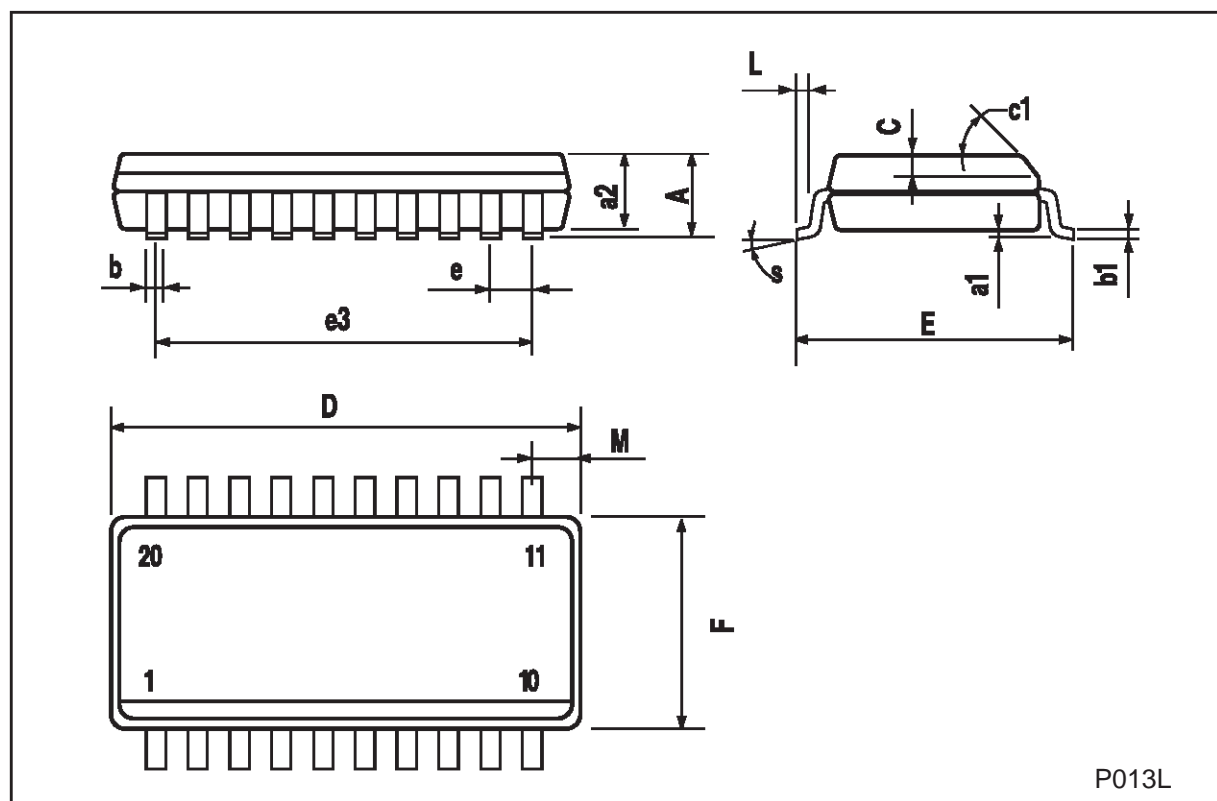
Plastic DIP-20 (0.25) MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-------|-------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.254 | | | 0.010 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.45 | | | 0.018 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 25.4 | | | 1.000 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 22.86 | | | 0.900 | |
| F | | | 7.1 | | | 0.280 |
| l | | | 3.93 | | | 0.155 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.34 | | | 0.053 |



SO-20 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-----------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.10 | | 0.20 | 0.004 | | 0.007 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.013 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.50 | | | 0.020 | |
| c1 | 45 (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.299 |
| L | 0.50 | | 1.27 | 0.19 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8 (max.) | | | | | |



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