



STT4NF30L

N - CHANNEL 30V - 0.055Ω - 4A - TSOP-6 STripFET™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STT4NF30L	30 V	< 0.065 Ω	4 A

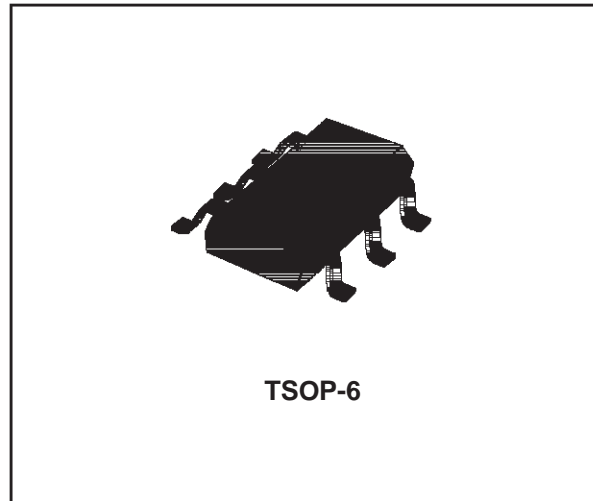
- TYPICAL R_{DS(on)} = 0.055 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

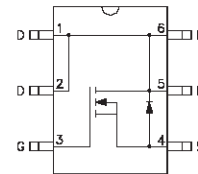
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/DESKTOP PCs



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	4	A
I _D	Drain Current (continuous) at T _c = 100 °C	2.5	A
I _{DM} (●)	Drain Current (pulsed)	16	A
P _{tot}	Total Dissipation at T _c = 25 °C	2	W

(●) Pulse width limited by safe operating area

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THERMAL DATA

$R_{thj-amb}$	(*)Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}\text{C}/\text{W}$
T_J	Maximum Operating Junction Temperature		150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature		-55 to 150	$^{\circ}\text{C}$

(*) Mounted on FR-4 board ($t \leq 5$ sec)

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu\text{A}$ $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ $I_D = 2 \text{ A}$ $V_{GS} = 4.5\text{V}$ $I_D = 2 \text{ A}$		0.055 0.06	0.065 0.09	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 \text{ V}$	4			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 6 \text{ A}$		6		S
C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$ $f = 1 \text{ MHz}$ $V_{GS} = 0$		420	550	pF
C_{oss}	Output Capacitance			62	80	pF
C_{rss}	Reverse Transfer Capacitance			20	30	pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 15\text{ V}$ $I_D = 2\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (see test circuit, figure 3)		13	17	ns
t_r	Rise Time			30	40	ns
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}$ $I_D = 4\text{ A}$ $V_{GS} = 4.5\text{ V}$		8	12	nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			2.6		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 24\text{ V}$ $I_D = 4\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (see test circuit, figure 5)		6	8	ns
t_f	Fall Time			9	12	ns
t_c	Cross-over Time			20	26	ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				16	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 4\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		22		ns
Q_{rr}	Reverse Recovery Charge			13		nC
I_{RRM}	Reverse Recovery Current			1.2		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

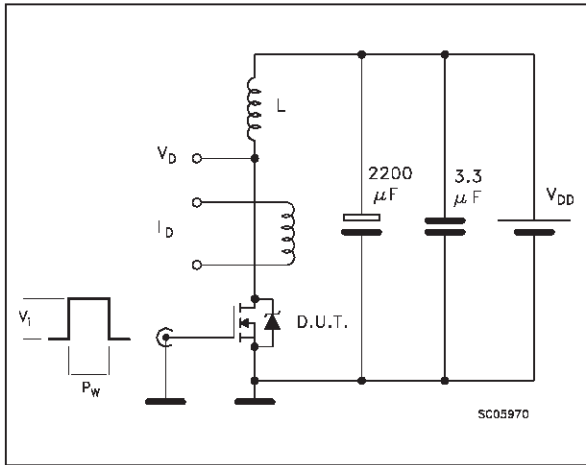


Fig. 2: Unclamped Inductive Waveform

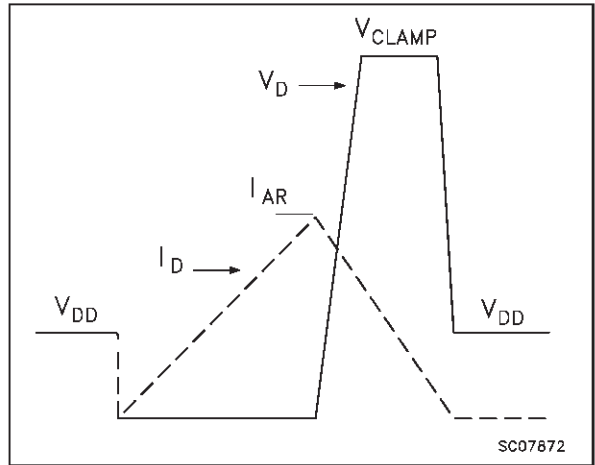


Fig. 3: Switching Times Test Circuits For Resistive Load

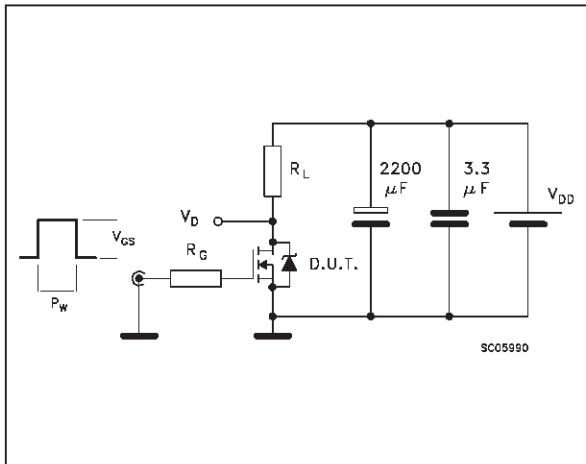


Fig. 4: Gate Charge test Circuit

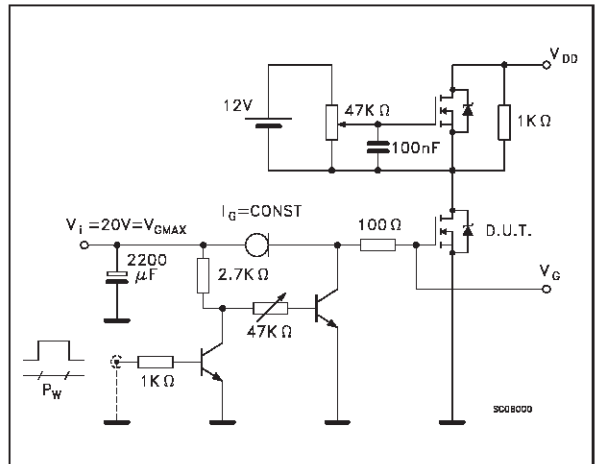
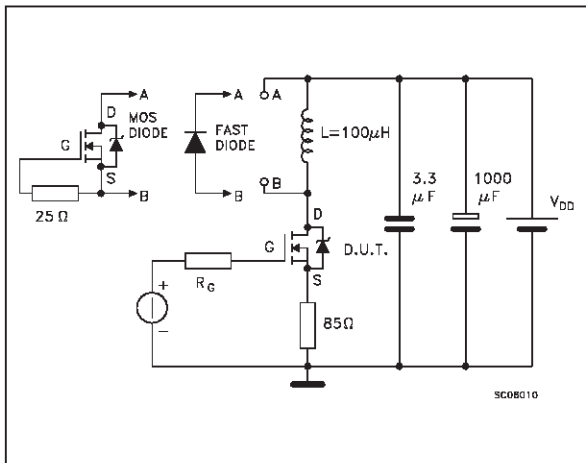


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



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