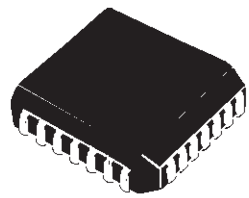
ST7536

POWER LINE MODEM

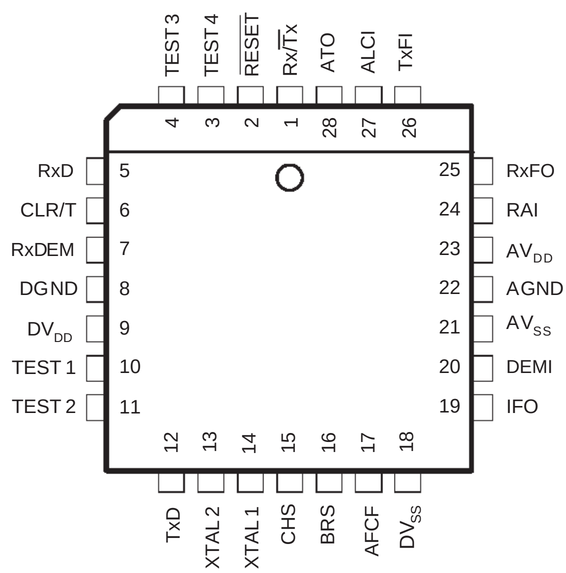
- HALF DUPLEX SYNCHRONOUS FSK MODEM
  - TWO PROGRAMMABLE CHANNELS FOR 600BPS DATA RATE
  - TWO PROGRAMMABLE CHANNELS FOR 1200BPS DATA RATE
- AUTOMATICALLY TUNED Rx AND Tx FILTERS
- TX CARRIER FREQUENCIES SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL (S/H2 $\geq$ 50dB)
- AUTOMATIC LEVEL CONTROL ON Tx SIGNAL
- Rx SENSITIVITY : $2mV_{RMS}$ (600bps)
  $3mV_{RMS}$ (1200bps)
- Rx CLOCK RECOVERY
- POWER-DOWN MODE
- SUITABLE TO APPLICATION IN ACCORDANCE WITH DH028/29 ENEL, EN50065-1 CENELEC AND FCC SPECIFICATIONS



PLCC28
(Plastic Leaded Chip Carrier Package)

ORDER CODE : ST7536CFN

PIN CONNECTIONS



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DESCRIPTION

The ST7536 is a half duplex synchronous FSK MODEM designed for power line communication network applications.

It operates from a dual power supply +5V and -5V, and requires an external interface for the coupling to the power line. It offers two programmable data rate with two programmable channels each.

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	Rx/$\overline{Tx}$	Digital	Rx or Tx mode selection input
2	$\overline{RESET}$	Digital	Logic reset and power-down mode input. Active when low.
3	TEST4	Digital	Test input which selects the Tx band-pass filter input (TxFI) when high.
4	TEST3	Digital	Test input which gives an access to the clock recovery input stage. This input is selected when TEST1 is high.
5	RxD	Digital	Synchronous receive data output
6	CLR/T	Digital	Rx or Tx clock according to the functional mode
7	RxDEM	Digital	Demodulated data output
8	DGND	Supply	Digital ground
9	DV_{DD}	Supply	Digital positive supply voltage : 5V $\pm$ 5%
10	TEST1	Digital	Test input which cancels the Tx to Rx mode automatic switching and validates TEST3 input. Active when high.
11	TEST2	Digital	Test input which reduces the Tx to Rx mode automatic switching time. Active when high.
12	TxD	Digital	Transmit data input
13	XTAL2	Digital	Crystal oscillator output
14	XTAL1	Digital	Crystal oscillator input
15	CHS	Digital	Channel selection input
16	BRS	Digital	Baud rate selection input
17	AFCF	Analog	Automatic frequency control output for connecting compensation network.
18	DV_{SS}	Supply	Digital negative supply voltage : -5V $\pm$ 5%
19	IFO	Analog	Intermediate frequency filter output
20	DEMI	Analog	FSK demodulator input
21	AV_{SS}	Supply	Analog negative supply voltage : -5V $\pm$ 5%
22	AGND	Supply	Analog ground : 0V
23	AV_{DD}	Supply	Analog positive supply voltage : 5V $\pm$ 5%
24	RAI	Analog	Receive analog input
25	RxFO	Analog	Receive filter output
26	TxFI	Analog	Transmit filter input (selected when TEST4 is high)
27	ALCI	Analog	Automatic level control input
28	ATO	Analog	Analog transmit output

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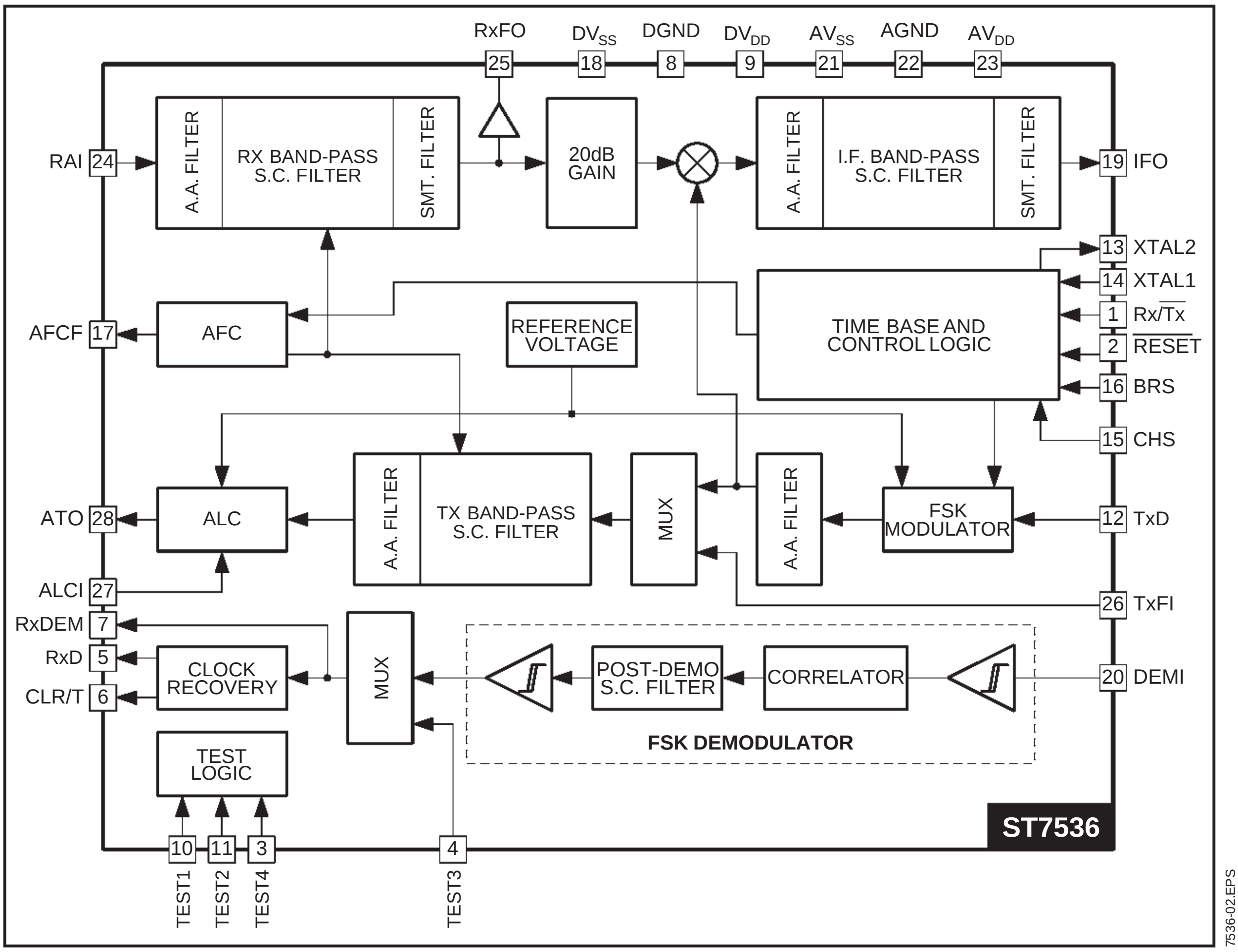
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - Transmit Section

The transmit mode is set when $Rx/\overline{Tx}$ = 0, if $Rx/\overline{Tx}$ is held at 0 longer than 3s, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires $Rx/\overline{Tx}$ to be returned to 1 for a minimum 2µs period before being set to 0.

The Transmit Data (TxD) is sampled on a positive edge of CLR/T which delivers the transmit bit clock when the transmit mode is selected. This data enters a FSK modulator whose two basic frequencies are selected by the Baud Rate Selection pin (BRS) and the Channel Selection pin (CHS) according to the Table 1.

Figure 1 : Tx Data Input Timing

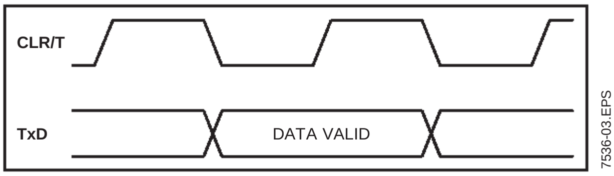


Table 1

BRS	CHS	Baud Rate (Baud)	Tx Frequencies (kHz) TxD=1 - TxD=0
0	0	600	81.75 - 82.35
0	1	600	67.2 - 67.8
1	0	1200	71.4 - 72.6
1	1	1200	85.95 - 87.15

These frequencies are synthesized from a 11.0592MHz crystal oscillator ; their precision is the same as the crystal one's (100 ppm).

The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.

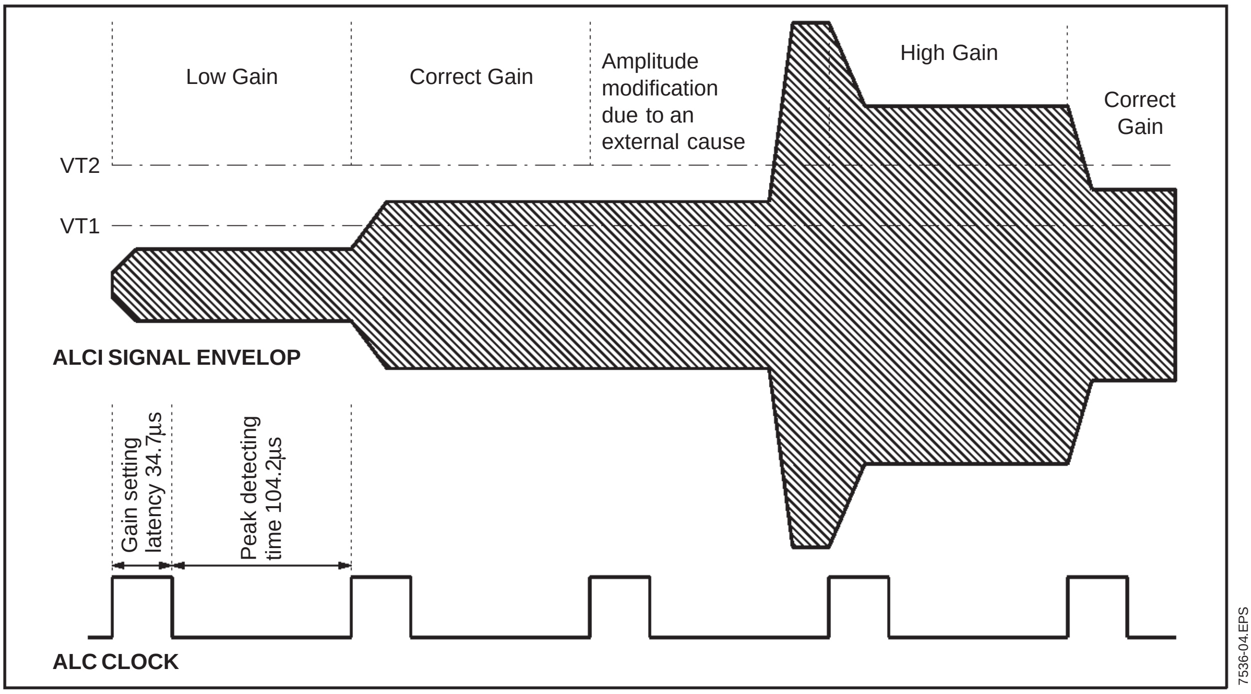
The output stage of the Tx path consists of an Automatic Level Control (ALC) system which keeps the output signal (ATO) amplitude independant of the line impedance variations. This ALC is a variable gain system (with 32 discrete values) controlled by an analog feed-back signal ALCI (see Figure 2).

The ALC gain range is 0dB to -26dB and gain change is clocked at 7200Hz. Gain steps are of magnitude 0.84dB typically.

A period of this clock is decomposed into a 34.7µs gain settling latency and a 104.2µs peak detecting time. The gain change is related to the result of a peak detection obtained by making a direct comparison of ALCI maximum value (during detecting time) with two threshold voltages V_{T1} and V_{T2} (see Figure 2).

- max (VALCI) < V_{T1} - The next gain is increased by 0.84dB,
- $V_{T1} \leq$ max (VALCI) $\leq V_{T2}$ - No gain change,
- V_{T2} < max (VALCI) - The next gain is decreased by 0.84dB.

Figure 2 : Automatic Level Control Timing Chart



FUNCTIONAL DESCRIPTION (continued)

2 - Receive Section

The receive section is active when $Rx/\overline{Tx}$ = 1.

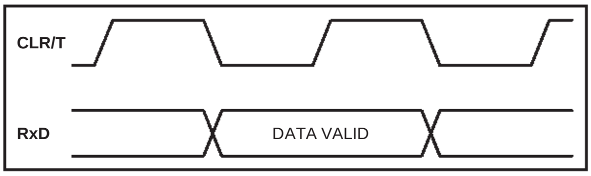
The baud rate and channel selection is also made according to Table 1.

The Rx signal is applied on RAI with a common mode voltage of 0V and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the received carrier frequency and whose bandwidth is around 6kHz. The input voltage range on RAI is $2mV_{RMS}$ - $2V_{RMS}$.

The Rx filter output is amplified by a 20dB gain stage which provides symmetrical limitations for large voltage. The resulting signal is down-converted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 2.7kHz when BRS = 0 and 5.4kHz when BRS = 1 improves the signal to noise ratio before entering the FSK demodulator. The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 (1µF ±10%, 10V) which cancels the Rx path offset voltage.

A clock recovery circuit extracts the receive clock (CLR/T) from the demodulated output (RxDEM) and delivers synchronous data (RxD) on the positive edge of CLR/T.

Figure 3 : Rx Data Output Timing



3 - Additional Digital and Analog Functions

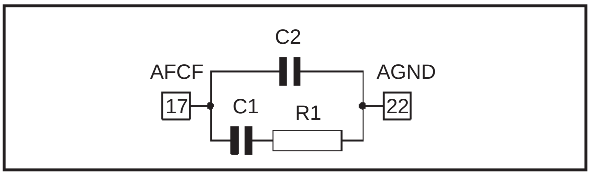
A reset intput ($\overline{RESET}$) initializes the device.

When $\overline{RESET}$ = 0, the device is in power-down mode and all the internal logic is reset. When $\overline{RESET}$ = 1, the device is active.

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 depending on the crystal characteristic typically 22pF ±10% for proper operation. It is also possible to provide directly the clock on pin XTAL1 ; in this case C3 and C4 should be removed.

An Automatic Frequency Control (AFC) Section adjusts the central frequency of Rx and Tx band-pass filter to the carrier central frequency. The stability of the AFC loop is ensured by an external compensation network C1 (470nF ±10%, 10V), C2 (47nF ±10%, 10V) and R1 (1.5kΩ ±5%) connected to pin AFCF.

Figure 4 : Automatic Frequency Loop Filter



4 - Testing Features

- An additionnal amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter (TxFI) is available and selected when TEST4 = 1.
- The 3 second normal duration of the Tx to Rx mode automatic switching is reduced to 1.48ms when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is desactivated and the functional mode of the circuit is controlled by $Rx/\overline{Tx}$ as follow : when $Rx/\overline{Tx}$ = 0 the circuit is transmitting continuously, when $Rx/\overline{Tx}$ = 1 the clock recovery block is disconnected from the FSK demodulator for testing purpose, in this configuration TEST 3 is the data input of the clock recovery block, RxDEM follow TEST3 and RxD delivers the resynchronized data.

5 - Power Supplies Wiring and Decoupling Precautions

The ST7536 has two positive power supply pins, two negative power supply pins and two ground pins in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally and require special routing precautions in order to get the best receive sensitivity performances.

The three major routing requirements are :

- The ground impedance should be as low as possible, for this purpose the AGND an DGND terminals can be connected via a local plane.
- The positive and negative power supplies (AV_{DD}, DV_{DD}, AV_{SS}, DV_{SS}) should be star-connected, avoiding common current path for the digital and analog power supplies terminals.
- Five decoupling capacitors located as close as possible to the power supply terminals should be used. Two 2.2µF tantalum and two 100nF ceramic capacitors perform the main decoupling function in the vicinity of the analog power supplies and a 100nF ceramic capacitor in the vicinity of the positive digital power supply is used to reduce the high frequency perturbations generated by the logic part of the circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}/DV_{DD}	Positive Supply Voltage (1)	-0.3, +7	V
AV_{SS}/DV_{SS}	Negative Supply Voltage (1)	-7, +0.3	V
$V_{AGND/DGND}$	Voltage between AGND and DGND	-0.3, +0.3	V
V_I	Digital Input Voltage	DGND-0.3, DV_{DD}+0.3	V
V_O	Digital Output Voltage	DGND-0.3, DV_{DD}+0.3	V
I_O	Digital Output Current	-5, +5	mA
V_i	Analog Input Voltage	AV_{SS}-0.3, AV_{DD}+0.3	V
V_o	Analog Output Voltage	AV_{SS}-0.3, AV_{DD}+0.3	V
I_o	Analog Output Current	-5, +5	mA
P_D	Power Dissipation	500	mW
T_{oper}	Operating Temperature	- 25, + 70	^oC
T_{stg}	Storage Temperature	- 65, + 150	^oC

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Notes : 1. The voltages are referenced to AGND and DGND.
2. Latch-up problems can be overcome with 2 reverse biased schottky diodes connected respectively between A/DV_{DD} & A/DGND and A/DV_{SS} & A/DGND.
3. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied.

GENERAL ELECTRICAL CHARACTERISTICS

The test conditions are A/DV_{DD} = +5V, A/DV_{SS} = -5V, A/DGND = 0V,
T_{amb} = -10 to 70^{o}C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV_{DD}/DV_{DD}	Positive Supply Voltage		4.75	5	5.25	V
AV_{SS}/DV_{SS}	Negative Supply Voltage		-5.25	-5	-4.75	V
$AI_{DD} + DI_{DD}$	Positive Supply Current in Tx Mode	$\overline{\text{RESET}}$ = 1, RX/$\overline{\text{Tx}}$ = 0		30	35	mA
$AI_{DD} + DI_{DD}$	Positive Supply Current in Rx Mode	$\overline{\text{RESET}}$ = 1, RX/$\overline{\text{Tx}}$ = 1		29	34	mA
$AI_{SS} + DI_{SS}$	Negative Supply Current in Tx Mode	$\overline{\text{RESET}}$ = 1, RX/$\overline{\text{Tx}}$ = 0	- 34	- 29		mA
$AI_{SS} + DI_{SS}$	Negative Supply Current in Rx Mode	$\overline{\text{RESET}}$ = 1, RX/$\overline{\text{Tx}}$ = 1	- 33	- 28		mA
$AI_{DD} + DI_{DD}$	Positive Power-down Current	$\overline{\text{RESET}}$ = 0, RX/$\overline{\text{Tx}}$ = 1 XTAL1 = 1			1.2	mA
$AI_{SS} + DI_{SS}$	Negative Power-down Current		- 1.2			mA
V_{IH}	High Level Input Voltage	Digital inputs except XTAL1	2.2			V
V_{IL}	Low Level Input Voltage	Digital inputs			0.8	V
V_{OH}	High Level Output Voltage	Digital outputs, I_{OH} = - 400µA	2.4			V
V_{OL}	Low Level Output Voltage	Digital outputs, I_{OL} = 1.6mA			0.4	V
V_{IH}	High Level Input Voltage	XTAL1 input	3.6			V
DC	XTAL1 Clock Duty Cycle	External clock	40		60	%

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TRANSMITTER ELECTRICAL CHARACTERISTICS

The test conditions are A/DV$_{DD}$ = +5V, A/DGND = 0V, A/DV$_{SS}$ = -5V,
T_{amb} = -10 to +70^{o}C unless othewise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TAC}	Max Carrier Output AC Voltage	R_L = 2kΩ, $V_{ALCI} < V_{T1}$	2.8	3.2	3.7	V_{PP}
HD2	Second Harmonic Distortion	R_L = 2kΩ, $V_{ALCI} < V_{T1}$			0.32	%
FD	FSK Peak-to-peak Deviation	BRS = 0 BRS = 1		600 1200		Hz Hz
TRxTx	Carrier Activation Time	After Rx/$\overline{Tx}$ 1 → 0 transition			1	ms
TALC	Carrier Stabilisation Time	ALC maximum settling time, 32 gain steps			5	ms
DRNG	ALC Dynamic Range		25	26	27	dB
VT1	ALC Low Threshold Voltage		1.81	1.87		V
VT2	ALC High Threshold Voltage			2.12	2.18	V
GST	ALC Gain Step			0.84		dB
PSRR1 PSRR2	Power supply rejection ratio on ATO (see Note 1)	V_{IN} = 200mV$_{PP}$, f_{IN} = 50Hz on V_{DD} or V_{SS}	35 10			dB dB

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Note 1 : This characteristic is guaranteed by correlation.

RECEIVER ELECTRICAL CHARACTERISTICS

The test conditions are A/DV$_{DD}$ = +5V, A/DGND = 0V, A/DV$_{SS}$ = -5V,
T_{amb} = -10 to +70^{o}C unless othewise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Maximum Input Signal				2	V_{RMS}
R_{IN}	Input Impedance		100			kΩ
RCJ	Recovered Clock Jitter	Percentage of the nominal clock	- 5		+ 5	%
PSRR1 PSRR2	Power supply rejection ratio on RxFO (see Note 1)	V_{IN} = 200mV$_{PP}$, f_{IN} = 50Hz on V_{DD} or V_{SS}	35 10			dB dB
 V_{IN0} V_{IN1}	Rx sensitivity (see Note 1)	Typical measured BER < 10^{-5} BRS = 0 BRS = 1			 2 3	mV$_{RMS}$
 BER1 BER2	Bit error rate at minimum Rx signal (see Note 1)	White Noise, S/N = 15dB RAI = 2mV$_{RMS}$, BRS = 0 RAI = 3mV$_{RMS}$, BRS = 1		 $2 \cdot 10^{-5}$ $3 \cdot 10^{-4}$	 10^{-3} 10^{-3}	
BER3	Bit error rate at maximum Rx signal (see Note 1)	RAI = 2V$_{RMS}$, White Noise, S/N = 25dB		10^{-7}	10^{-3}	
BER4	Bit error rate at medium Rx signal (see Note 1)	RAI= 0.6V$_{RMS}$, S/N= 15dB		10^{-6}	10^{-3}	
BER5	Bit error rate with impulsive noise (see Note 1)	RAI = 90mV$_{RMS}$, N = 5V$_{PP}$ pulse wave, f = 100Hz, duty cycle = 10%			10^{-3}	
  BER6 BER7	Bit error rate with modulated sinusoidal noise Ns (see Note 1)	S+ Ns < 0.2V$_{RMS}$, Ns = sine carrier with 80% AM modul., f_m = 1kHz, See Figure 5 S_{min} = 2mV$_{RMS}$, BRS = 0 S_{min} = 3mV$_{RMS}$, BRS = 1			 10^{-3} 10^{-3}	

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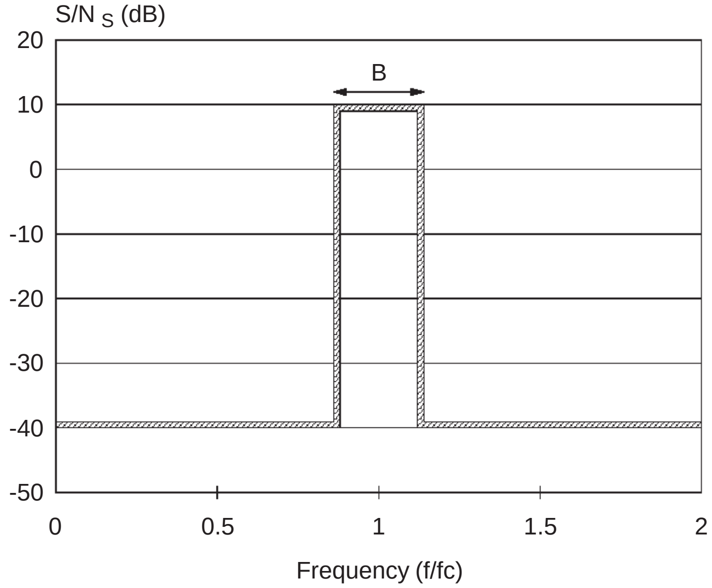
Note 1 : This characteristic is guaranteed by correlation

Figure 5 : S/N Mask for 80% AM Sine Noise



B = 20kHz at 600 Bit/s (BRS = 0)
B = 40kHz at 1200 Bit/s -BRS = 1)

fc : Central Carrier Frequency

7536-07.EPS

FILTER TEMPLATES

Frequency (kHz)	Test Conditions	Amplitude (dB)		
		Min.	Typ.	Max.
RECEIVE AND TRANSMIT FILTER				
54	BRS = 0, CHS = 0			- 35
79.05		- 4	- 3	- 2
Ref 82.05			0	
85.05		- 4	- 3	- 2
123				- 35
44.4	BRS = 0, CHS = 1			- 35
65		- 4	- 3	- 2
Ref 67.46			0	
69.93		- 4	- 3	- 2
101.13				- 35
47.57	BRS = 1, CHS = 0			- 35
69.64		- 4	- 3	- 2
Ref 72.28			0	
74.92		- 4	- 3	- 2
108.36				- 35
57.08	BRS = 1, CHS = 1			- 35
83.57		- 4	- 3	- 2
Ref 86.74			0	
89.91		- 4	- 3	- 2
130.03				- 35

Frequency (kHz)	Test Conditions	Amplitude (dB)		
		Min.	Typ.	Max.
INTERMEDIATE FREQUENCY FILTER				
1.2	BRS = 0			- 35
2.15		- 5	- 3	- 2
Ref 2.7			0	
3.25		- 5	- 3	- 2
5.8				- 35
2.4	BRS = 1			- 35
4.3		- 5	- 3	- 2
Ref 5.4			0	
6.5		- 5	- 3	- 2
11.6				- 35

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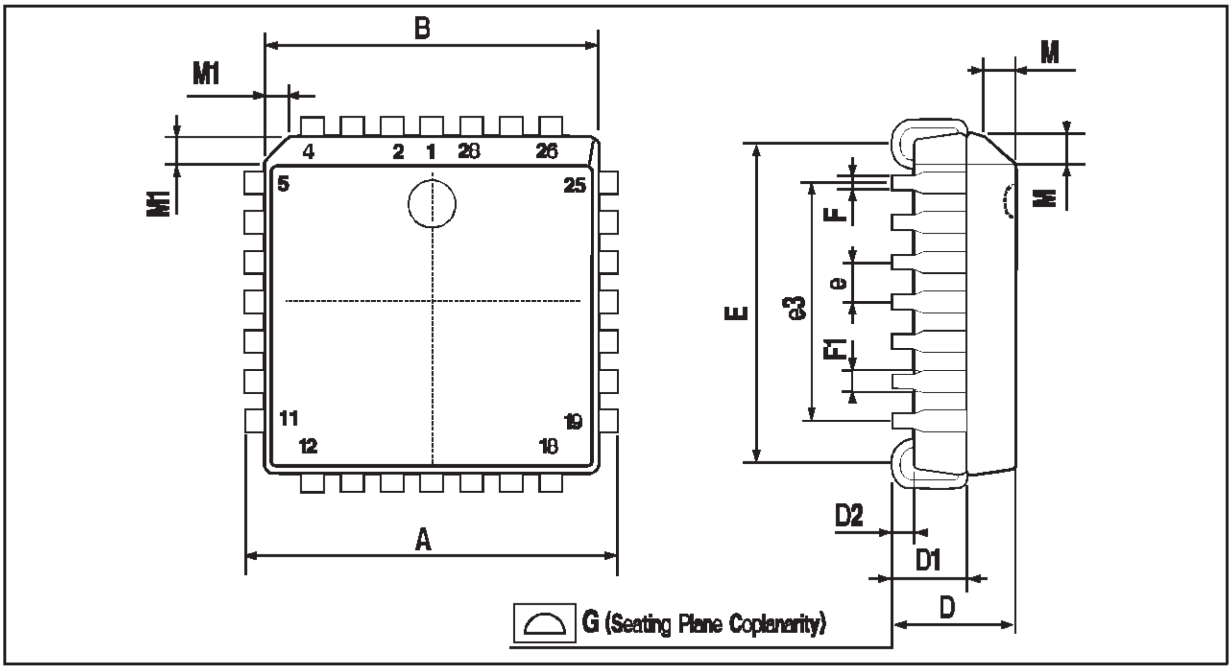
PACKAGE MECHANICAL DATA

28 PINS - PLASTIC LEADED CHIP CARRIER (PLCC)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

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