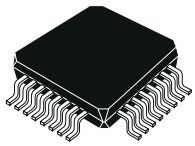
# L4992

## TRIPLE OUTPUT POWER SUPPLY CONTROLLER

- DUAL PWM BUCK CONTROLLERS (3.3V and 5.1V)
- 12V/120mA LINEAR REGULATOR
- DUAL SYNCH RECTIFIERS DRIVERS
- 96% EFFICIENCY ACHIEVABLE
- 50µA (@ 12V) STAND BY CONSUMPTION
- 5.5V TO 25V SUPPLY VOLTAGE
- EXCELLENT LOAD TRANSIENT RESPONSE
- DISABLE PULSE SKIPPING FUNCTION
- POWER MANAGEMENT:
  - UNDER AND OVERVOLTAGE OUTPUT DETECTION
  - POWER GOOD SIGNAL
  - SEPARATED DISABLE
- THERMAL SHUTDOWN
- PACKAGE: TQFP32



**TQFP32**

**ORDERING NUMBER: L4992**

### APPLICATION

- NOTEBOOK AND SUBNOTEBOOK COMPUTERS
- PEN TOP AND PORTABLE EQUIPMENT
- COMMUNICATING COMPUTERS

### DESCRIPTION

The L4992 is a sophisticated dual PWM step-down controller and power monitor intended for Notebook computer and/or battery powered equipment. The device produces regulated +3.3V, +5.1V and 12V supplies for use in portable and PCMCIA applications.

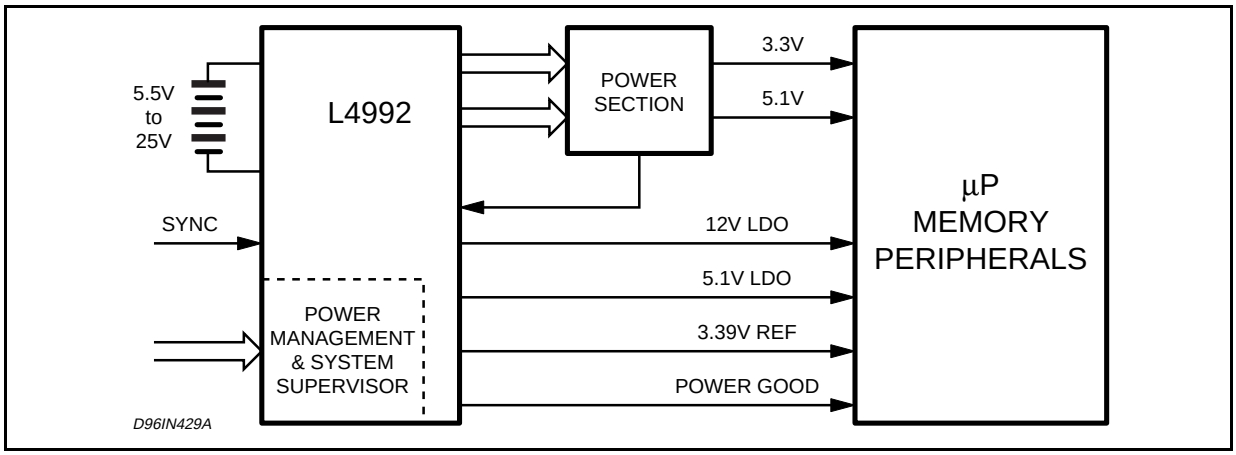
The internal architecture allows to operate with minimum external components count. A very high switching frequency (200/300 KHz or externally synchronizable) optimizes their physical dimensions.

Synchronous rectification and pulse skipping mode for the buck sections optimise the overall efficiency over a wide load current range (96% efficiency @1A/5.1V and 93% efficiency @ 0.05A/5.1V.

The two high performance PWM controllers for +3.3V and +5.1V lines are monitored for overvoltage, undervoltage and overcurrent conditions. On detection of a fault, a POWER GOOD signal is generated and a specific shutdown procedure takes place to prevent physical damage and data corruption.

A disable function allows to manage the output power sections separately, optimising the quiescent consumption of the IC in stand-by conditions.

### SYSTEM BLOCK DIAGRAM



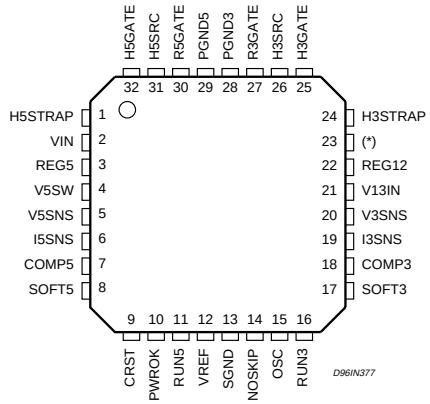
## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Power Supply Voltage on $V_{IN}$ | 0 to 25 | V |
| $V_I$ | Maximum Pin Voltage to Pins 1, 24, 25, 32 | -0.5 to ($V_{IN}$ +5) | V |
| $I_{IN}$ | Input Current Except V13IN and $V_{IN}$ | -1 to +1 | mA |
| $I_{OUT}$ | Output Current Digital Output | -15 to +15 | mA |
| $T_J$ | Junction Temperature | -55 to 150 | °C |

## THERMAL DATA

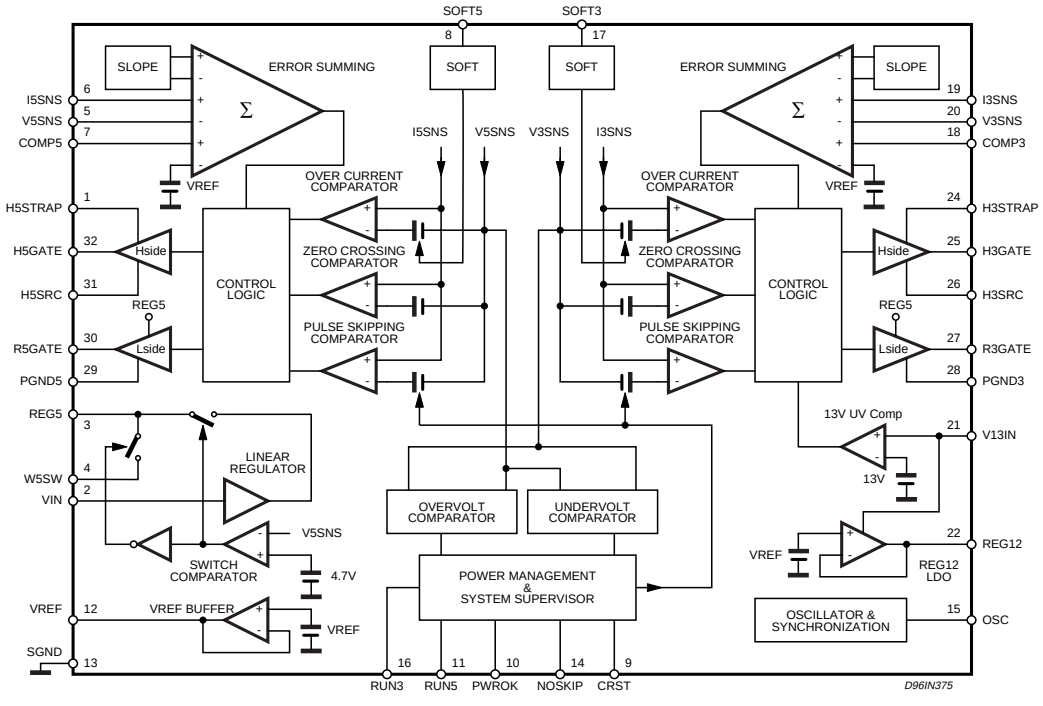
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{TH\ J\text{-}amb}$ | Thermal Resistance Junction -Ambient | 60 | °C/W |

## PIN CONNECTION (Top view)




(*)TO BE CONNECTED TO PIN13

## BLOCK DIAGRAM



## PIN FUNCTIONS

| N. | Name | Description |
|---|---|---|
| 1 | H5STRAP | +5.1V section bootstrap capacitor connection |
| 2 | $V_{IN}$ | Device supply voltage. From 5.5 to 25V |
| 3 | REG5 | +5V regulator supply. Used mainly for bootstrap capacitors. It should be bypassed to ground. |
| 4 | V5SW | Alternative device supply voltage. When the +5.1V section is operating, the device is no longer powered through $V_{IN}$ but through this pin. |
| 5 | V5SNS | This pin connects to the (-) input of the +5.1V internal current sense comparator |
| 6 | I5SNS | This pin connects to the (+) input of the +5.1V internal current sense comparator |
| 7 | COMP5 | Feedback input for the +5.1V section. |
| 8 | SOFT5 | Soft-start input of the +5.1V section. The soft-start time is programmed by an external capacitor connected between this pin and SGND. Approximately, 1ms/nF @ full load. |
| 9 | CRST | Input used for start-up and shut-down timing. A capacitor defines a time of 2ms/nF. |
| 10 | PWROK | Power-good diagnostic signal. This output is driven high when both switching sections are enabled and running properly, after a delay defined by the CRST capacitor. |
| 11 | RUN5 | Control input to enable/disable the 5.1V section. A high level (>2.4V) enables this section, a low level (<0.8V) shuts it down |
| 12 | VREF | Internal +3.39V high accuracy voltage generator. It can source 5mA to external load. Bypass to ground with a 4.7µF capacitor to reduce noise. |
| 13 | SGND | Signal ground. Reference for internal logic circuitry. It must be routed separately from high current returns. |
| 14 | NOSKIP | Pulse skipping mode control. A high level (>2.4V) disables pulse skipping at low load current, a low level (<0.8V) enables it. |
| 15 | OSC | Oscillator frequency control: connect to 2.5V to select 300KHz operation, to ground or to 5V for 200KHz operation. A proper external signal can synchronize the oscillator |
| 16 | RUN3 | Control input to enable/disable the +3.3V section. A high level (>2.4V) enables this section, a low level (>0.8V) shuts it down. |
| 17 | SOFT3 | Soft-start input for the 3.3V section. The soft-start time is programmed by an external capacitor connected between this pin and GND. Approximately, 1ms/nF @full load. |
| 18 | COMP3 | Feedback input for the +3.3V section |
| 19 | I3SNS | This pin connects to the (+) input of the +3.3V internal current sense comparator |
| 20 | V3SNS | This pin connects to the (-) input of the +3.3V internal current sense comparator |
| 21 | V13IN | 12V regulator input supply voltage, included between 13 and 20V. This voltage can be supplied by a flyback winding on +3.3V inductor |
| 22 | REG12 | 12V regulator output voltage. It can source up to 150mA to an external load |
| 23 | SGND | To be connected to pin 13 |
| 24 | H3STRAP | +3.3V section bootstrap capacitor connection |
| 25 | H3GATE | Gate- driver output for the +3.3V high-side N-MOS |
| 26 | H3SRC | +3.3V high-side N-MOS source connection |
| 27 | R3GATE | Gate- driver output for the +3.3V low- side N-MOS (synchronous rectifier). |
| 28 | PGND3 | Current return for +3.3V section drivers |
| 29 | PGND5 | Current return for +5.1V section drivers |
| 30 | R5GATE | Gate-driver output for the +5.1V low-side N-MOS (synchronous rectifier). |
| 31 | H5SRC | +5.1V high-side N-MOS source connection |
| 32 | H5GATE | Gate-driver output for the +5.1V high-side N-MOS |

**ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = 12V; $T_J$ = 25°C; $V_{OSC}$ = GND; unless otherwise specified.)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $V_{IN}$ | Input Supply Voltage | | 5.5 | | 25 | V |
| $I_2$ | Operating Quiescent Current | R5GATE = R3GATE = OPEN<br>H5GATE = H3GATE = OPEN<br>RUN3 = RUN5 = REG5<br>(DRIVERS OFF) | | | 1.35 | mA |
| $I_2$ | Stand-By Current | RUN3 = RUN5 = GND<br>$V_{IN}$ = 12V<br>$V_{IN}$ = 20V | | 50<br>60 | 100<br>120 | µA |
| **+5.1V PWM CONTROLLER SECTION** | | | | | | |
| $V_{5OUT}$ (*) | V5SNS Feedback Voltage | $V_{IN}$ = 5.5 to 20V;<br>$V_{I5SNS}$ - $V_{V5SNS}$ = 0 to 70mV | 4.85 | 5.13 | 5.25 | V |
| $V_6$ - $V_5$ | Over-Current Threshold Voltage | VSOFT5 = 4V | 80 | 100 | 120 | mV |
| $V_6$ - $V_5$ | Pulse Skipping Mode Thereshold Voltage | $V_{IN}$ > 6.8V | 14 | 26 | 38 | mV |
| | | $V_{IN}$ < 5.8V | 7 | 13 | 19 | mV |
| $V_5$ | Over Voltage Threshold ON V5SNS | | 5.35 | 5.55 | 5.77 | V |
| | Under Voltage Threshold ON V5SNS | | 4.54 | 4.69 | 4.87 | V |
| **+3.3V PWM CONTROLLER SECTION** | | | | | | |
| $V_{3OUT}$ (*) | V3SNS Feedback Voltage | $V_{IN}$ = 5.5 to 20V;<br>$V_{I3SNS}$ - $V_{V3SNS}$ = 0 to 70mV | 3.285 | 3.39 | 3.495 | V |
| $V_{19}$ - $V_{20}$ | Over Current Threshold Voltage | VSOFT3 = 4V | 80 | 100 | 120 | mV |
| $V_{19}$ - $V_{20}$ | Pulse Skipping Mode Threshold Voltage | $V_{IN}$ = 5.5 to 20V; | 14 | 26 | 38 | mV |
| $V_{20}$ | Over Voltage Threshold ON V3SNS | | 3.55 | 3.7 | 3.85 | V |
| | Under Voltage Threshold ON V3SNS | | 3.02 | 3.14 | 3.27 | V |
| **PWM CONTROLLERS CHARACTERISTICS (BOTH SECTIONS)** | | | | | | |
| $F_{OSC}$ | Switching Frequency Accuracy | OSC = REG5/2 | 255 | 300 | 345 | kHz |
| | | OSC = 0 or REG5 | 170 | 200 | 230 | kHz |
| $V_{15}$ | Voltage Range for 300kHz Operation | | 2.4 | | 2.6 | V |
| $T_{OFF}$ | Dead Time | | 300 | 375 | 450 | ns |
| $T_{OV}$ | Overvoltage Propagation Time | V5SNS to PWROK or<br>V3SNS to PWROK | | | 1.25 | µs |
| $T_{UV}$ | Undervoltage Propagation Time | V5SNS to PWROK or<br>V3SNS to PWROK | | | 1.5 | µs |
| $I_8$, $I_{17}$ | Soft Start Charge Current | | 3.2 | 4 | 4.8 | µA |
| $V_8$, $V_{17}$ | Soft Start Clamp Voltage | | | 4 | | V |

(*) Guaranteed by design, not tested in production

**ELECTRICAL CHARACTERISTICS** (Continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **HIGH AND LOW SIDE GATE DRIVER (BOTH SECTIONS)** | | | | | | |
| $I_{25}$, $I_{27}$, $I_{32}$, $I_{30}$ | Source Output Peak Current | $C_{LOAD}$ = 1nF | 0.2 | 0.5 | | A |
| | Sink Output Peak Current | $C_{LOAD}$ = 1nF | 0.2 | 0.5 | | A |
| $R_H$ | $R_{DSON}$ Resistance (or Impedance) | Driver OUT HIGH | | | 7 | Ω |
| $R_L$ | $R_{DSON}$ resistance (or Impedance) | Driver OUT LOW | | | 5 | Ω |
| $V_{OH}$ | Output High Voltage | HSTRAP = REG5<br>$I_{SOURCE}$ = 10mA; HSRC = GND | 4.40 | 5.3 | 5.61 | V |
| $V_{OL}$ | Output Low Voltage | HSTRAP = REG5<br>$I_{SINK}$ = 10mA HSRC = GND | | | 0.5 | V |
| $T_{CC}$ | Cross-Conduction Delay | | 30 | 75 | 130 | ns |
| **12V LINEAR REGULATOR SECTION** | | | | | | |
| $V_{21}$ | Input Voltage Range | | 13 | | 20 | V |
| $V_{22}$ | Output Voltage | $I_{22}$ = 0 to 120mA | 11.54 | 12.0 | 12.48 | V |
| $I_{22}$ | Current Limiting | $V_{REG12}$ = 12V | 120 | | | mA |
| | Short Circuit Current | $V_{REG12}$ = 0V | 150 | | | mA |
| $V_{CP}$ | Input Voltage Clamp | $I_{CLAMP}$ = 100µA | 16 | | | V |
| | "One Shot" Activation Threshold | $V_{13IN}$ Falling | 12.88 | 13.7 | 14.52 | V |
| | "One Shot" Pulse | | | | 1.5 | µs |
| **INTERNAL REGULATOR (VREG5) AND REFERENCE VOLTAGE** | | | | | | |
| $V_3$ | VREG5 Output Voltage | $V_{IN}$ = 5.5 to 20V<br>$I_{LOAD}$ = 0 to 5mA | 4.5 | 5.3 | 5.61 | V |
| $I_3$ | Total Current Capability | VREG5 = 5.3V<br>$V_{REG5}$ = 6V | 25<br>70 | | | mA |
| | Switch-Over Threshold Voltage | | 4.3 | 4.53 | 4.7 | V |
| $V_{12}$ | Reference Voltage | | 3.35 | 3.39 | 3.43 | V |
| | | $V_{IN}$ = 5.5 to 20V<br>$I_{LOAD}$ = 1 to 5mA | 3.32 | 3.39 | 3.46 | V |
| $I_{12}$ | Source Current at Reference Voltage | | 5 | | | mA |
| **POWER GOOD AND ENABLE FUNCTION** | | | | | | |
| $V_{16}$, $V_{11}$ | RUN3, RUN5, Enable Voltage | HIGH LEVEL | 2.4 | | | V |
| $V_{16}$, $V_{11}$ | RUN3, RUN5, Disable Voltage | LOW LEVEL | | | 0.8 | V |
| $T_{10}$ | Power Good Delay | $C_{CRST}$ = 100nF | 160 | 200 | 240 | ms |
| $T_{27}$, $T_{30}$ | Shutdown Delay Time before Low Side Activation (Except Over-Voltage Fault) | $C_{CRST}$ = 100nF, | 160 | 200 | 240 | ms |
| | CRST Timing Rate | | | 2 | | ms/nF |
| | Power Good High Level | $I_{PWROK}$ = 40µA | 4.1 | | | V |
| | Power Good LowLevel | $I_{PWROK}$ = 320µA | | | 0.4 | V |
| **SYNCHRONIZATION** | | | | | | |
| | Synchronisation Pulse Width | | 400 | | | ns |
| | Synchronisation Input Voltage (Falling Edge Transition) | | 5 | | | V |

## DETAILED FUNCTIONAL DESCRIPTION

In the L4992 block diagram six fundamental functional blocks can be identified:

- 3.3V step-down PWM switching regulator (pins 17 to 20, 24 to 27).
- 5.1V step-down PWM switching regulator (pins 1, 4 to 8, 30 to 32).
- 12V low drop-out linear regulator (pins 21,22).
- 5V low drop-out linear regulator (pin 3).
- 3.3V reference voltage generator (pin 12).
- Power Management section (pins 9 to 11, 14,16).

The chip is supplied through pin VIN (2), typically by a battery pack or the output of an AC-DC adapter, with a voltage that can range from 5.5 to 25V. The return of the bias current of the device is the signal ground pin SGND (13), which references the internal logic circuitry.

The drivers of the external MOSFET's have their separate current return for each section, namely the power ground pins PGND3 (28) and PGND5 (29). Take care of keeping separate the routes of signal ground and the two power ground pins when laying out the PCB (see "Layout and grounding" section).

The two PWM regulators share the internal oscillator, programmable or synchronizable through pin OSC (15).

### +3.3V AND +5.1V PWM REGULATORS

Each PWM regulator includes control circuitry as well as gate-drive circuits for a step-down DC-DC converter in buck topology using synchronous rectification and current mode control.

The two regulators are independent and almost identical. As one can see in the Block Diagram, they share only the oscillator and the internal supply and differ for the pre-set output voltages and for the control circuit that links the +3.3V section to the operation of the 12V linear regulator (see the relevant section).

Each converter can be turned on and off independently: RUN3 and RUN5 are control inputs which disable the relevant section when a low logic level (below 0.8 V) is applied and enable its operation with a high logic level (above 2.4 V). When both inputs are low the device is in stand-by condition and its current consumption is extremely reduced (less than 120µA over the entire input voltage range).

#### Oscillator

The oscillator, which does not require any external timing component, controls the PWM switching frequency. This can be either 200 or 300 kHz, depending on the logic state of the control pin OSC, or else can be synchronized by an external oscillator.

If OSC is grounded or connected to pin REG5 (5V) the oscillator works at 200kHz. By connecting OSC to a 2.5 V voltage, 300 kHz operation will be selected. Instead, if pin OSC is fed with an external signal like the one shown in fig. 1, the oscillator will be synchronized by its falling edges.

Considering the spread of the oscillator, synchronization can be guaranteed for frequencies above 230kHz. Even though a maximum frequency value is in practice imposed by efficiency considerations it should be noticed that increasing frequency too much arises problems (noise, subharmonic oscillation, etc.) without significant benefits in terms of external component size reduction and better dynamic performance.

The oscillator imposes a time interval (300 ns min.), during which the high-side MOSFET is definitely OFF, to recharge the bootstrap capacitor (see "MOSFET's Drivers" section). This, implies a limit on the maximum duty cycle (88.5% @ fsw = 300kHz, 92.6% @ fsw = 200kHz, worst case) which, in turn, imposes a limit on the minimum operating input voltage.

#### PWM regulation

The control loop does not employ a traditional error amplifier in favour of an error summing comparator which sums the reference voltage, the feedback signal, the voltage drop across an external sense resistor and a slope compensation ramp (to avoid subharmonic oscillation with duty cycles greater then 50%) with the appropriate signs.

The output latch of both controllers is set by every pulse coming from the oscillator. That turns off the low-side MOSFET (synchronous rectifier) and, after a short delay (typ. 75 ns) to prevent cross-conduction, turns on the high-side one, thus allowing energy to be drawn from the input source and stored in the inductor.

**DETAILED FUNCTIONAL DESCRIPTION** (continued)
**Figure 1:** Synchronization signal and operation.

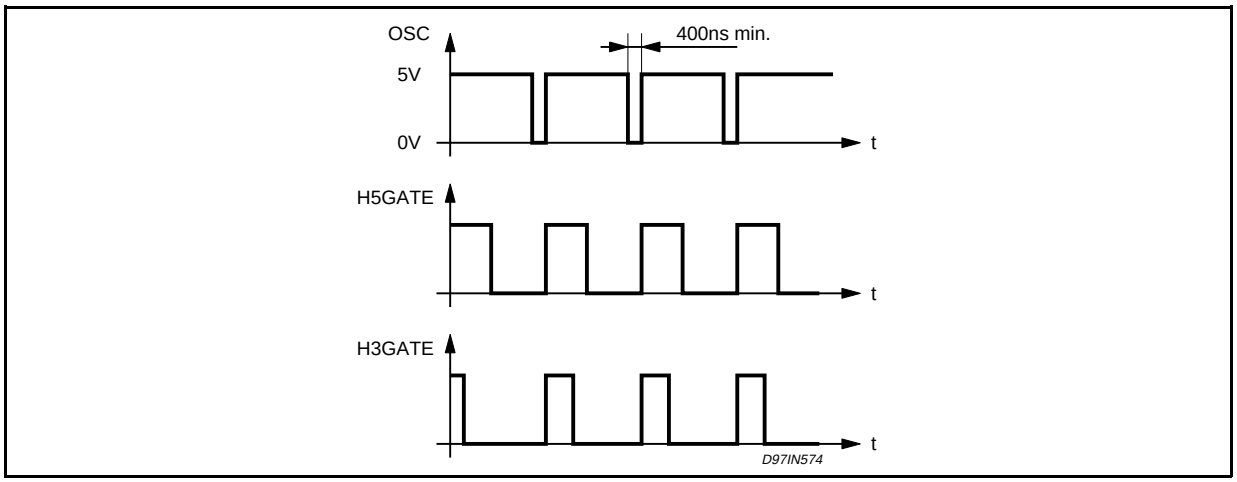
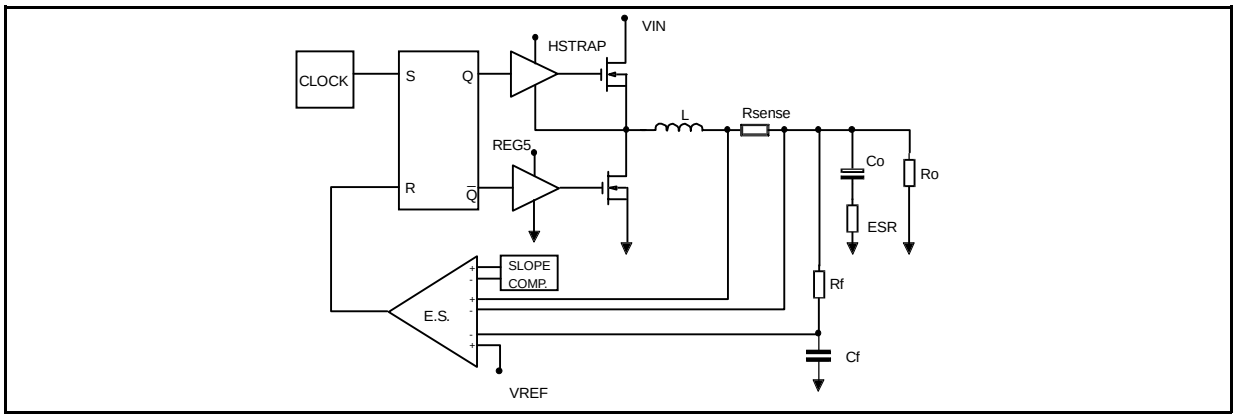



**Figure 2:** L4992 Control Loop.




The error summing, by comparing the above mentioned signals, determines the moment in which the output latch is to be reset. The high-side MOSFET is then turned off and the synchronous rectifier is turned on after the appropriate delay (typ. 75 ns), thus making the inductor current recirculate. This state is maintained until the next oscillator pulse.

With reference to the schematic of fig. 2, the open-loop transfer function of such a kind of control system, under the assumption of an ideal slope compensation, is:

$$F(s) = A \cdot \frac{R_O}{R_{sense}} \cdot \frac{1 + s \cdot ESR \cdot C_O}{(1 + s \cdot R_O C_O) \cdot (1 + s \cdot R_F C_F)}$$

where A is the gain of the error summing comparator, which is 2 by design.

The system is inherently very fast since it tends to correct output voltage deviations nearly on a cycle-by-cycle basis. Actually, in case of line or load changes, few switching cycles can be sufficient for the transient to expire.

The operation above illustrated is modified during particular or anomalous conditions. Leaving out other circumstances (described in "Protections" section) for the moment, consider when the load current is low enough or during the first switching cycles at start-up: the inductor current may become discontinuous, that is it is zero during the last part of each cycle. In such a case, a "zero current comparator" detects the event and turns off the synchronous rectifier, avoiding inductor current reversal and reproducing the natural turn-off of a diode when reverse biased. Both MOSFET's stay in off state until the next oscillator pulse.

**DETAILED FUNCTIONAL DESCRIPTION** (continued)

**Synchronous rectification.**

Very high efficiency is achieved at high load current with the synchronous rectification technique, which is particularly advantageous because of the low output voltage. The low-side MOSFET, that is the synchronous rectifier, is selected with a very low on-resistance, so that the paralleled Schottky diode is not turned on, except for the small time in which neither MOSFET is conducting. The effect is a considerable reduction of power loss during the recirculation period.

Although the Schottky might appear to be redundant, it is not in a system where a very high efficiency is required. In fact, its lower threshold prevents the lossy body-diode of the synchronous rectifier MOSFET from turning on during the above mentioned dead-time. Both conduction and reverse recovery losses are cut down and efficiency can improve of 1-2% in some cases. Besides a small diode is sufficient since it conducts for a very short time.

As for the 3.3V section only, the synchronous rectifier is also involved in the 12 V linear regulator operation (see the relevant section). See also the "Power Management" to see how both synchronous rectifiers are used to ensure zero voltage output in stand-by conditions or in case of overvoltage.

**Pulse-skipping operation.**

To achieve high efficiency at light load current as well, under this condition the regulators change their operation (unless this feature is disabled): they abandon PWM and enter the so-called pulse-skipping mode, in which a single switching cycle takes place every many oscillator periods.

The "light load condition" is detected when the voltage across the external sense resistor ($V_{Rsense}$) does not exceed 26mV while the high-side MOSFET is conducting. When the reset signal of the output latch comes from the error summing comparator while $V_{Rsense}$ is below this value, it is ignored and the actual reset is driven as soon as $V_{Rsense}$ reaches 26mV. This gives some extra energy that maintains the output voltage above its nominal value for a while. The oscillator pulses now set the output latch only when the feedback signal indicates that the output voltage has fallen below its nominal value. In this way, most of oscillator pulses is skipped and the resulting switching frequency is much lower, as expressed by the following relationship:

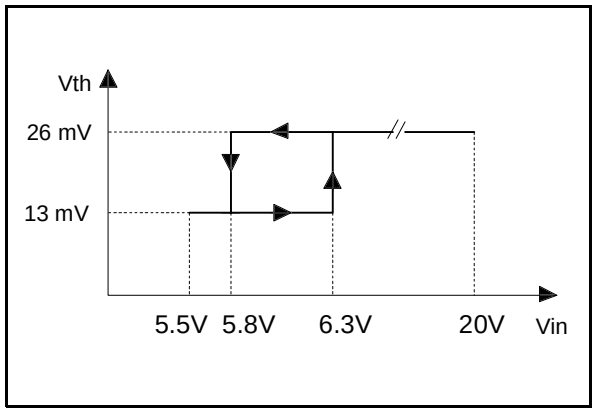
$$f_{ps} = K \cdot \frac{R_{sense}^2}{L} \cdot I_{out} \cdot V_{out} \cdot \left(1 - \frac{V_{out}}{V_{in}}\right)$$

where $K = 3.2 \cdot 10^3$ and $f_{ps}$ is in Hz. As a result, the losses due to switching and to gate-drive, which mostly account for power dissipation at low output power, are considerably reduced.

The +5.1V section can work with the input voltage very close to the output one, where the current waveform may be so flat to prevent pulse-skipping from being activated. To avoid this, the pulse-skipping threshold (of the +5.1V section only) is roughly halved at low input voltages, as shown in fig. 3. Under this condition, in the above formula the constant K becomes $12.8 \cdot 10^3$.

When in pulse-skipping, the output voltage is some ten mV higher than in PWM mode, just because of its mode of operation. If this "load regulation" effect is undesirable for any reason, the pulse skipping feature can be disabled (see "Power Management" section) to the detriment of efficiency at light load.

**Figure 3:** Pulse-skipping threshold vs. input voltage (+5.1V section only).




**MOSFET's drivers**

To get the gate-drive voltage for the high-side N-channel MOSFET a bootstrap technique is employed. A capacitor is alternately charged through a diode from the 5V REG5 line when the high-side MOSFET is OFF and then connected to its gate-source leads by the internal floating driver to turn the MOSFET on. The REG5 line is used to drive the synchronous rectifier as well, and therefore the use of low-threshold

**DETAILED FUNCTIONAL DESCRIPTION** (continued)
MOSFET's (the so-called "logic-level" devices) is highly recommended.

The drivers are of "dynamic" type, which means they do not give origin to current consumption when they are in static conditions (ON or OFF), but only during transitions. This feature is aimed at minimizing the power consumption of the device even during stand-by when both low-side MOSFET's are ON.

### Protections

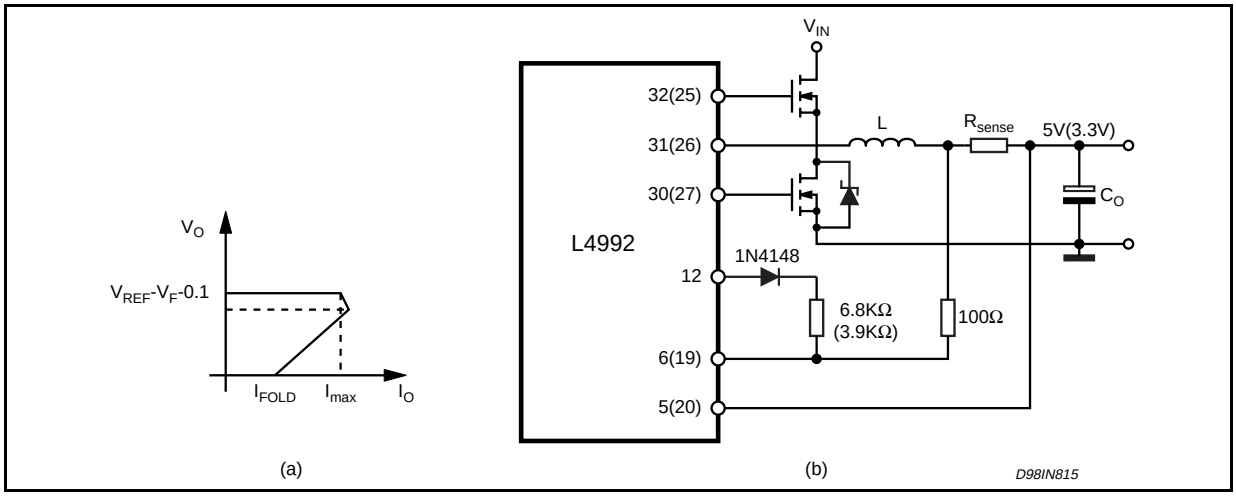
Each converter is fully protected against fault conditions. A monitoring system checks for overvoltages of the output, quickly disabling both converters in case such an event occurs. This condition is latched and to allow the device to start again either the supply voltage has to be removed or both RUN3 and RUN5 pins have to be driven low.

Undervoltage conditions are detected as well but do not cause interruption of the operation of the converters. Only PWROK signal (at pin 10) reveals the anomaly with a low output level.
If the chip overheats (above 135 °C typ.) the device stops operating as long as the temperature falls below a safe value (105 °C typ.). The overtemperature condition is signalled by a low level on PWROK as well.

A current limitation comparator prevents from excessive current in case of overload or short-circuit. It intervenes as the voltage VRsense exceeds 100 mV, turning off the high-side switch before the error summing does. By the way, this also gives the designer the ability to program the maximum operating current by selecting an appropriate sense resistor.
This pulse-by-pulse limitation gives a quasi-constant current characteristic. If a "folded back" characteristic, like the one shown in Fig. 4a, is desired the external circuit of Fig. 4b can be used. The circuits acts on the current limitation and is extremely simple and cheap. The advantage of such a technique i that a short circuit will cause a current much lower than the maximum to flow. Th e stress of the power components will be very little and no overheating will occur. The part values shown in Fig. 4b produce IFOLD = 1A in the Demo Board (see the relevant section).
Inrush current at start-up is reduced with soft-start. An external capacitor (one for each converter) is charged by an internal 4µA current generator and its linearly ramping voltage increases the setpoint of the current limit comparator, starting from zero up to the final value of 100 mV. Thus duty cycle reaches gradually its steady-state value and dangerous current peaks as well as overshoots of the output voltage are avoided.

+12 V LINEAR REGULATOR
The +12V Linear regulator is capable of delivering up to 120 mA to an external load through pin REG12. It is supplied from pin V13IN which accepts voltages included in the range of 13 to 20V.
If the application works with input voltages included between 14 and 20V, the supply for the regulator can be obtained directly from the input source. If such is not the case, the most convenient way to get the supply is to use an auxiliary winding on the 3.3 V section inductor with a catch diode, Ds, and a filter capacitor, Cs, as shown in fig. 5. This winding delivers energy to pin V13IN during the recirculation period of each switching cycle with a voltage determined by the turns ratio n and little dependent on the input voltage.

**Figure 4.**



**DETAILED FUNCTIONAL DESCRIPTION** (continued)

An auxiliary winding could be used also on the choke of the +5.1V section, either to power the +12V linear regulator or to derive a further supplemental output, however the 3.3 V section has been provided with some features aimed at ensuring a proper operation under all circumstances.

For a correct operation of the regulator, the voltage at pin V13IN must not be too low. The flyback connection of the two windings ensures a well regulated voltage, provided there is good magnetic coupling. The coupled inductors configuration, however, is not able to sustain the auxiliary voltage if the main output is lightly loaded: the secondary voltage drops and the system goes out of regulation.

To overcome this problem, when the V13IN voltage falls below a certain threshold (13.7 V +/- 5%) because of too light a load on the 3.3V section, the relevant synchronous rectifier is turned on for 1.5 µs max. during the interval in which the inductor current is zero ("one-shot" feature, see fig. 6). In this way, the inductor current reverses and draws from the output capacitor energy which is forward transferred to the auxiliary output.

In case the 3.3V section is working at full load and the linear regulator is lightly loaded, the voltage at pin V13IN can exceed the expected value. In fact, Ds and Cs act as a peak-holding circuit and V13IN is influenced by the voltage spikes at switching transients. An internal clamp limits the voltage but, in case of intervention, the chip power dissipation will rise.

When the 3.3V regulator is disabled, the linear regulator is disabled as well and is placed in a low-power mode to reduce device consumption.

**Figure 5:** 12V regulator supply with auxiliary winding.

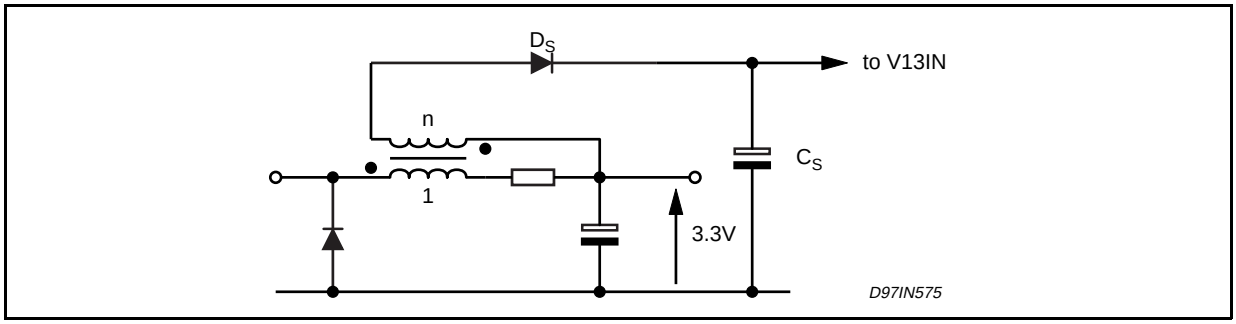
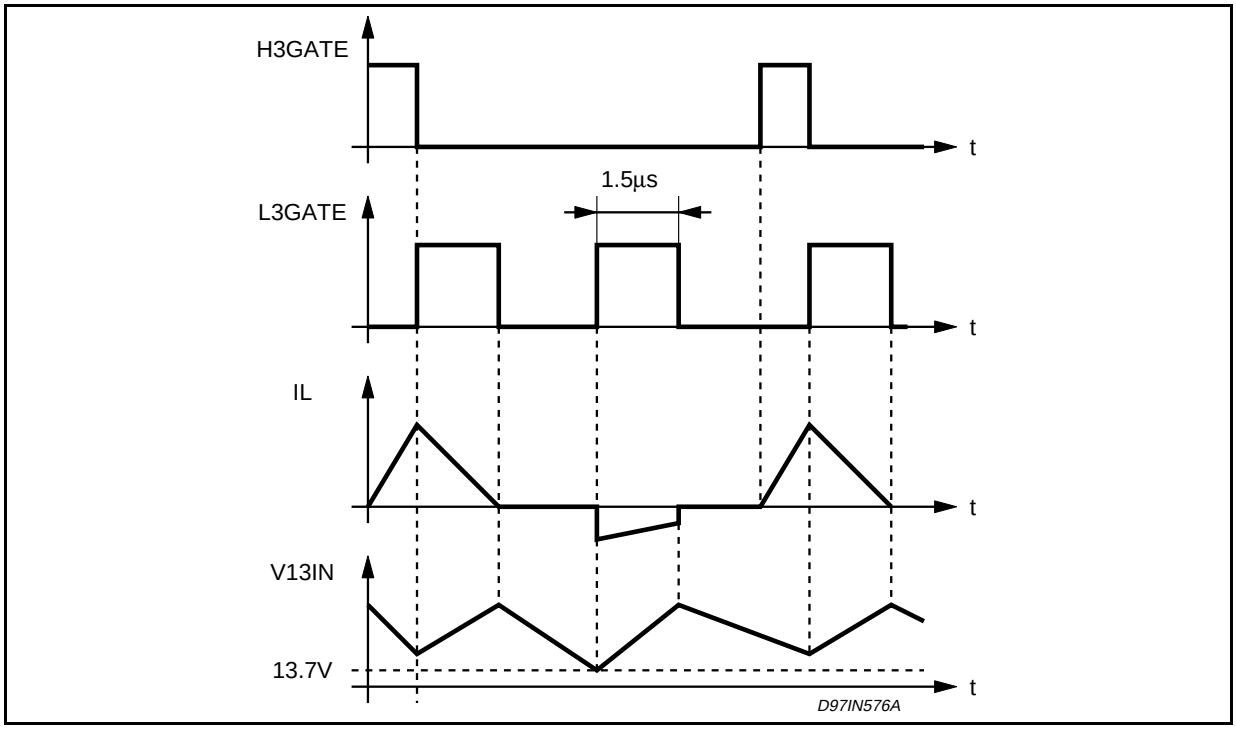



**Figure 6:** "One shot" feature to sustain V13IN voltage.



**DETAILED FUNCTIONAL DESCRIPTION** (continued)

+5 V LINEAR REGULATOR & +3.3 V REFERENCE VOLTAGE GENERATOR

This low drop-out regulator powers almost all the internal circuitry, that is the +3.3V reference voltage generator, amplifiers, comparators, digital logic, and MOSFET drivers. Its output is externally available through pin REG5.

The typical external use of this generator is to charge the bootstrap capacitors used to produce the gate-drive voltage for the high-side MOSFET's of both PWM converters.

At start-up and when the 5V section is not operating, this regulator is powered by the chip input voltage. To reduce power consumption, the linear regulator is turned off and the REG5 pin is internally connected to the 5V PWM regulator output via V5SW pin, when the 5V PWM regulator is active and its output voltage is above the switchover threshold, 4.5V.

The 5V regulator is always active, even if both PWM regulators are disabled, as long as power is applied to the chip.

The 3.3V reference voltage generator, which is active only when either PWM converter is enabled, provides comparison levels for threshold detection and device operation. It is allowed to source up to 5mA to an external load from its buffered output, externally available through pin VREF.

If either REG5 or VREF does not deliver the correct voltage, the device is shut down.

POWER MANAGEMENT

The L4992 is provided with some control pins suitable to perform some functions which are commonly used or sometimes required in battery-operated equipment. Besides, it features controlled timing sequences in case of turn-on/off and device shutdown for a safe and reliable behaviour under all conditions.

As above mentioned, RUN3 and RUN5 pins allow to disable separately both PWM converters by means of logic signals (likely coming from a μP) as mentioned earlier.

NOSKIP can disable the pulse-skipping feature: when it is held high neither of the PWM regulators is allowed to enter this kind of operation.

The PWROK output signal drives low immediately when either PWM regulator output falls below its own undervoltage threshold or when either of them is disabled. It is high when both regulator run properly.

A capacitor connected between CRST and ground fixes a time, in the order of 2ms/nF, which delays the transition low-high of PWROK. This happens at start-up or after recovering an undervoltage condition, provided both RUN3 and RUN5 are high. The delay starts from the moment in which the output voltage has reached its correct value for both sections.

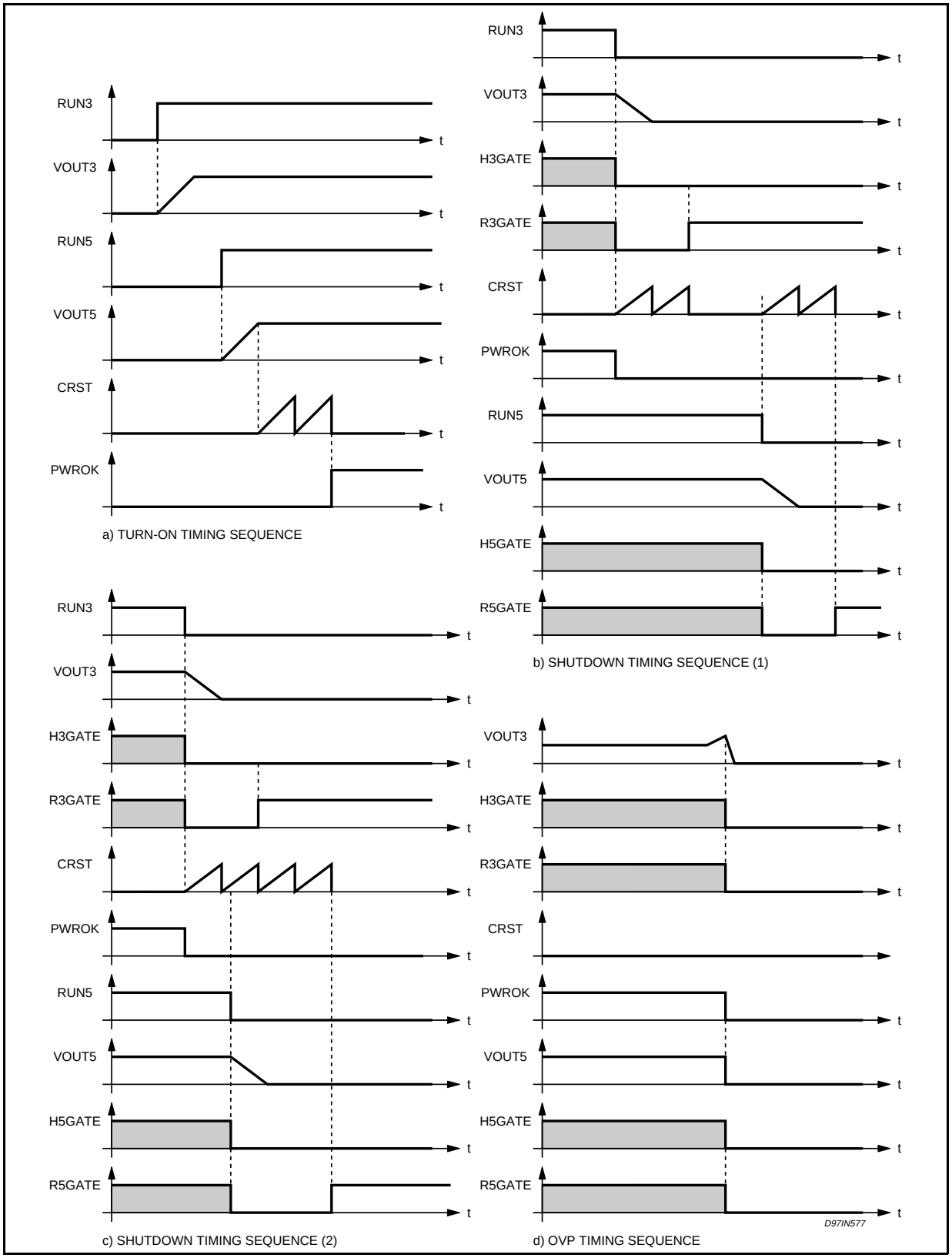
The same delay intervenes also in another circumstance: when a section is disabled (because its RUN is driven low or owing to a thermal shutdown), the relevant synchronous rectifier is turned on after the above delay in order to make sure that the load is no longer supplied.

This delay, however, does not intervene in case of overvoltage: the synchronous rectifier is immediately turned on after the shutdown, thus acting as a built-in "crowbar".

All these timing sequences are illustrated in Fig 7.

**DETAILED FUNCTIONAL DESCRIPTION** (continued)

**Figure 7:** L4992 controlled timing sequences.



## DESIGN PROCEDURE

Basically, the application circuit topology is fixed, and the design procedure concerns only the selection of the component values suitable for the voltage and current requirements of the specific application.

The design data one needs to know are therefore:

- Input voltage range: the minimum ($V_{inmin}$) and the maximum ($V_{inmax}$) voltage under which the application is expected to operate;
- Maximum load current for each of the three sections:

- $I_{out3}$ for the +3.3V section;
- $I_{out5}$ for the +5.1V section:
- $I_{out12}$ for the +12V section;

- Maximum peak-to-peak ripple amplitude of the output voltage for each switching section:

- $V_{rpp3}$ for the +3.3V section;
- $V_{rpp5}$ for the +5.1V section;

- The operating frequency $f_{sw}$ (200/300 kHz or externally synchronized).

It is worth doing some preliminary considerations. The selection of the switching frequency depends on the requirements of the application. If the aim is to minimize the size of the external components, 300 kHz will be chosen. For low input voltage applications 200 kHz is preferred, since it leads to a higher maximum duty cycle.

As for the switching regulators, the inductance value of the output filter affects the inductor current ripple: the higher the inductance the lower the ripple. This implies a lower current sense resistor value (for a given $I_{out}$), lower core losses and a lower output voltage ripple (for a given output capacitor) but, on the other hand, more copper losses and a worse transient behaviour due to load changes. Usually the maximum ripple peak-to-peak amplitude (which occurs at $V_{inmax}$) is chosen between 15% and 50% of the full load current. It is convenient to introduce a ripple factor coefficient, RF, that is therefore a number between 0.15 and 0.5.

As for the linear regulator, its input voltage $V_{inlin}$ should not fall below 13V and therefore the auxiliary winding should be dimensioned to get this voltage with a certain margin (say, 14V). Conversely, an higher input voltage leads to higher losses inside the regulator, to the detriment of efficiency, and to higher total current on the +3.3V inductor. Besides it implies a higher turns ratio and therefore a worse magnetic coupling, which affect energy transfer during flyback.

### SWITCHING REGULATORS

#### +5.1V Inductor

To define the inductor, it is necessary to determine firstly the inductance value. Its minimum value is given by:

$$L_{5min} = \frac{5.1 \cdot (V_{in\,max} - 5.1)}{V_{in\,max} \cdot f_{sw} \cdot I_{out5} \cdot RF}$$

and a value $L5 > L5_{min}$ should be selected.

Core geometry selection is connected to the requirements of the specific application in terms of space utilization and other practical issues like ease of mounting, availability and so on. As to the material, the choice should be directed towards ferrite, molypermalloy or Kool Mμ®, to achieve high efficiency. These materials provide low core losses (ferrite in particular), so that the design can be concentrated on preventing saturation and limiting copper losses.

Saturation must be avoided even at maximum peak current:

$$I_{L5pk} = I_{out5} + \frac{5.1 \cdot (V_{in\,max} - 5.1)}{2 \cdot f_{sw} \cdot L_5 \cdot V_{in\,max}}$$

To limit copper losses, the winding DC resistance, $R_L$, should be as low as possible (in the range of mΩ). AC losses can usually be neglected. A practical criterion to minimize DC resistance could be to use the largest wire that fits the selected core.

Anyway the best solution, whenever possible, is to use an off-the-shelf inductor which meets the requirements in terms of inductance and maximum DC current. Nowadays there is a broad range of products

**DESIGN PROCEDURE** (continued)
offered by manufacturer, also for surface mount assemblies.

**+3.3 V Transformer**

The primary winding carries the secondary power as well, thus the total primary average current is:

$$I_{tot3} = I_{out3} + \frac{V_{inlin} \cdot I_{out12}}{3.3}$$

where $V_{inlin}$ is the voltage generated during the recirculation of the primary and fed into the input of the +12V linear regulator. The turns ratio 1:n of the transformer is chosen so that $V_{inlin}$ is above 13V. To reduce the turns ratio in order to minimize stray parameters, the secondary is referred to the 3.3V output, and therefore the minimum value is given by:

$$n_{min} = \frac{V_{inlin} - 3.3 + V_f}{3.3}$$

where $V_f$ is the forward drop across the rectifier (assume 1V to be conservative). Make sure the secondary is connected with the proper polarity (see fig. 6).

The minimum primary inductance value can be expressed as:

$$L_{3pmin} = \frac{3}{4} \cdot \frac{3.3 \cdot (V_{in} - 3.3)^2}{V_{in} \cdot f_{sw} \cdot [I_{tot3} \cdot RF \cdot (V_{in} - 3.3) - n \cdot V_{in} \cdot I_{out12}]}$$

where RF, to get positive values for $L_{3pmin}$, must satisfy the inequality:

$$RF > \frac{n \cdot V_{in} \cdot I_{out12}}{I_{tot3} \cdot (V_{in} - 3.3)}$$

and where $V_{in}$ can be either $V_{inmin}$ or $V_{inmax}$, whichever gives the higher value for $L_{3pmin}$.

With a primary inductance $L_{3p} > L_{3pmin}$ the primary peak current, which must not saturate the magnetic core, will be:

$$I_{L3pk} = I_{tot3} + \frac{3.3 \cdot (V_{in\,max} - 3.3)}{2 \cdot f_{sw} \cdot L_{3p} \cdot V_{in\,max}} + n \cdot I_{out12}$$

As to the transformer realization, the considerations regarding to the +5.1V inductor can be here repeated.

**Power MOSFET's and Schottky diodes**

Since the gate drivers of the L4992 are powered by a 5V bus , the use of logic-level MOSFET's is highly recommended, especially for high current applications. Their breakdown voltage $V_{(BR)DSS}$ must be greater than $V_{inmax}$ with a certain margin, so the selection will address 20V or 30V devices.

The $R_{DS(ON)}$ can be selected once the allowable power dissipation has been established. By selecting identical power MOSFET's as the main switch and the synchronous rectifier, the total power they dissipate does not depend on the duty cycle. Thus, if $P_{ON}$ is this power loss (few percent of the rated output power), the required $R_{DS(ON)}$ (@ 25 °C) can be derived from:

$$R_{DS(ON)} = \frac{P_{ON}}{I_{out}^2 \cdot (1 + \alpha \cdot \Delta T)}$$

where $I_{out}$ is either $I_{tot3}$ or $I_{out5}$, according to the section under consideration, $\alpha$ is the temperature coefficient of $R_{DS(ON)}$ (typically, $\alpha = 5 \cdot 10^{-3}$ °C$^{-1}$ for these low-voltage classes) and $\Delta T$ the admitted temperature rise.

It is worth noticing, however, that generally the lower $R_{DS(ON)}$, the higher is the gate charge $Q_g$, which leads to a higher gate drive consumption. In fact, each switching cycle, a charge $Q_g$ moves from the input source to ground, resulting in an equivalent drive current:

$$I_g = Q_g \cdot f_{sw}$$

**DESIGN PROCEDURE** (continued)

which affects efficiency at low load currents. Besides, this current is drawn from the REG5 line whose source capability, $I_{SRC}$ (25mA min), must not be exceeded, thus a further constraint concernes the MOSFET total gate charge (@ $V_{gs}$ = 5V);

$$Q_g \leq \frac{I_{SRC}}{4 \cdot f_{SW}},$$

assuming four identical MOSFET's.

The Schottky diode to be placed in parallel to the synchronous rectifier must have a reverse voltage VRRM greater than Vinmax. Since it conducts for less than 5% of the switching period, the current rating can be much lower than Iout. The selection criterion should be:

$$V_f(\text{schottky}) < V_f(\text{body-diode}) \ @ \ I = I_{Lpk}$$

**Sense Resistors**

The sense resistor of each section is selected according to their respective maximum output current. The current sense comparator limits the inductor peak current and therefore the maximum DC output current is the peak value less half of the peak-to-peak ripple. The intervention threshold is set at 100 mV for both sections, thus the resistor values should be:

$$R_{sense5} = \frac{100}{I_{L5pk}} \ [m\Omega]$$

$$R_{sense3} = \frac{100}{I_{L3pk}} \ [m\Omega]$$

Since the comparator threshold that triggers pulse-skipping mode is 26mV, the output current at which the system enters this kind of operation is approximately one fourth of the maximum output current.

The sense resistors values are in the low milliohms thus it is important to take correctly the current sense signals. Make sure that the Kelvin connections between the current sense pins of the IC and the sense resistor do not carry the output current.

**Input Capacitors**

A pulsed current (with zero average value) flows through the input capacitor of a buck converter. The AC component of this current is quite high and dissipates a considerable amount of power on the ESR of the capacitor:

$$P_{Cin} = ESR \cdot I_{out}^2 \cdot \frac{V_{out} \cdot (V_{in} - V_{out})}{V_{in}^2}$$

It is easy to find that PCin has a maximum equal to (1/2) · Iout (@ Vin=2 · Vout, that is, 50% duty cycle). The input capacitor of each section, therefore, should be selected for a RMS ripple current rating as high as half the respective maximum output current.

The capacitance value is not very important but in reality a minimum value must be ensured for stability reasons. In fact, switching regulators exhibit a negative input impedance that, at low frequencies, is:

$$Z_{in(DC)} = -\frac{V_{in}^2}{V_{out} \cdot I_{out}}$$

thus, if the impedance of the power source is not well below the absolute value of $Z_{in(DC)}$ at frequencies up to the bandwidth of the regulator control loop, there is the possibility for oscillations. To ensure stability, the following condition must be satisfied:

$$C_{in} >> \frac{L_{eq}}{ESR_{in} \cdot | Z_{in(DC)} |}$$

where $L_{eq}$ is the inductance of the circuit upstream the switching regulator input and $ESR_{in}$ is related to the input capacitor itself.

The use of high performance electrolytic capacitors is recommended. If a higher cost is of no concern, OS-CON capacitors are an excellent choice because they offer the smallest size for a given ESR or current rating. Tantalum capacitors do not tolerate pulsed current, so their use is not advisable.

**DESIGN PROCEDURE** (continued)

**Output Capacitors**

The output capacitor selection is based on the output voltage ripple requirements. This ripple is related to the current ripple through the inductor and is almost entirely due to the ESR of the output capacitor. Therefore, the goal is to achieve an ESR lower than a certain value, regardless of the actual capacitance value.

The maximum current ripple of the +5.1V section is:

$$\Delta I_{L5} = 2 \cdot (I_{L5pk} - I_{out5})$$

considering the values obtained in the paragraph "+5.1 V Inductor".

As for the +3.3V, the maximum ripple is given by:

$$\Delta I_{L3} = n \cdot I_{out12} \cdot \frac{V_{in}}{V_{in} - 3.3} + \frac{3}{4} \cdot \frac{3.3 \cdot (V_{in} - 3.3)}{f_{sw} \cdot L_{3p} \cdot V_{in}}$$

where $V_{IN}$ is $V_{inmin}$ or $V_{inmax}$, as selected in the "+3.3V transformer" section.

Anyhow, the maximum ESR will be:

$$ESR_x \leq \frac{V_{rppx}}{\Delta I_{Lx}}$$

where the subscript x refers to either section.

In pulse-skipping operation, the capacitive component of the output ripple is comparable to the resistive one, thus both should be considered:

$$V_{rppx}^{(R)} = 0.025 \cdot \frac{ESR_X}{R_{sense_x}}$$

$$V_{rppx}^{(C)} = 3.1 \cdot 10^{-6} \cdot \frac{L_x}{C_{outx}} \cdot \frac{1}{R_{sensex}^2} \cdot \left( \frac{1}{V_{in\,min} - V_{out}} - \frac{1}{V_{out}} \right)$$

If specification on the output ripple under pulse-skipping condition is also given, $C_{outx}$ and $ESR_X$ must comply with it as well.

Further constraints on the minimum output capacitance can arise from specifications regarding the maximum undershoot, $\Delta V^-_{out}$, or overshoot, $\Delta V^+_{out}$, due to a step-load change $\Delta I_{out}$:

$$C_{out} > \frac{L \cdot \Delta I_{out}^2}{\Delta V_{out}^- \cdot (V_{in\,min} \cdot D_{max} - V_{out})}; \quad C_{out} > \frac{L \cdot \Delta I_{out}^2}{\Delta V_{out}^+ \cdot V_{out}}$$

whichever is greater, and where $D_{max}$ is the maximum duty cycle and the quantities are relevant either to the +3.3V or +5.1V section.

High performance capacitors should be employed to reduce the capacitance needed for a given ESR, to avoid paralleling several parts with a considerable waste of space. Although excellent electrolytic capacitors are available, OS-CON or tantalums may be preferred especially if very compact design is required, or in case of surface mount assemblies. Multilayer ceramic capacitors with extremely low ESR are now available, but they have a large spread of the capacitance value, so they should be paralleled with another more stable, high-ESR capacitor.

**Miscellaneous components**

The feedback loop has virtually unlimited bandwidth, thus a filter is necessary to make the system insensitive to the switching frequency ripple and, in general, to prevent noise from disturbing the correct operation of the error summing comparator. Anyway, the cut-off frequency of this filter can be very high, so that line and load transient response is extremely fast. This filter is a simple R-C type where resistance and capacitance can be chosen for a typical 3dB cut-off frequency of 60 kHz.

As to the bootstrap diodes, even though small signal p-n diodes might be effectively used, it is preferable to employ low-power Schottky rectifiers, since that increase slightly the gate drive voltage, in favour of efficiency. The bootstrap capacitor can be a 100nF film capacitor.

The soft-start capacitors determine the time during which the current limitation circuit moves gradually the setpoint from zero up to 100 mV in order to limit the current inflow at start-up. This ramp lasts approximately 1 ms per nF of soft-start capacitance (10 to 100 nF typical values), but the actual time necessary to the output voltage to reach the steady-state value depends on the load current and the output filter capacitance.

There are some critical points of the IC that may require by-pass capacitors to prevent noise from dis-

**DESIGN PROCEDURE** (continued)
turbing the circuit. These points are the reference voltage VREF, the IC supply pin VIN, the REG5 line and the alternative supply pin V5SW. Use film capacitors suitable for AC decoupling.

+12 V LINEAR REGULATOR

**Catch Diode**

The diode which steers the current generated by the secondary winding of the +3.3V transformer should be a p-n fast-recovery one, with a breakdown voltage greater than:

$$V_{RR} = (V_{inlin} - 3.3) + n \cdot (V_{in\,max} - 3.3)$$

with a certain safety margin. The diode has to withstand a pulsed current whose peak value is approximately:

$$I_{13pk} \cong I_{out12} \cdot \frac{V_{in\,min}}{V_{in\,min} - 3.3},$$

while its RMS value is given by:

$$I_{13RMS} = I_{out12} \cdot \sqrt{\frac{V_{in\,min}}{V_{in\,min} - 3.3}}$$

The DC value is obviously $I_{out12}$.

**Filter Capacitors**

The most stringent requirement on the input filter capacitor (connected between V13IN and ground) is its RMS ripple current rating, which should be at least:

$$I_{13AC} = I_{out12} \cdot \sqrt{\frac{3.3}{V_{in\,min} - 3.3}}$$

The working voltage should be higher than the voltage generated when the regulator is lightly loaded. Also for this part the use of high quality electrolytic or OS-CON capacitors is advised.

LAYOUT AND GROUNDING

The electrical design is only the first step in the development of a switching converter. Since currents ranging from μAmperes to some Amperes, both DC and switched, live together on the same circuit-board, the PCB layout is vital for a correct operation of the circuit but is not an easy task.

A proper layout process generally includes careful component placing, proper grounding, correct traces routing, and appropriate trace widths. Fortunately, since low voltages are involved in this kind of applications, isolation requirements are of no concern.

Referring to literature for a detailed analysis of this matter, only few important points will be here reminded.

1) All current returns (signal ground, power ground, etc.) should be mutually isolated and should be connected only at a single ground point. Ground planes may be extremely useful both to arrange properly current returns and to minimize radiation (see next 2 points), even though they cannot solve every problem
2) Noise coupling between adjacent circuitry can be reduced minimizing the area of the loop where current flows. This is particularly important where there are high pulsed currents, that is the circuit including the input filter capacitor, the power switch, the synchronous rectifier and the output capacitor. The next priority should be given to the gate drive circuits.
3) Magnetic field radiation (and stray inductance) can be reduced by keeping all traces which carry switched currents as short as possible.
4) The Kelvin-connected traces of current sense should be kept short and close together.
5) For high current paths, the traces could be doubled on the other side of the PCB whenever possible: this will reduce both the resistance and the inductance of the wiring.
6) In general, traces carrying signal currents should run far from traces carrying pulsed currents or with quickly swinging voltages. From this viewpoint, particular care should be taken of the high impedance paths (feedback input, current sense traces...). It could be a good idea to route signal traces on one

**DESIGN PROCEDURE** (continued)

PCB side and power traces on the other side.

7) Use heavy copper traces: this will reduce their resistance, increasing overall efficiency and will improve their heat-sinking ability.

**L4992 EVAL-KIT**

The L4992 EVAL KIT is a fully assembled and tested demonstration board that implements a standard application circuit, configured according to the following specifications:

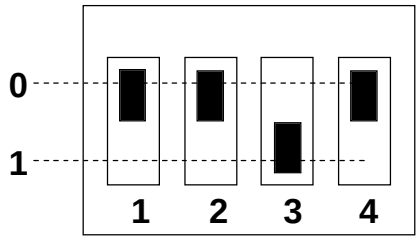
- Input Voltage Range: 6 to 25 V
- 3.3V Output: $I_{out3}$ = 3 A, $V_{rpp3} \leq 30$ mV
- 5.1V Output: $I_{out5}$ = 3 A, $V_{rpp5} \leq 50$ mV
- 12 V Output: $I_{out12}$ = 120 mA
- Switching frequency: $f_{sw}$ = 300 kHz

The electrical schematic, illustrated in fig. 9, shows that some pull-up/down resistor are added to the components strictly needed in a real application. Along with a quad dip-switch, they allow to set manually the logic signals that control the chip operation. These signals are in the present case:

- Switch 1: RUN5 (0= 5.1V OFF, 1= 5.1V ON)
- Switch 2: NOSKIP (0= pulse-skipping ON, 1= pulse-skipping OFF)
- Switch 3: OSC (0= 200 kHz, 1= 300 kHz)
- Switch 4: RUN3 (0= 3.3V OFF, 1= 3.3V ON)

The demonstration board is delivered with the switches configured as illustrated in fig. 8.

**Figure 8:** Default switches configuration




Switches 1 and 4 enable/disable the two PWM sections (switch 4 manages the +12V linear regulator as well). They must be set on 1 to turn on the regulators.

Please note that as long as each regulator is disabled, the relevant low-side MOSFET is in ON state. Hence, if the load is capable of sourcing current, it will be short-circuited to ground through the choke and the low-side MOS.

Although the default switching frequency is 300 kHz (switch 3 set on 1) and the passive components have been selected for this frequency, the demo board will work satisfactorily at 200 kHz as well. Actually, at 200 kHz the regulators exhibit the maximum efficiency and the maximum extension of the input voltage range downwards. On the other hand, the output ripple is greater and the dynamic behaviour slightly worse.

The demostration board, as it is, does not provide an interface for synchronization. Anyway, it is possible to synchronize the oscillator (with an appropriate signal: 5V amplitude pulses, spaced out by 400 ns min.), provided the switch is set on 1, simply by feeding the signal into the middle of the divider R8-R9. In this way, synchronization can be achieved at a frequency higher than 300 kHz. To synchronize the oscillator to a frequency between 200 and 300 kHz, heavier interventions on the board are needed.

**DESIGN PROCEDURE** (continued)

**Figure 9a:** Evaluation Board Circuit.

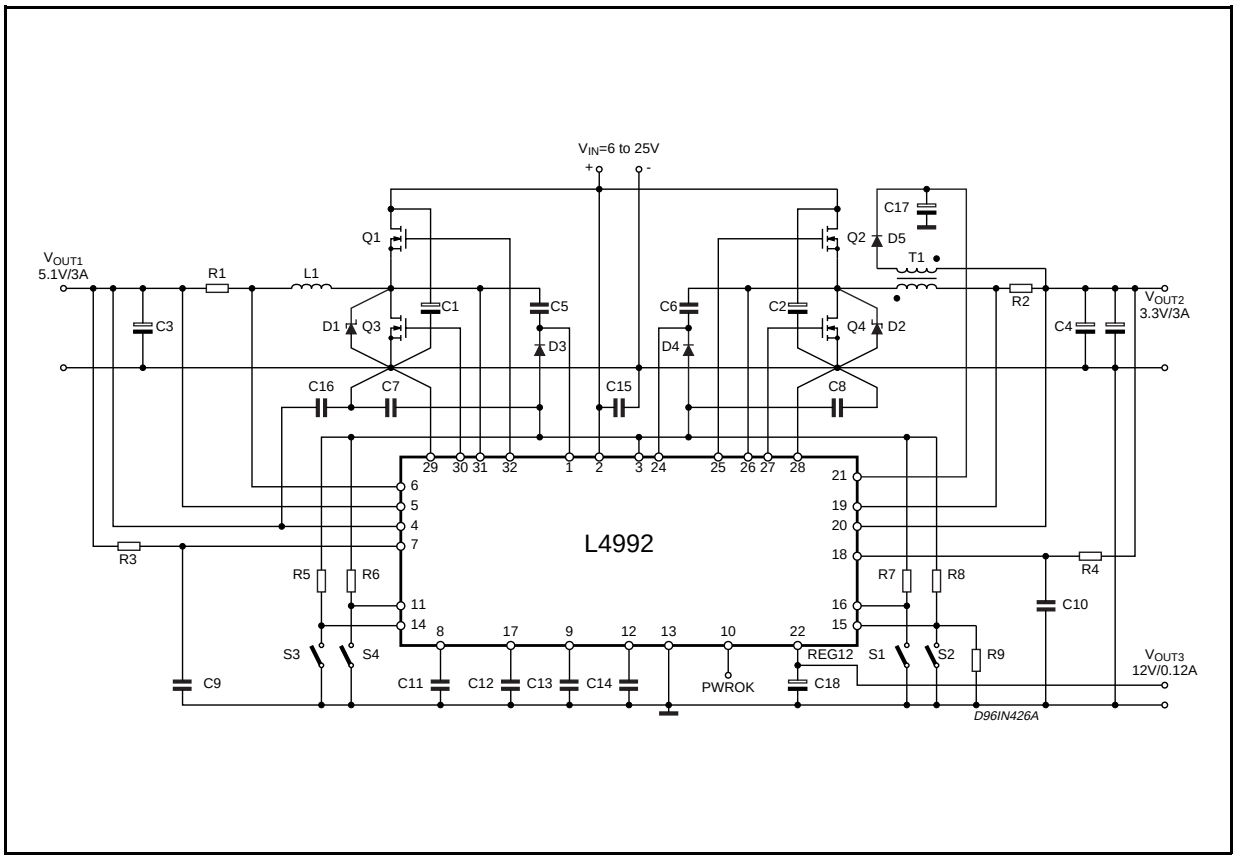
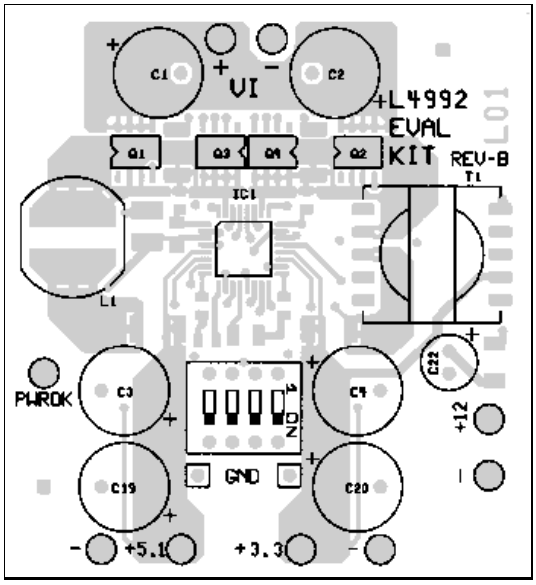



**Table 1:** L4992 EVAL-KIT parts list

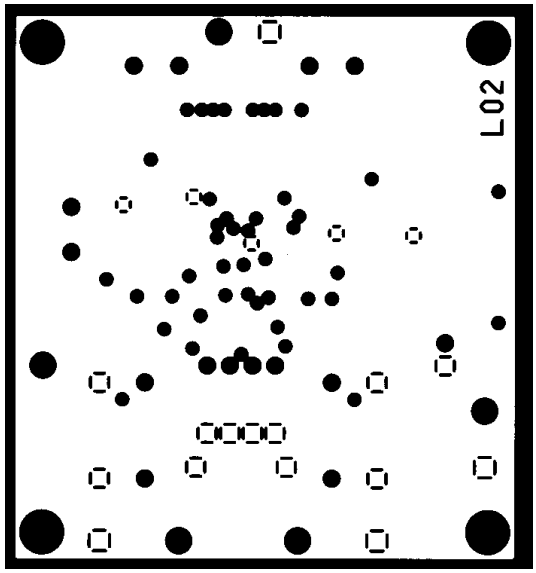
| Component | Refer. | Value | Description |
|---|---|---|---|
| Resistors | R1 | 25mΩ | 1%, 0.5W. DALE. p.n. WSL-2512R0251 |
| | R2 | 20mΩ | 1%, 0.5W. DALE. p.n. WSL-2512R0201 |
| | R3, R4 | 270Ω | 1%,SMD |
| | R5, R6, R7, R8, R9 | 1MΩ | SMD |
| Capacitors | C1, C2 | 100µF | 20V. SANYO OS-CON. p.n. 20SA100K |
| | C3, C4 | 220µF | 10V. SANYO OS-CON. p.n. 10SA220K |
| | C5, C6, C12, C13 | 100µF | SMD |
| | C7, C8, C15, C16 | 1µF | SMD |
| | C9, C10, C11 | 10nF | SMD |
| | C14, C18 | 4.7µF | 16V. Tantalum. SMD |
| | C17 | 15µF | 25V. SANYO OS-CON. p.n. 25SC15M |
| Magnetics | L1 | 10µH | 2.65A. SUMIDA. p.n. CDR125-100 |
| | T1 | 10µH | 1:4 ratio. TRANSPOWER. p.n. TTI5902 |
| MOSFET's | Q1, Q2, Q3, Q4 | Si9410DY | SILICONIX |
| Diodes | D1, D2 | TMBYV10-40 | ST. MELF package |
| | D3, D4 | TMMBAT46 | ST. MINIMELF package |
| | D5 | SMBYW01-200 | ST.SOD6 package |
| Switches | S1, S2, S3, S4 | - | Quad dip-switch |

**DESIGN PROCEDURE** (continued)

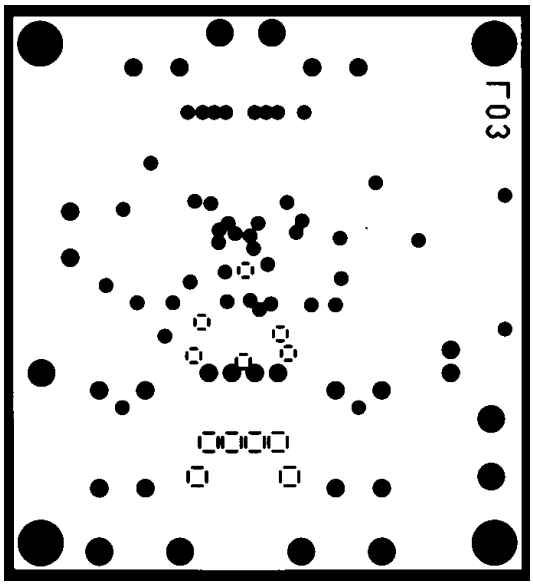
**Figure 9b:** PCB and component Layout of the Evaluation Board of Figure 9a.



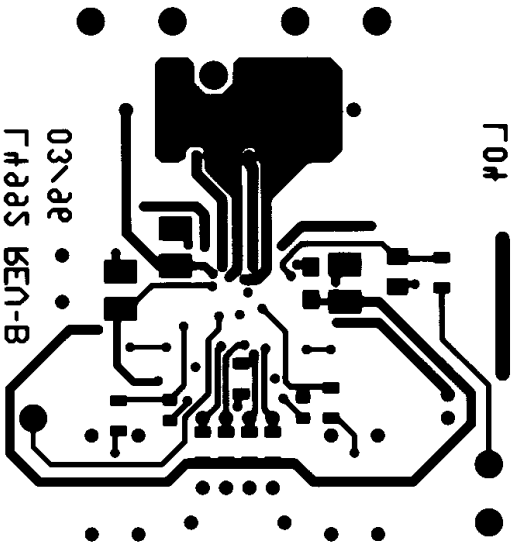

Top Layer + Silk (56 x 61mm)




Signal Ground Plane




Power Ground Plane




Bottom Layer

**DESIGN PROCEDURE** (continued)

Pulse-skipping operation is enabled by default in order to maximize efficiency also in low load current range. The transition between PWM and pulse-skipping occurs approximately below 1A, however there is a region in which the two operation modes coexist rather than a definite boundary. That can be seen on the scope as an irregularity of the waveforms but does not have much influence both on output ripple and efficiency.

Those who do not appreciate asynchronous operation of the pulse-skipping mode can disable it for both regulators, by setting switch 2 on 1. That maintains PWM operation up to very low output currents where, however, the regulation becomes incompatible with the switching frequency. This means that the minimum ON-time of the high-side MOSFET is too long for the thruput energy level at the operating frequency. Thus the control system begins skipping conduction cycles to avoid the output voltage drifting upwards.

Table 1 shows the complete L4992 EVAL KIT parts list. Critical components characteristics are given in detail.

**DEMO BOARD EVALUATION**

The following diagrams and tables show the typical performance of the demonstration board in terms of efficiency, line regulation and load regulation. The 12V linear regulator and REG5 are also characterized.

**Table 2:** PWM Regulators: Optimum Efficiency

| Parameter | Test Condition | Value | Unit |
|---|---|---|---|
| +3.3V Maximum Efficiency | RUN3 = RUN5 = HIGH, NOSKIP = LOW<br>Vin = 6V, Iout = 0.5 A, $f_{SW}$ = 200 kHz<br>Vin = 6V, Iout = 1A, $f_{SW}$ = 300 kHz | <br>95.2<br>94.6 | % |
| +5.1V Maximum Efficiency | RUN3 = LOW, NOSKIP = LOW<br>Vin = 6V, Iout = 1A, $f_{SW}$ = 200 kHz<br>Vin = 6V, Iout = 1A, $f_{SW}$ = 300 kHz | <br>96.4<br>95.8 | % |

**Table 3:** PWM regulators: Line and Load Regulation.

| Parameter | Test Condition | Value | Unit |
|---|---|---|---|
| +3.3V Line Regulation | RUN5 = LOW, NOSKIP = LOW, 6 < Vin < 20V<br>Iout = 0.1 A, $f_{SW}$ = 200 kHz<br>Iout =1A, $f_{SW}$ = 200 kHz | <br>2<br>15 | mV |
| +5.1V Line Regulation | RUN3 = LOW, NOSKIP = LOW, 6 < Vin < 20V<br>Iout = 0.1A, $f_{SW}$ = 200 kHz<br>Iout = 1A, $f_{SW}$ = 200 kHz | <br>3<br>20 | mV |
| +3.3V Load Regulation | RUN5 = LOW, NOSKIP = LOW, 5 mA < Iout < 3A<br>Vin = 6 V, $f_{SW}$ = 200 kHz<br>Vin = 15V, $f_{SW}$ = 200 kHz | <br>85<br>70 | mV |
| +5.1V Load Regulation | RUN3 = LOW, NOSKIP = LOW, 5 mA < Iout < 3A<br>Vin = 6 V, $f_{SW}$ = 200 kHz<br>Vin = 15V, $f_{SW}$ = 200 kHz | <br>90<br>75 | mV |

**DEMO BOARD-EVALUATION** (continued)

**Figure 10:** 5.1V Output (RUN3=LOW, RUN5 = HIGH, OSC = GND, NOSKIP = LOW)

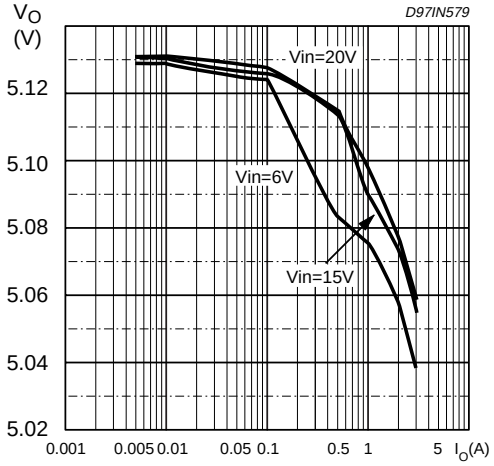



**Figure 11:** 3.3V Output (RUN3=HIGH, RUN5 = LOW, OSC = GND, NOSKIP = LOW)

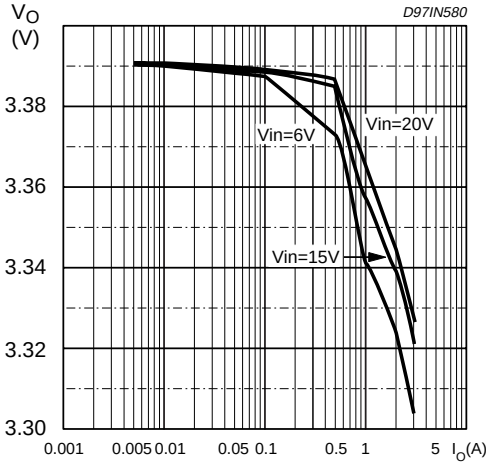



**Figure 12:** Demo Board Efficiency vs Output Current

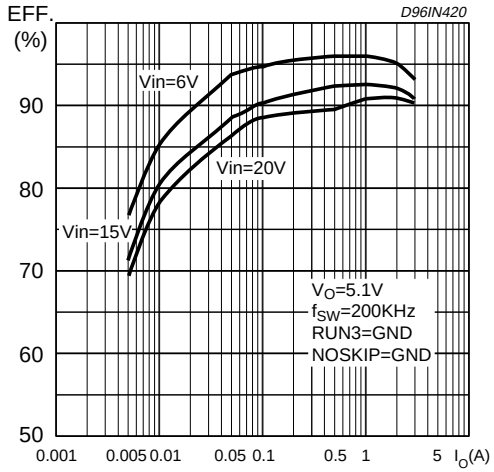



**Figure 13:** Demo Board Efficiency vs Output Current

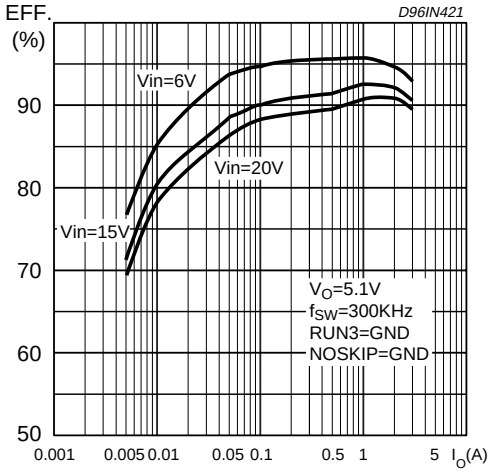



**Figure 14:** Demo Board Efficiency vs Output Current

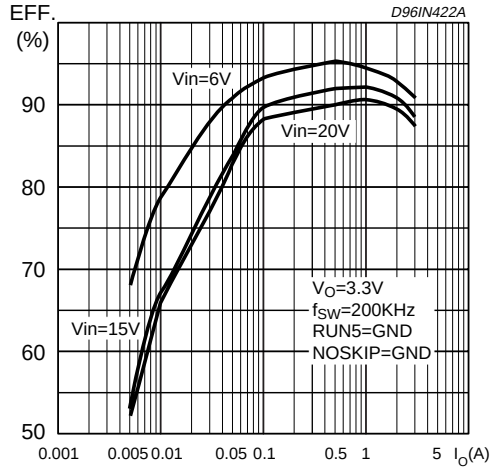
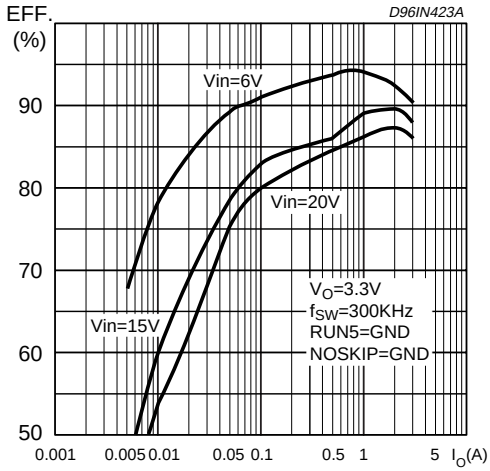



**Figure 15:** Demo Board Efficiency vs Output Current



**DEMO BOARD-EVALUATION** (continued)

**Figure 16:** Demo Board Overall Efficiency (Iout3 = 3A, REG12 = OPEN, OSC = GND)

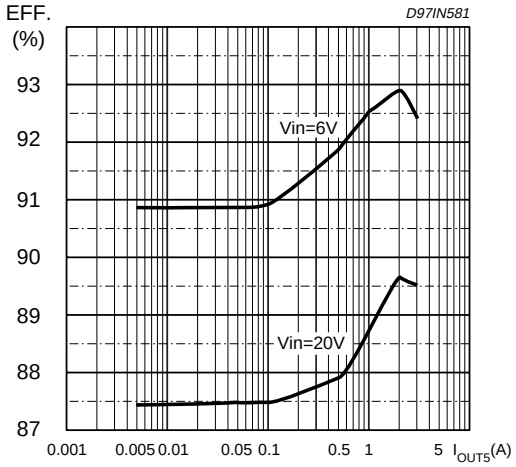



**Figure 17:** Demo Board Overall Efficiency (Iout5 = 3A, REG12 = OPEN, OSC = GND)

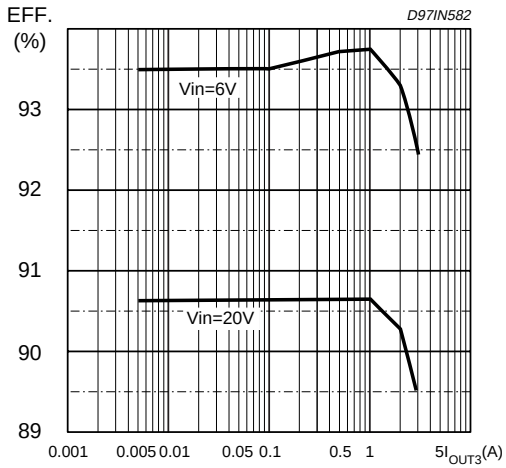



**Figure 18:** Switching Frequency vs Output Current (pulse skipping)

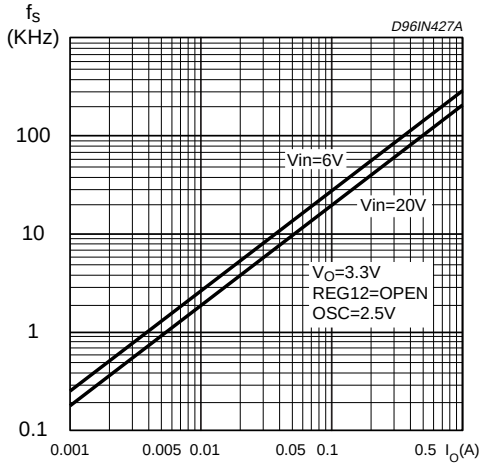



**Figure 19:** Switching Frequency vs Output Current (pulse skipping)

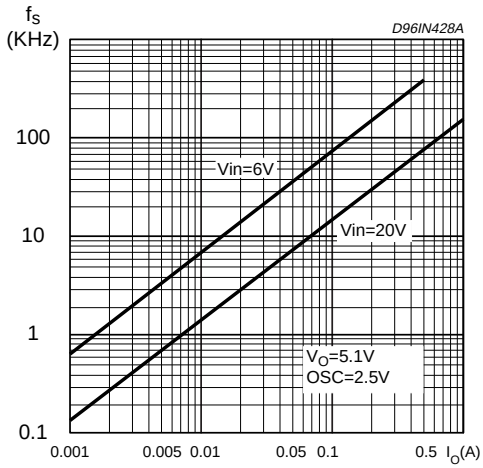



**Figure 20:** REG5 Regulator Characteristic (Vin = 6V, RUN3 = RUN5 = LOW, Tj = 25°C)

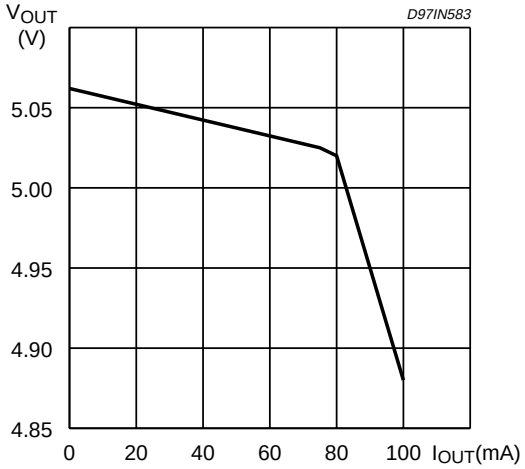
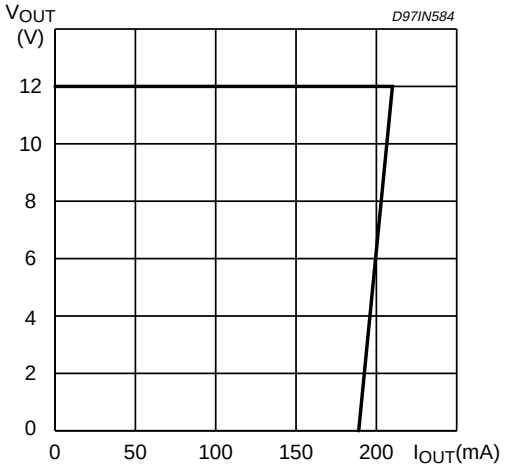



**Figure 21:** 12V Linear Regulator Characteristic (V13IN = 15V, RUN3 = HIGH, Tj = 25 °C)



## APPLICATION IDEAS

**Figure 22:** Application with Split Supply

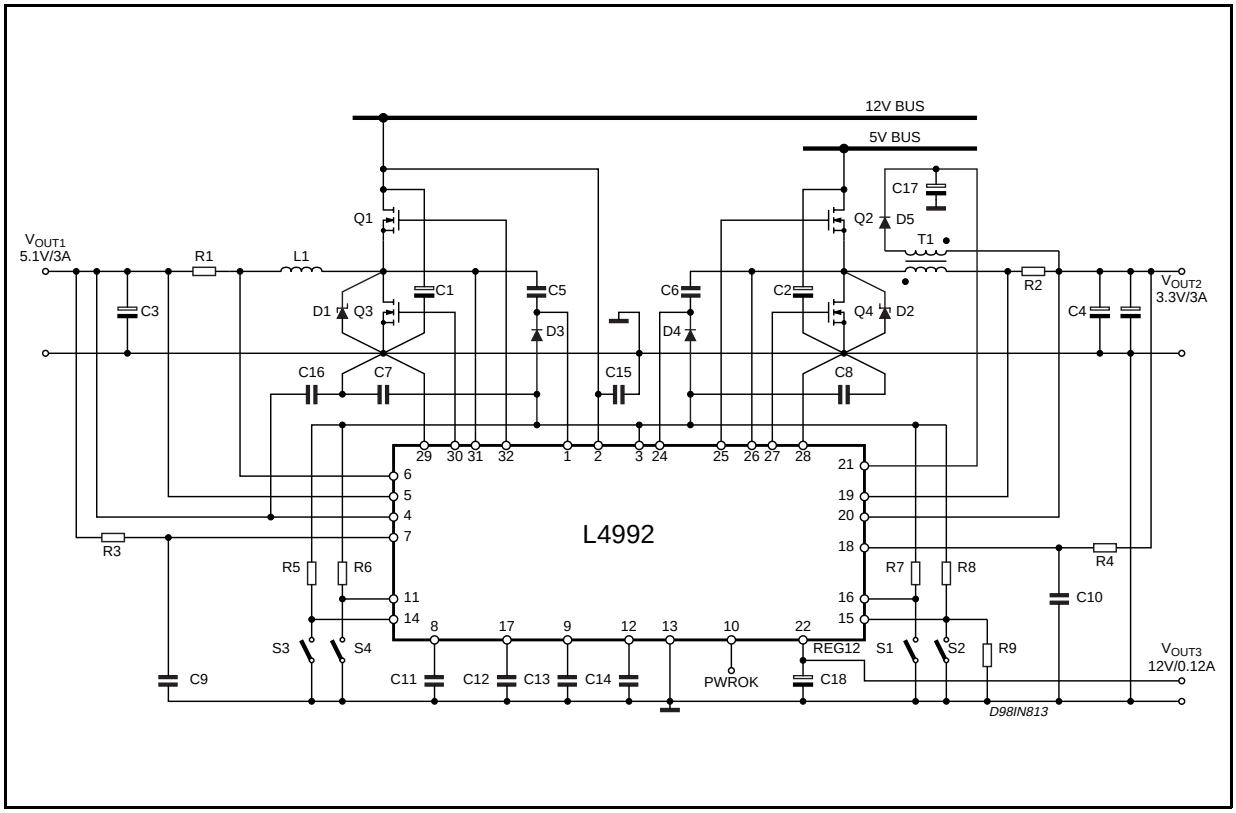
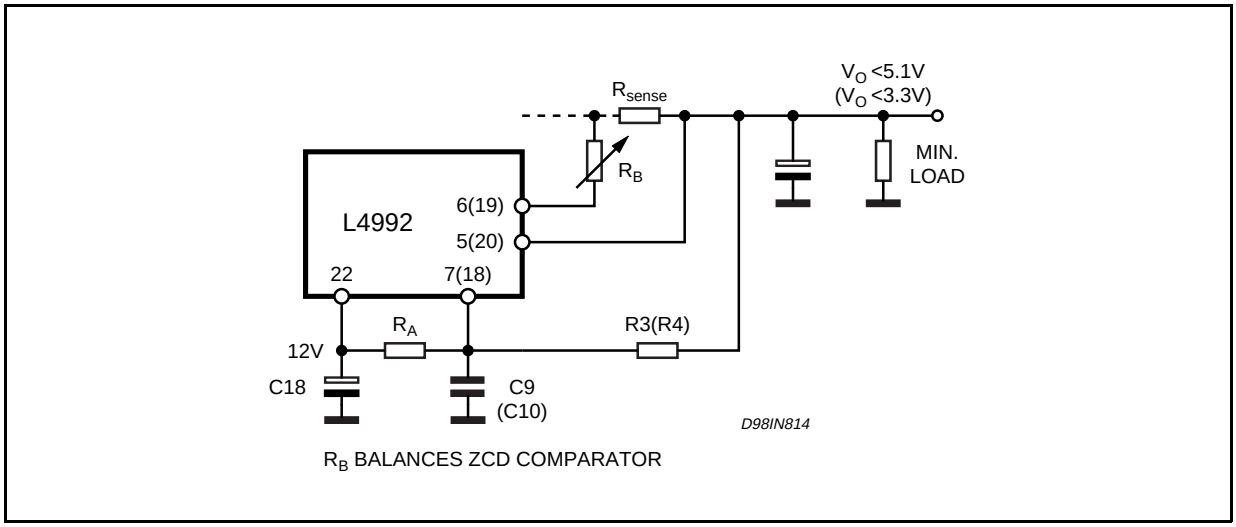


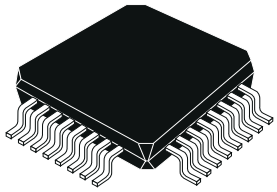

**Figure 23:** Low output voltage.




$R_B$ BALANCES ZCD COMPARATOR

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B | 0.30 | 0.37 | 0.45 | 0.012 | 0.015 | 0.018 |
| C | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 9.00 | | | 0.354 | |
| D1 | | 7.00 | | | 0.276 | |
| D3 | | 5.60 | | | 0.220 | |
| e | | 0.80 | | | 0.031 | |
| E | | 9.00 | | | 0.354 | |
| E1 | | 7.00 | | | 0.276 | |
| E3 | | 5.60 | | | 0.220 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| K | 0°(min.), 7°(max.) | | | | | |

## OUTLINE AND MECHANICAL DATA



## TQFP32