

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT
HCT563 INVERTING - HCT573 NON INVERTING

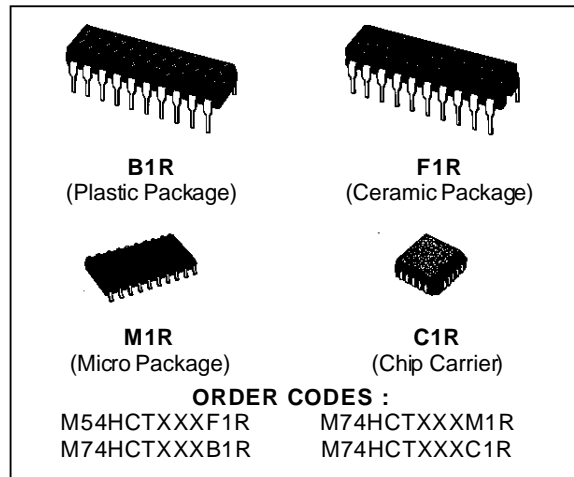
- HIGH SPEED
t_{PD} = 18 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX.)
- OUTPUT DRIVE CAPABILITY
15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
I_{OL} = |I_{OH}| = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
t_{PLH} = t_{PHL}
- PIN AND FUNCTION COMPATIBLE
WITH 54/74LS563/573

DESCRIPTION

The M54/74HCT563 and M54HCT573 are high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with silicon gate C²MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8 bit D-Type latches are controlled by a latch enable input (LE) and a output enable input (OE). While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the OE input is at low level,

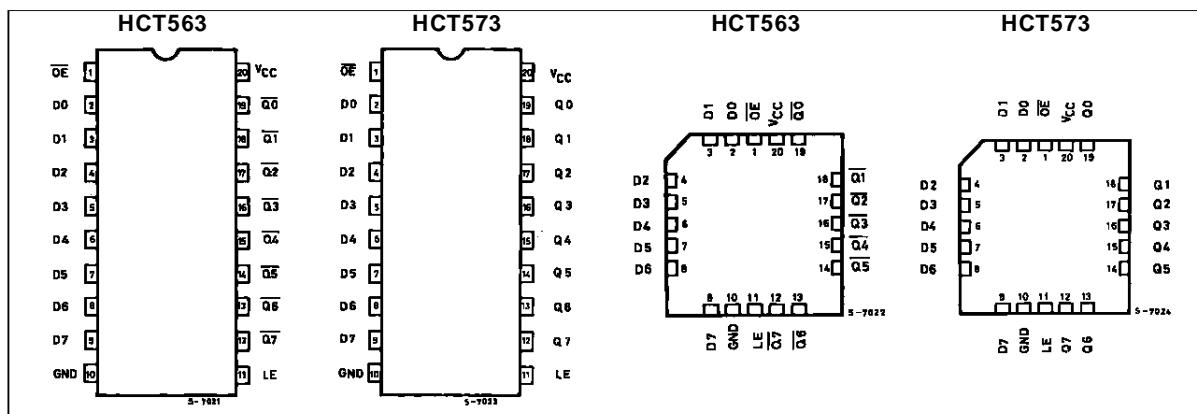


the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The application designer has a choice of combination of inverting and non inverting outputs. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

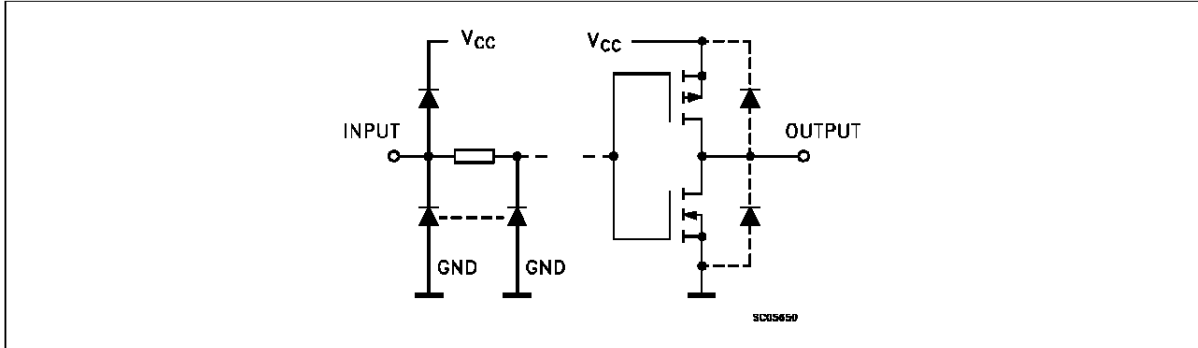
All inputs are equipped with protection circuits against discharge and transient excess voltage.

PIN CONNECTION (top view)



M54/M74HCT563/573

INPUT AND OUTPUT EQUIVALENT CIRCUIT



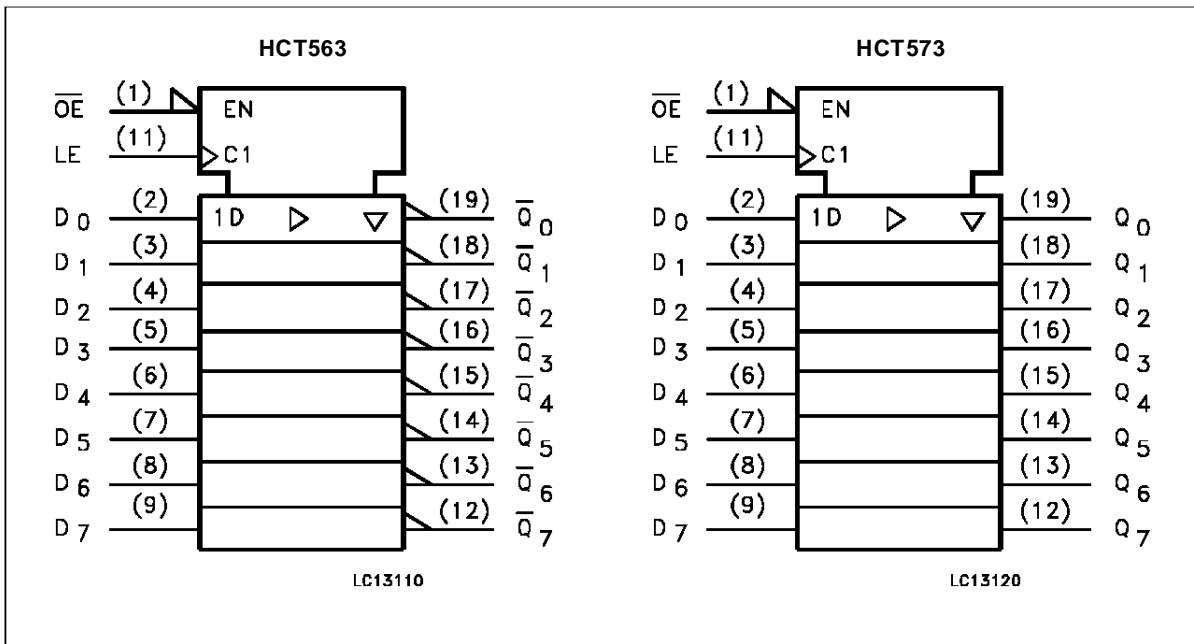
PIN DESCRIPTION (HCT563)

PIN No	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HCT573)

PIN No	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS

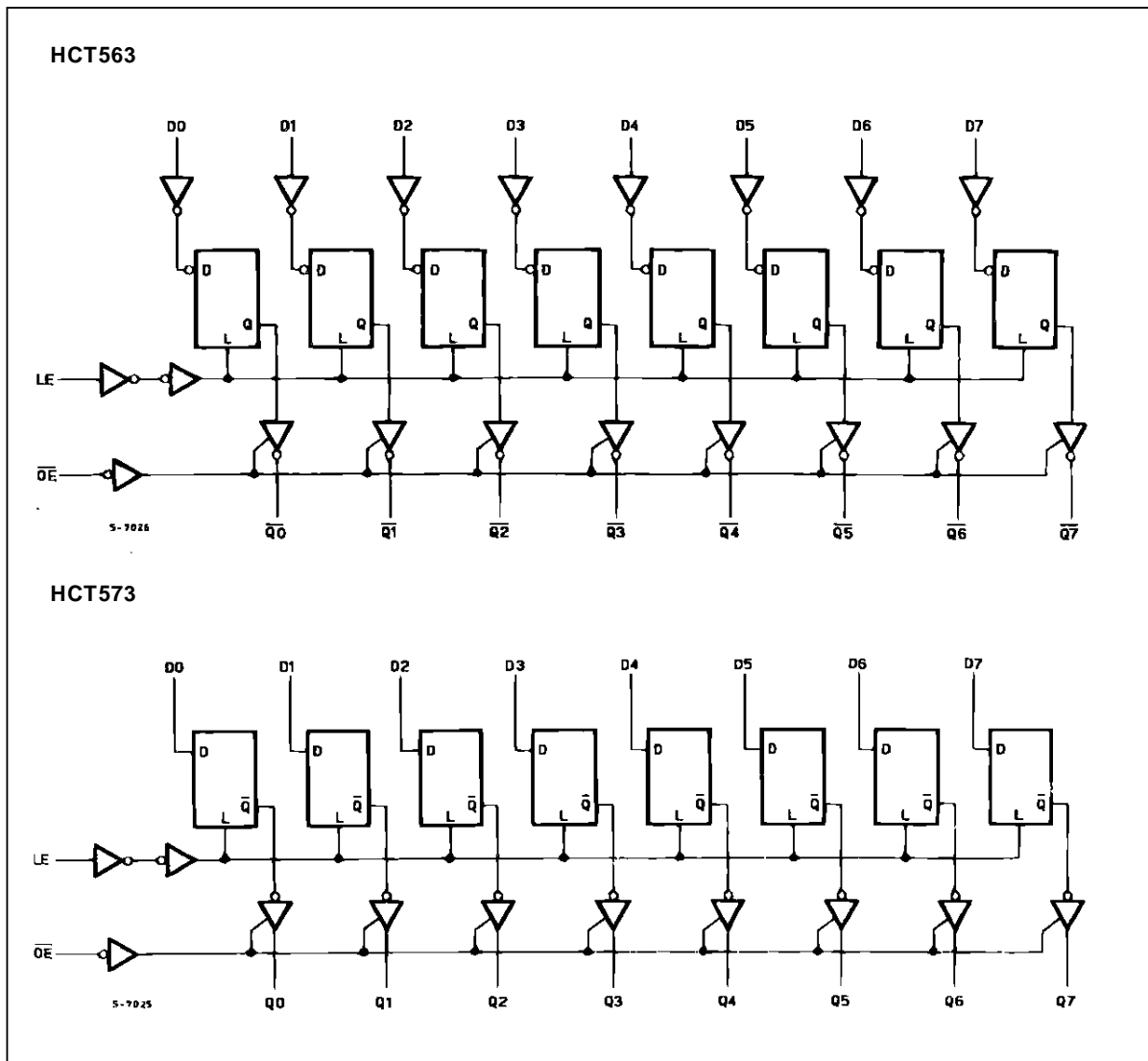


TRUTH TABLE

INPUTS			OUTPUTS	
\overline{OE}	LE	D	Q (HCT573)	\overline{Q} (HCT563)
H	X	X	Z	Z
L	L	X	NO CHANGE *	NO CHANGE *
L	H	L	L	H
L	H	H	H	L

X: DON'T CARE
 Z: HIGH IMPEDANCE
 *: Q/Q OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS



M54/M74HCT563/573

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	4.5 to 5.5	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C
t _r , t _f	Input Rise and Fall Time (V _{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

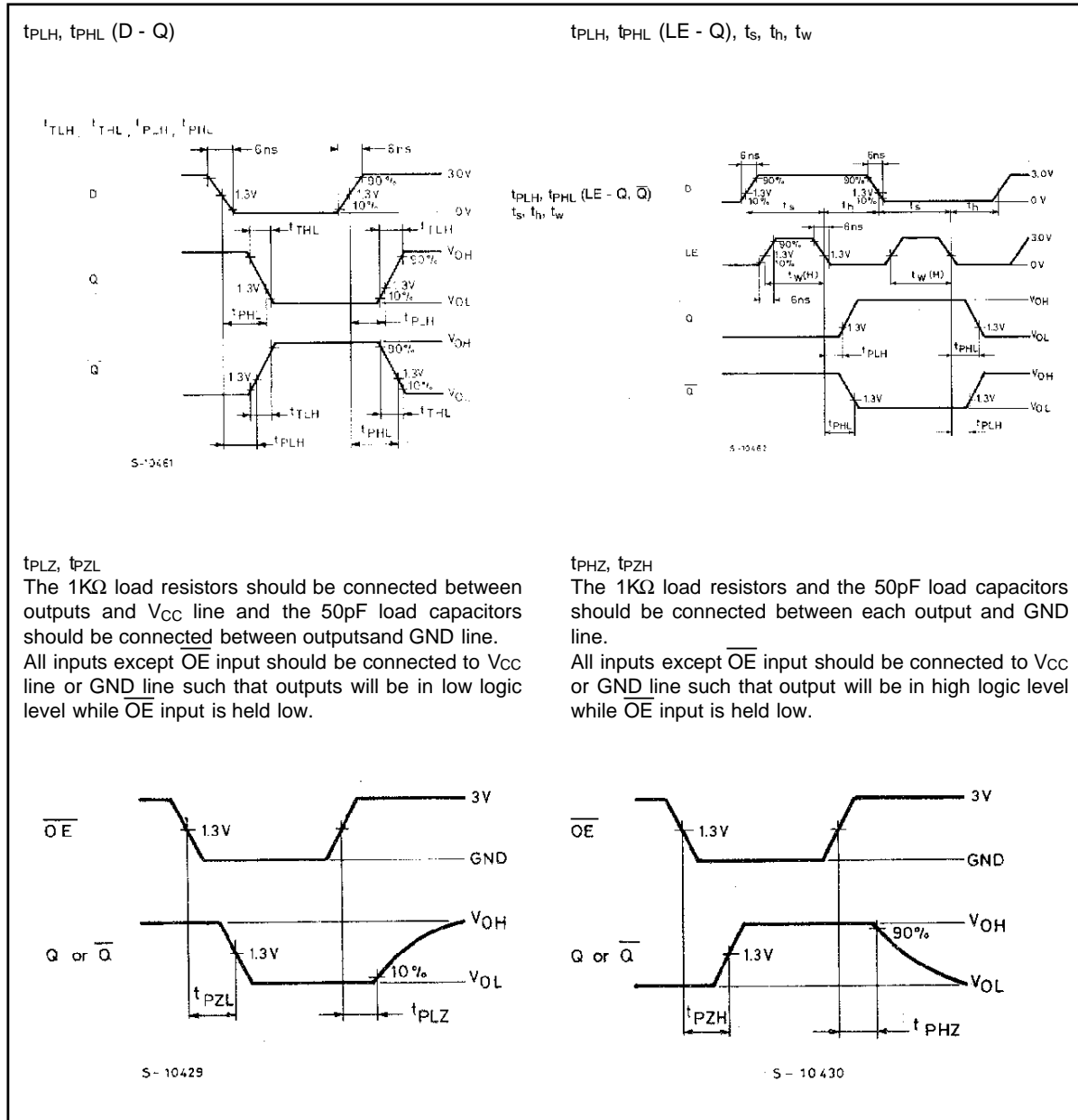
Symbol	Parameter	Test Conditions		Value						Unit		
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V	
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V	
V _{OH}	High Level Output Voltage	4.5	V _I = V _{IH} or V _{IL}	I _O = -20 μA	4.4	4.5		4.4		4.4	V	
				I _O = -6.0 mA	4.18	4.31		4.13		4.10		
V _{OL}	Low Level Output Voltage	4.5	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
				I _O = 6.0 mA		0.17	0.26		0.33		0.4	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND				±0.1		±1		±1	μA
I _{OZ}	3 State Output Off State Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND				±0.5		±5.0		±10	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND				4		40		80	μA
ΔI _{CC}	Additional worst case supply current	5.5	Per Input pin V _I = 0.5V or V _I = 2.4V Other Inputs at V _{CC} or GND				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	Test Conditions			Value						Unit	
		V_{CC} (V)	C_L (pF)		$T_A = 25 \text{ }^\circ\text{C}$ 54HC and 74HC			$-40 \text{ to } 85 \text{ }^\circ\text{C}$ 74HC		$-55 \text{ to } 125 \text{ }^\circ\text{C}$ 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q, \bar{Q})	4.5	50			21	33		41		50	ns
		4.5	150			25	39		49		59	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - Q, \bar{Q})	4.5	50			19	30		38		45	ns
		4.5	150			23	36		45		54	ns
t_{PZL} t_{PZH}	3 State Output Enable Time	4.5	50	$R_L = 1 \text{ K}\Omega$		19	30		38		45	ns
		4.5	150	$R_L = 1 \text{ K}\Omega$		23	36		45		54	ns
t_{PZL} t_{PZH}	3 State Output Disable Time	4.5	50	$R_L = 1 \text{ K}\Omega$		18	25		31		38	ns
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (LE)	4.5	50			7	15		19		22	ns
t_s	Minimum Set-up Time	4.5	50			4	10		13		15	ns
t_h	Minimum Hold Time	4.5	50				5		5		5	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
$C_{PD} (*)$	Power Dissipation Capacitance					51						pF

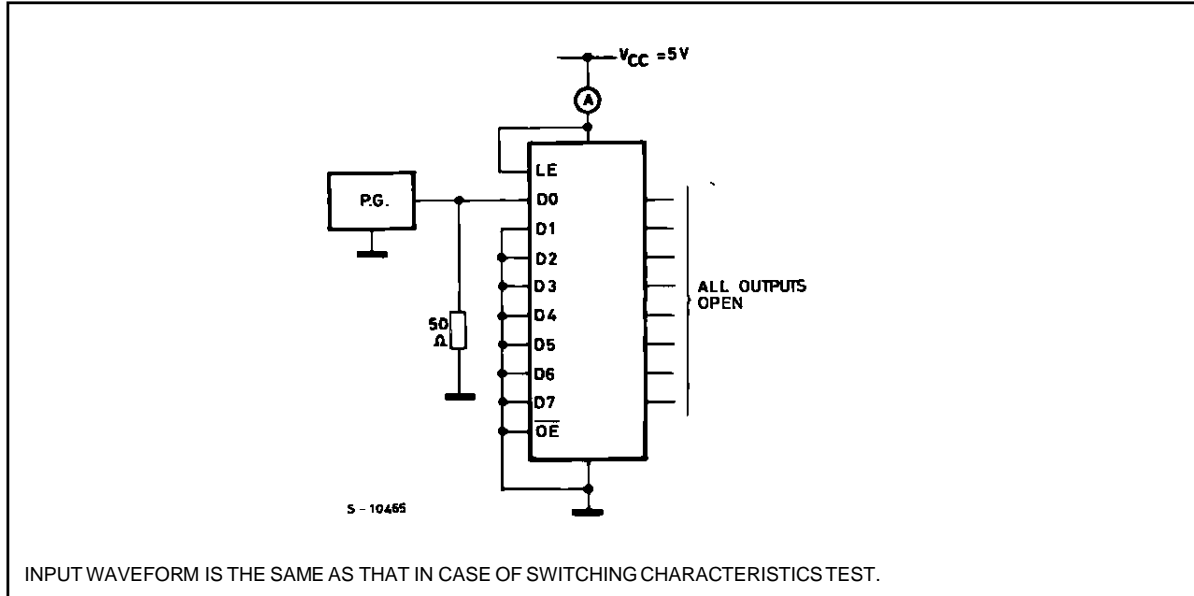
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip-Flop)

SWITCHING CHARACTERISTICS TEST WAVEFORM



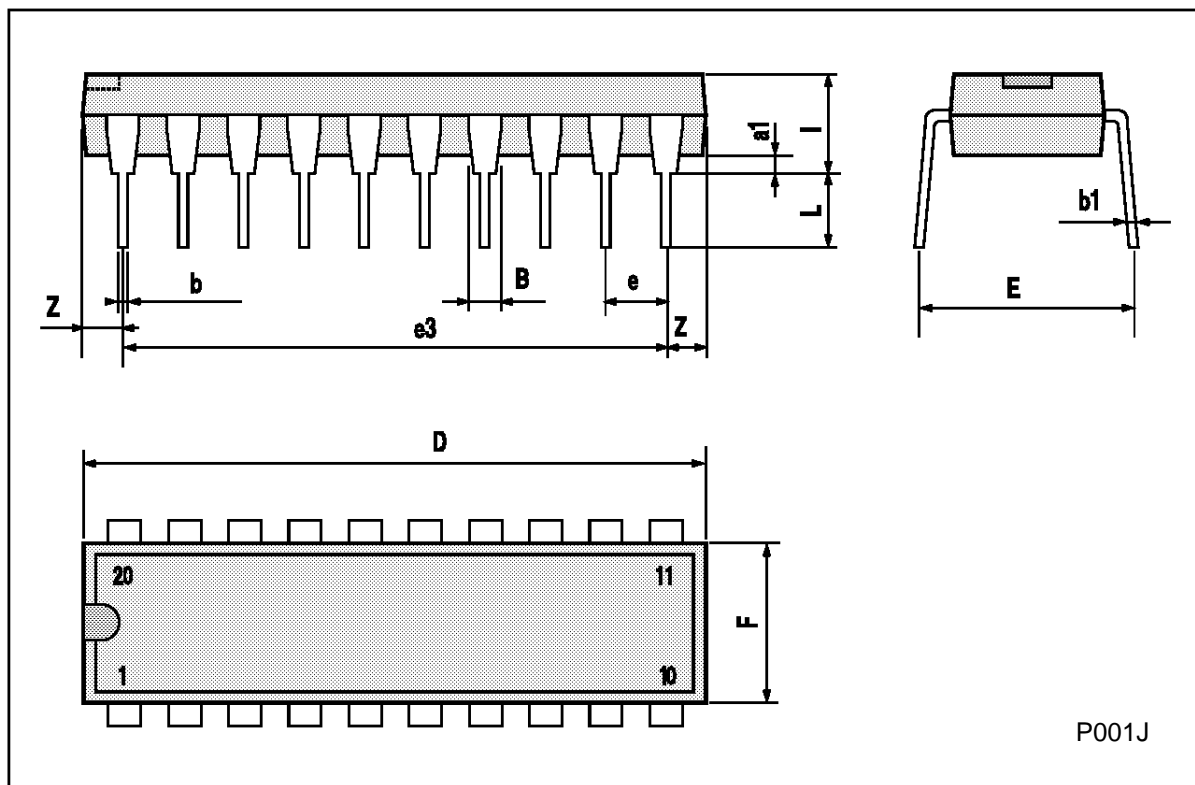
M54/M74HCT563/573

TEST CIRCUIT I_{CC} (Opr.)



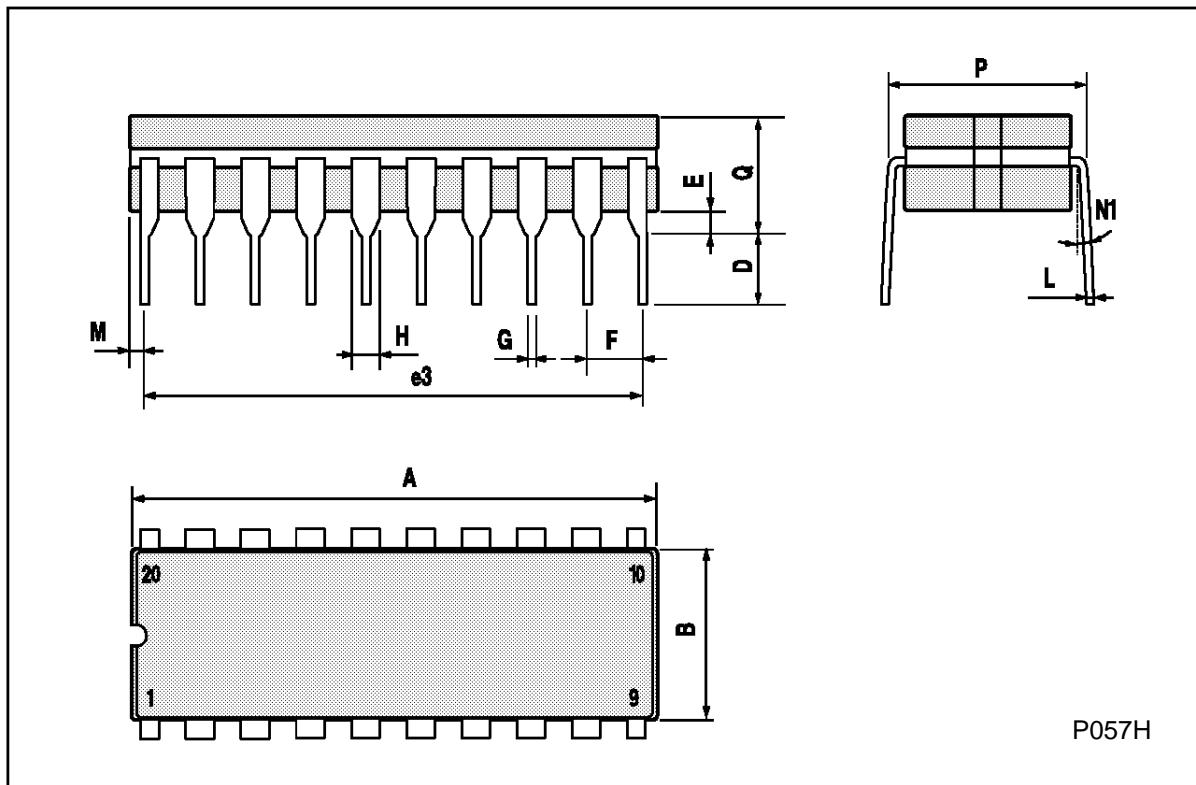
Plastic DIP20 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



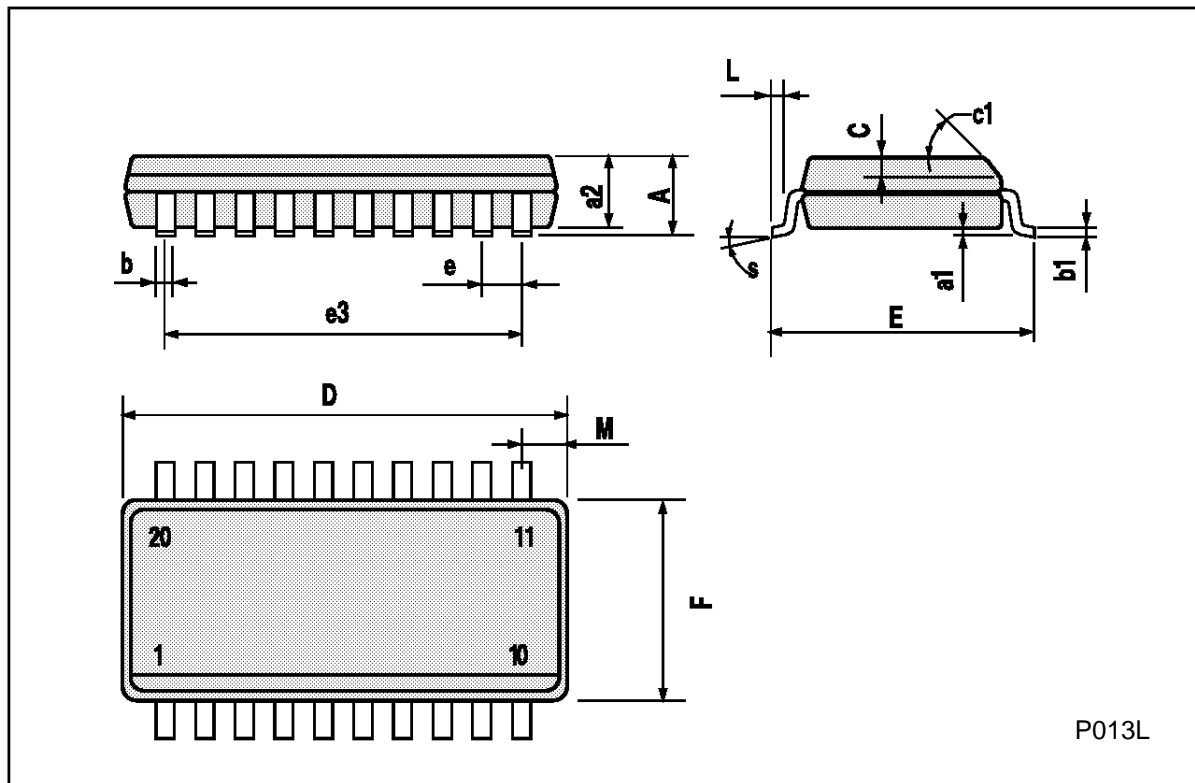
Ceramic DIP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225



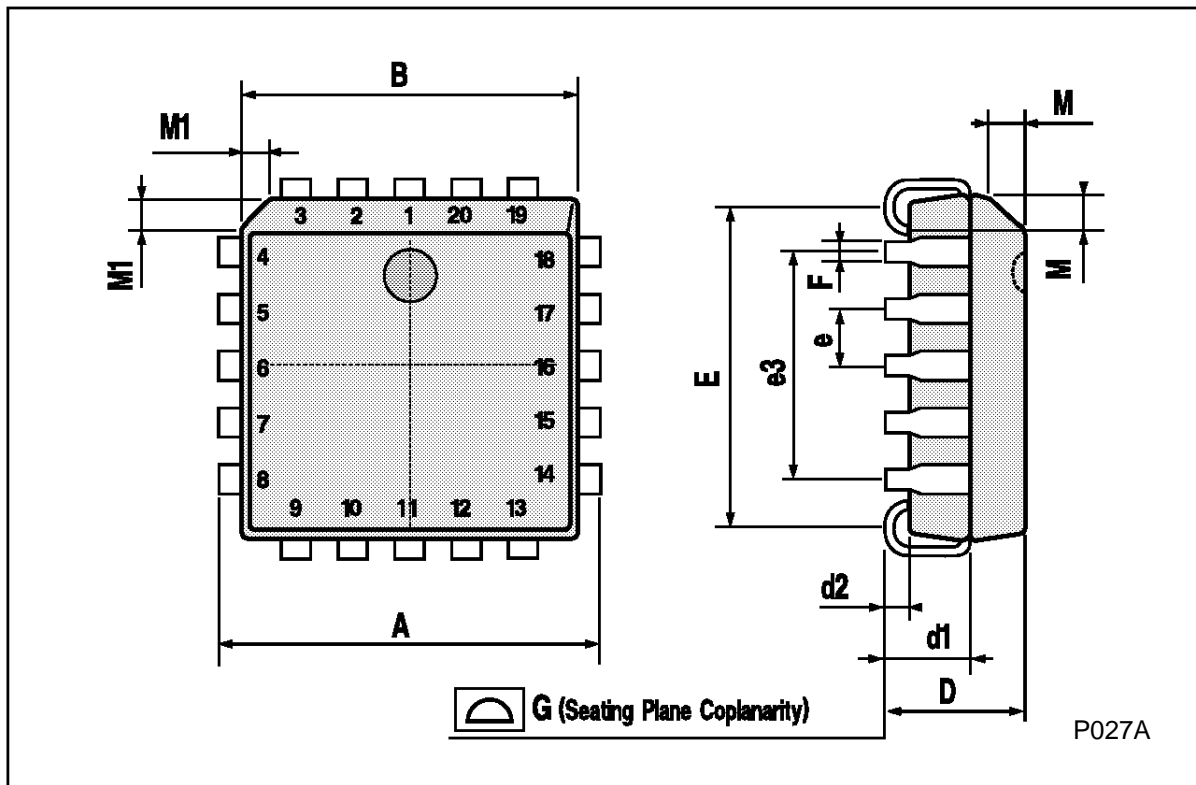
SO20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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