SGSP216/P217
SGSP316/P317
SGSP516/P517

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

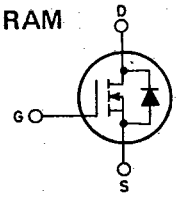
V_{DSS}	$R_{DS(ON)}$	I_D
200V	0.75Ω	6A
250V	1.2 Ω	6A

ABSOLUTE MAXIMUM RATINGS

		SOT-82 TO-220 TO-3	SGSP216 SGSP316 SGSP516	SGSP217 SGSP317 SGSP517
V_{DS}	Drain-source voltage (V_{GS} = 0)		250V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		250V	200V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		6A	
	at T_{case} = 100°C		3.8A	
I_{DM}(•)	Drain current (pulsed)		24A	
I_{DLM} (•)	Drain inductive current, clamped		24A	
		SOT-82	**TO-220**	**TO-3**
P_{tot}	Total dissipation at T_{case} = 25°C	50W	75W	75W
	Derating factor	0.4W/°C	0.6W/°C	0.6W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

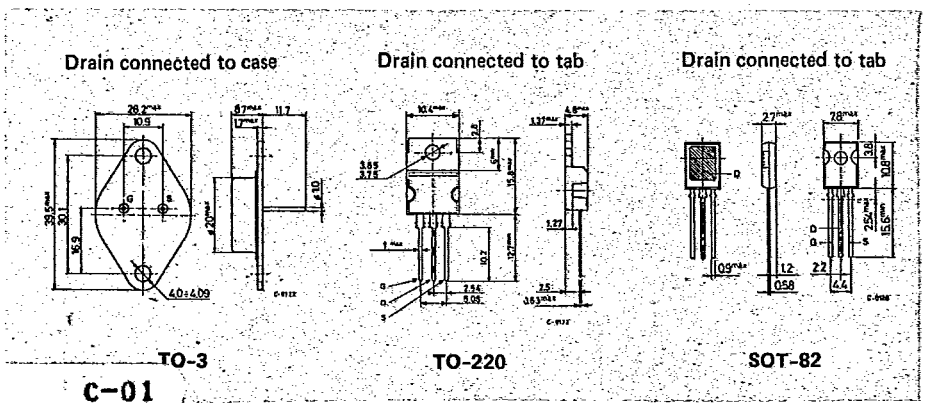
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



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THERMAL DATA

			SOT-82	TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	2.5°C/W	1.6°C/W	1.6°C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for SGSP216/P316/P516 for SGSP217/P317/P517	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 3 A for SGSP216/P316/P516 for SGSP217/P317/P517 V_{GS} = 10 V I_D = 6 A for SGSP216/P316/P516 for SGSP217/P317/P517 V_{GS} = 10 V I_D = 3 A T_{case} = 100°C for SGSP216/P316/P516 for SGSP217/P317/P517			 3.60 2.25 8.10 5.00 7.20 4.50	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3 A for SGSP216/P316/P516 for SGSP217/P317/P517			 1.20 0.75	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 3 A	1.5			mho

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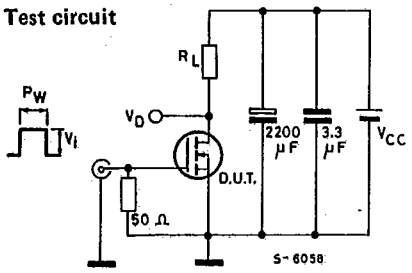
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz		380	500	pF
C_{oss}	Output capacitance	V_{GS} = 0		100	130	pF
C_{rss}	Reverse transfer capacitance			50	65	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 100 V I_D = 2.5 A		27		ns
t_r	Rise time	V_i = 10 V R_i = 50Ω		27		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				6	A
I_{SDM}(•)	Source drain current (pulsed)				24	A
V_{SD}	Forward on voltage	I_{SD} = 6 A V_{GS} = 0			1.3	V
t_{on}	Turn-on time	I_{SD} = 6 A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery time	dI/dt = 100 A/μs		180		ns

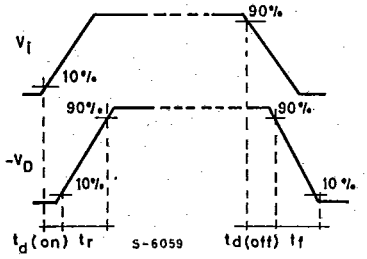
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



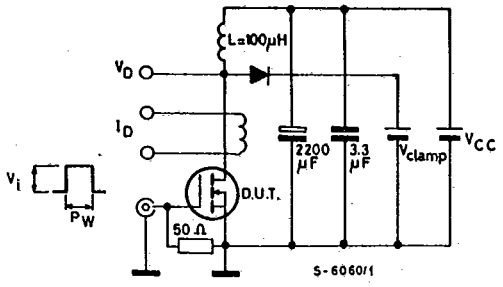
Waveforms



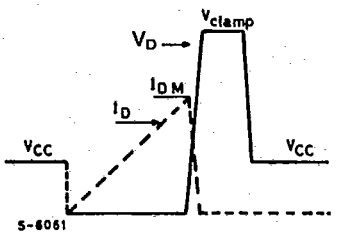
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

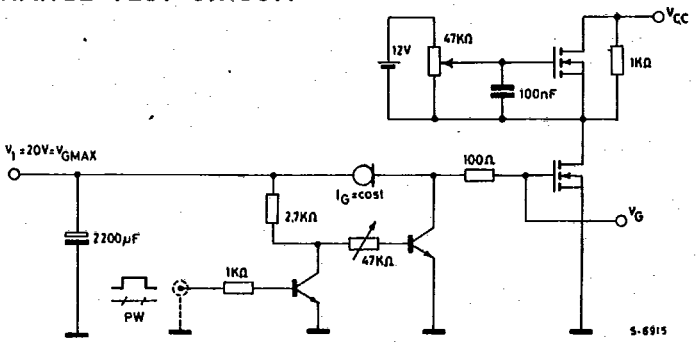


Waveforms



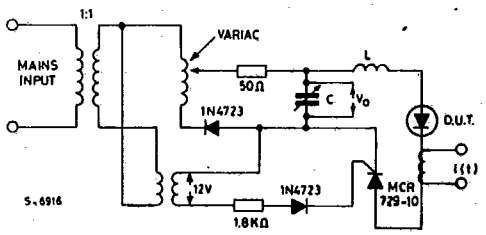
V_i = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT



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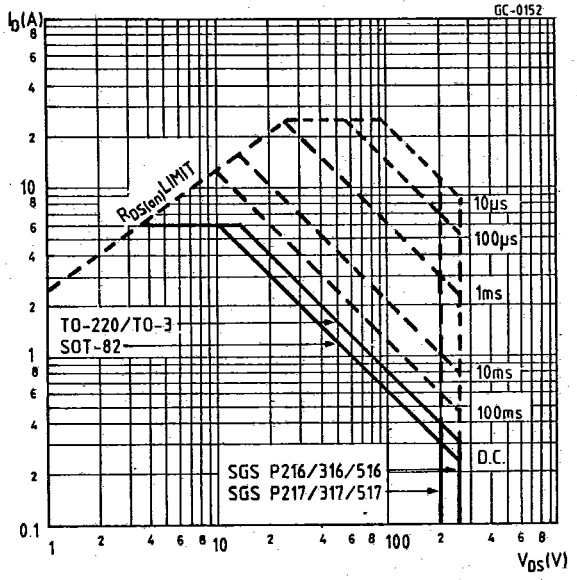
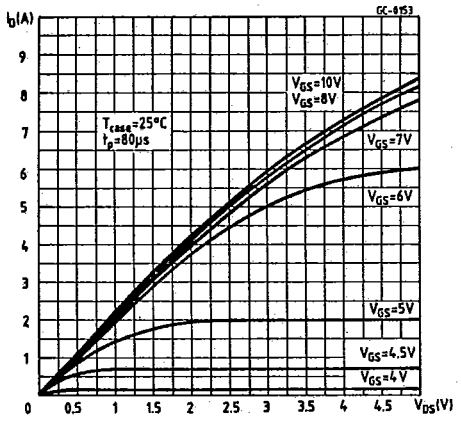
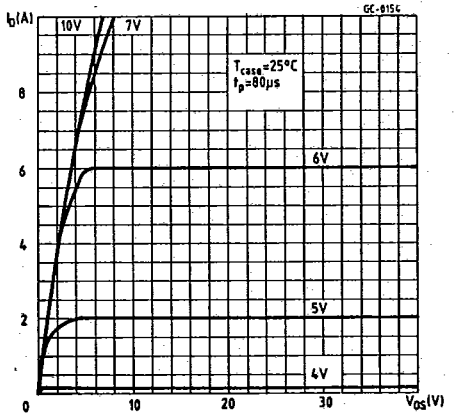
Safe operating areas



Output characteristics



Output characteristics



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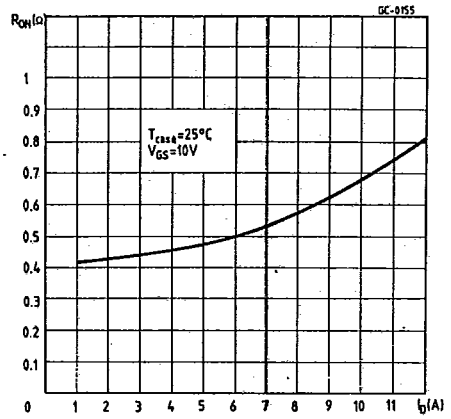
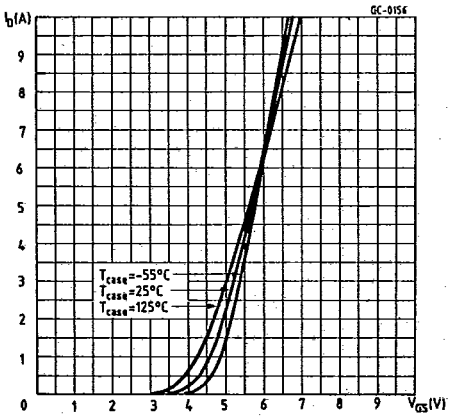
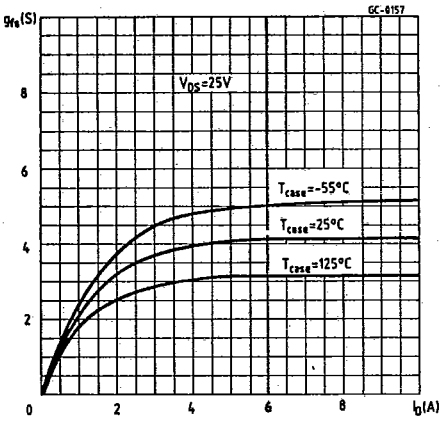
Static drain-source on resistance



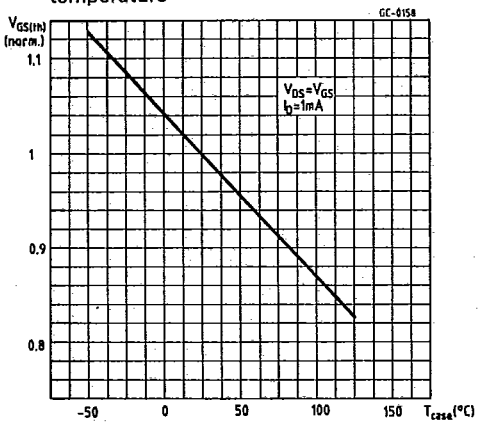
Transfer characteristics



Transconductance



Normalized gate thereshold vs. temperature



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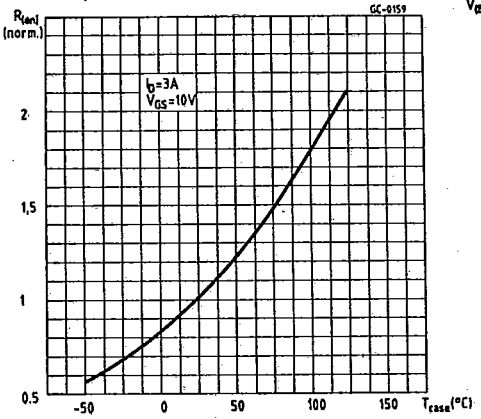
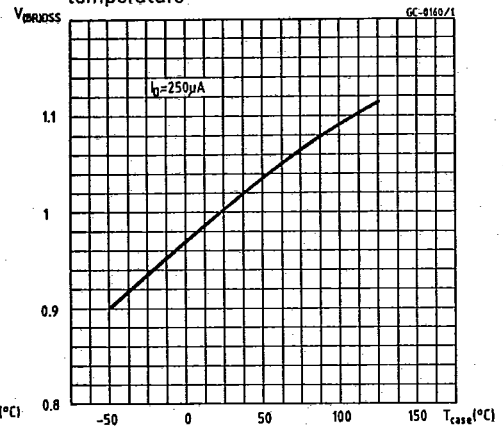
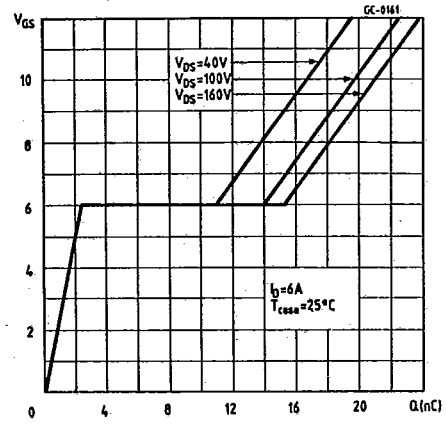
Normalized on resistance vs temperature



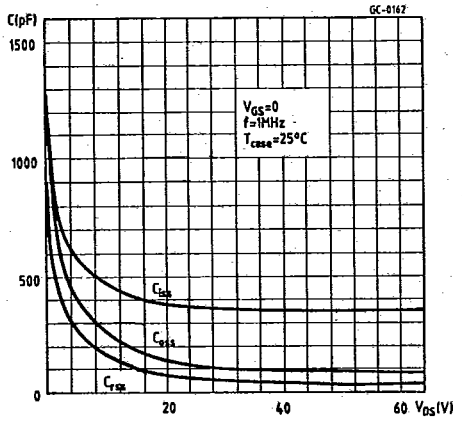
Normalized breakdown voltage vs temperature



Gate charge vs. gate to source voltage



Capacitance variation



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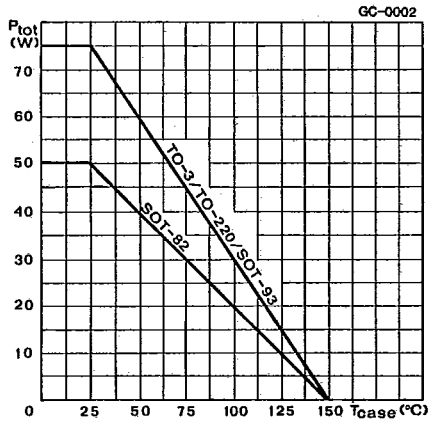
Derating curve



Source-drain diode forward characteristics