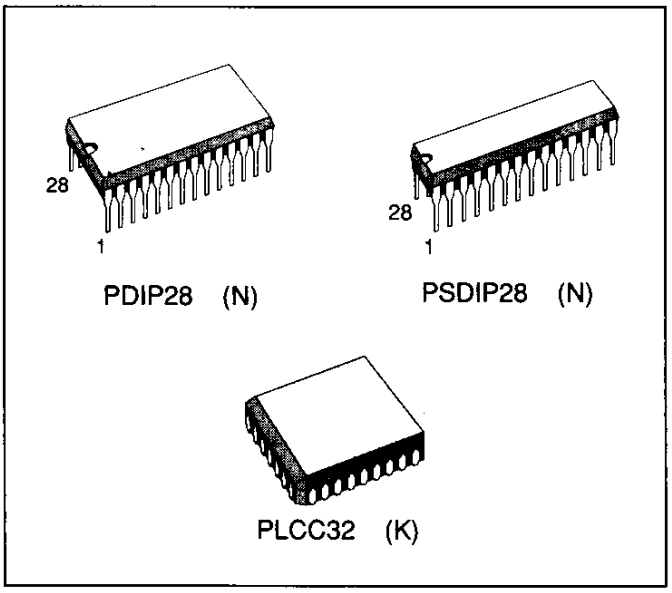
VERY FAST CMOS 512 / 1K / 2K x 9 BiPORT FIFO

- FIRST-IN-FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE x 9 ORGANIZATIONS:
  - MK45H01,11 (512 x 9)
  - MK45H02,12 (1K x 9)
  - MK45H03,13 (2K x 9)
- LOW POWER, HIGH SPEED HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- FULLY EXPANDABLE IN WORD WIDTH AND DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HALF-FULL FLAG IN SINGLE DEVICE MODE



DESCRIPTION

The MK45H01,11,02,12,03,13 are BiPORT™ FIFO memories from SGS-THOMSON Microelectronics, which utilize special two-port memory cell techniques. Specifically, these devices implement a First-In-First-Out (FIFO) algorithm, featuring asynchronous read/write operations, full, empty, and half full status flags, and unlimited expansion capability in both word size and depth. The full and empty flags are provided to prevent data overflow and underflow.

PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
D0-D8	Data Inputs
Q0-Q8	Data Outputs
$\overline{FL}/\overline{RT}$	First Load / Retransmit
$\overline{XI}$	Expansion Input
$\overline{XO}/\overline{HF}$	Expansion Output / Half-full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}, GND	5 Volts, Ground
NC	Not Connected

Figure 1. Pin Connections

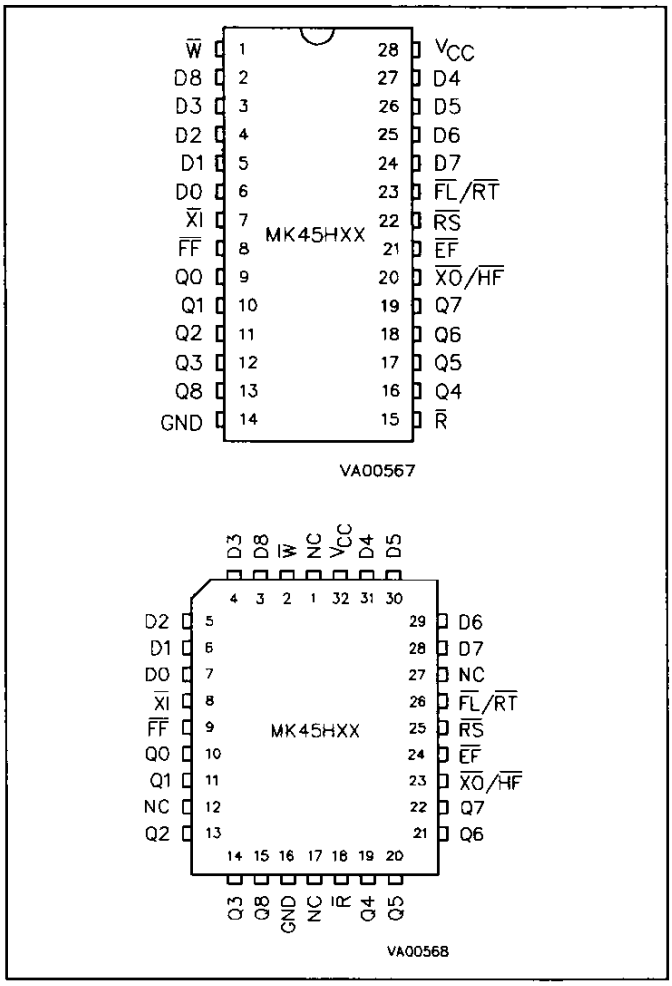
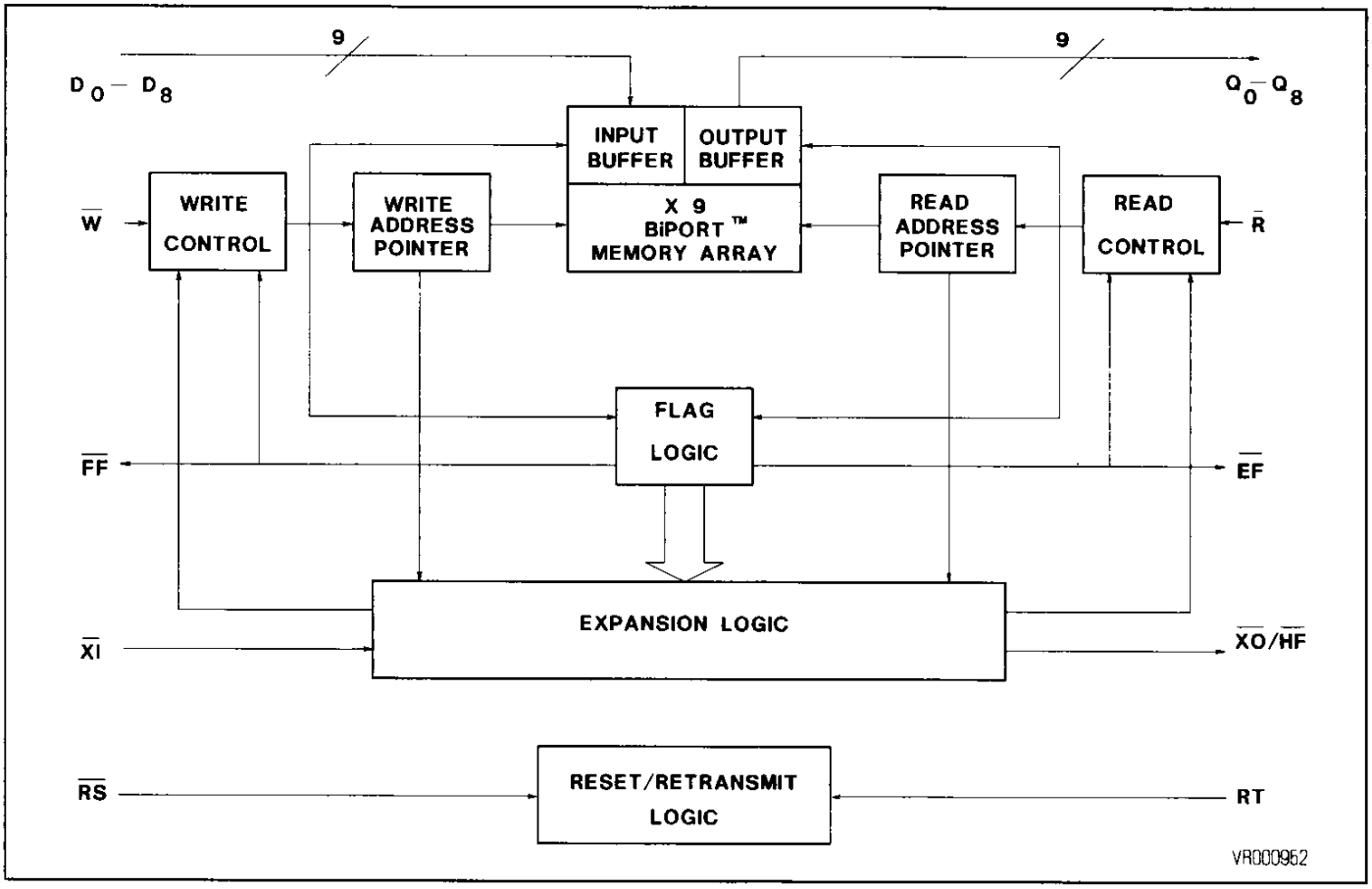


Figure 2. Block Diagram



DESCRIPTION (Continued)

The data is loaded and emptied on a first-in-first-out basis, and the latency for retrieval of data is approximately one load (write) cycle. These devices feature a read/write cycle time of only 35ns (28.5MHz).

The reads and writes are internally sequential through the use of separate read and write pointers in a ring counter fashion. Therefore, no address information is required to load or unload data. Data is loaded and unloaded with the use of $\overline{W}$ (write), and $\overline{R}$ (read) input pins. Separate data in (D0-D8) and data out (Q0-Q8) pins allow simultaneous and asynchronous read/write operations, provided the status flags are not protecting against data underflow or overflow.

The main application of these devices is a buffer for sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The MK45HX1, MK45HX2, and MK45HX3 incorporate 9-bit wide data arrays that provide for support control or parity bit functions. This feature is helpful in data communications where the extra parity bit is used for transmission and reception error checking. These devices also offer retransmit ($\overline{RT}$) and half-full features in single device or width expansion modes. The retransmit function allows data to be re-read by resetting the read pointer while not disturbing the write pointer. This is for applications where the FIFO is not full, or is written with less than 512, 1024, or 2048 words.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK45HX1, MK45HX2, and MK45HX3 employ a memory-based architecture wherein a byte written into the device does not "ripple through". Instead, a byte written into the device is stored in a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Two internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching the final address in the FIFO (512, 1024, or 2048). The empty, half full, and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location.

FUNCTIONAL DESCRIPTION (Continued)

As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

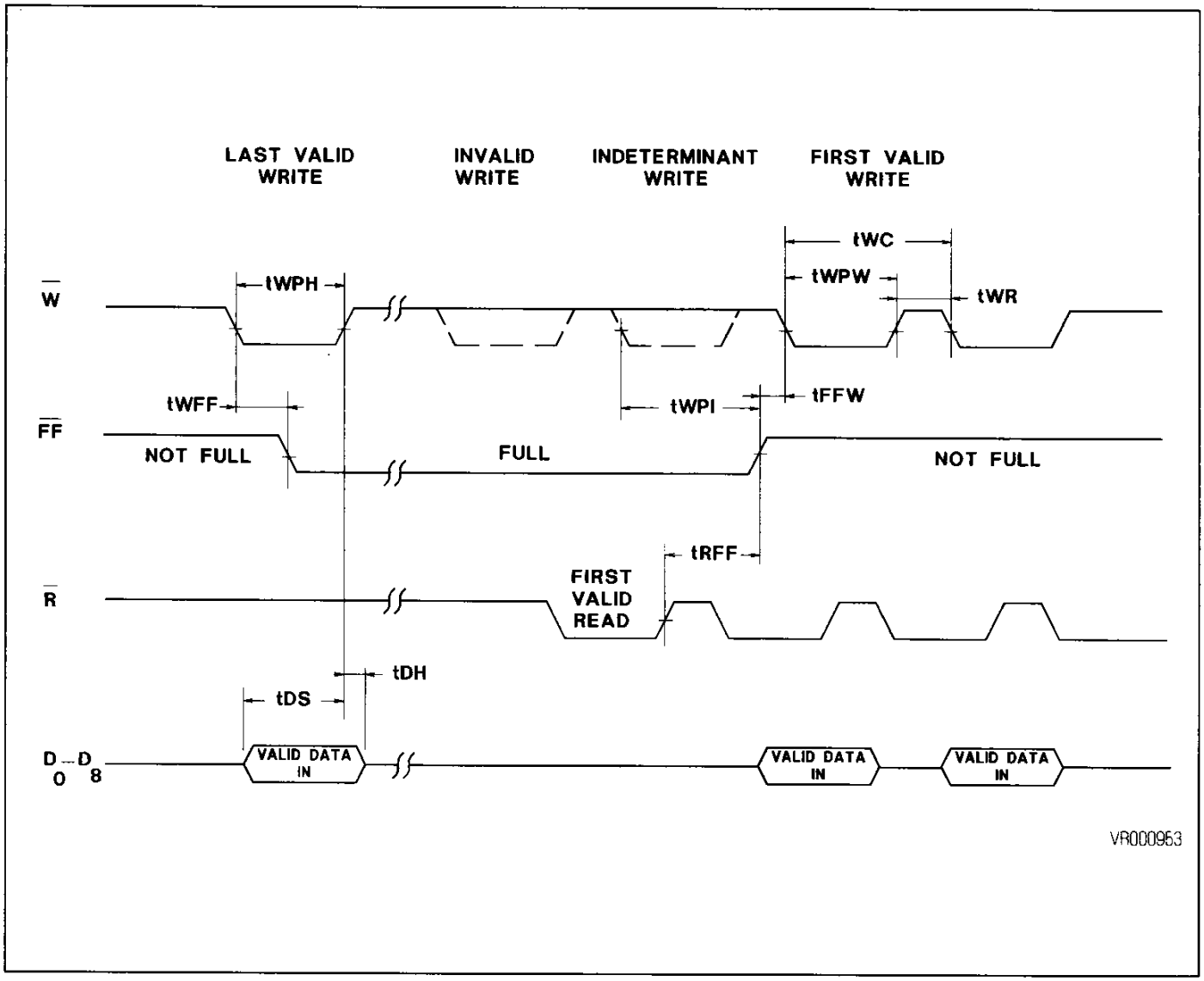
Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without effecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading individual FIFOs. The penalty of cascading is often unacceptable ripple through delays. The MK45HX1, MK45HX2, and MK45HX3 allow implementation of very large FIFOs with no timing penalties. The memory-based architecture of the device allows the connection of the read, write, data in, and data out lines of the device in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

WRITE MODE

The MK45HXX initiates a Write Cycle (see Figure 3) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not set. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is set during the last valid write as the MK45H03 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 5). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on the internal flag status.

Figure 3. Write and Full Flag Waveforms



Write and Full Flag AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

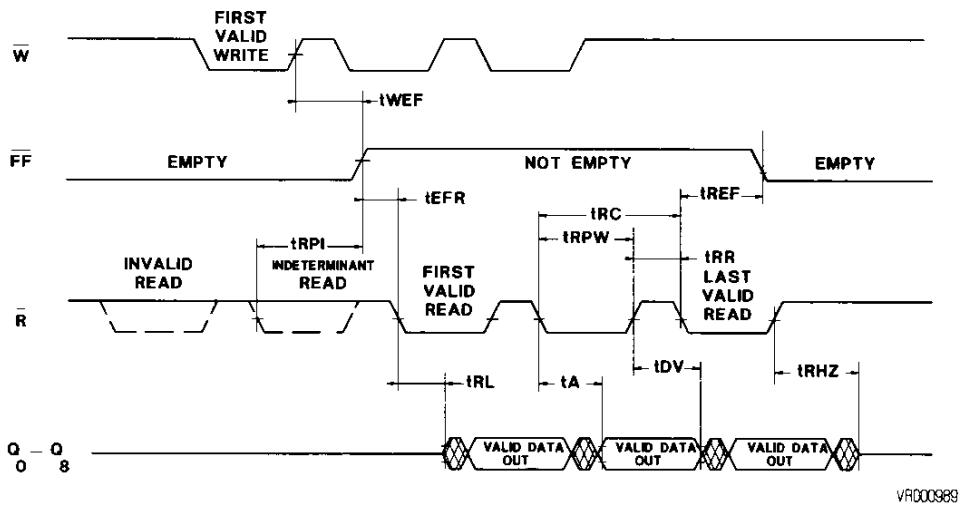
Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	35		45		65		80		140		ns	
t_{WPW}	Write Pulse Width	25		35		50		65		120		ns	1
t_{WR}	Write Recovery Time	10		10		15		15		20		ns	
t_{DS}	Data Set Up Time	15		18		30		30		40		ns	
t_{DH}	Data Hold Time	0		0		0		0		0		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		25		35		45		60		60	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write		10		10		10		10		10	ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		25		35		45		60		60	ns	2
t_{WPI}	Write Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

READ MODE

The MK45HXX initiates a Read Cycle (see Figure 4) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not set. In the read mode of operation, the MK45H0X provides fast access to data from 9 of the locations in the static storage array. The data is accessed on a FIFO basis independent of any on-going WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation. In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data inputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent read operation, provided that a second WRITE has not been completed (see Figure 6). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more that t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less then t_{EFR} later may or may not occur (be valid) depending on internal flag status.

Figure 4. Read and Empty Flag Waveforms



Read and Empty Flag AC Operating Conditions
(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	35		45		65		80		140		ns	
t_A	Access Time		25		35		50		65		120	ns	2
t_{RR}	Read Recovery Time	10		10		15		15		20		ns	
t_{RPW}	Read Pulse Width	25		35		50		65		120		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		18		20		25		25		35	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		25		35		40		60		60	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read		10		10		10		10		10	ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		25		35		45		60		60	ns	2
t_{RPI}	Read Protect Indeterminant	10		10		10		10		10		ns	2

Notes: 1. Pulse widths less than minimum values are not allowed
2. Measured using equivalent output load circuit

Figure 5. Read/Write to Full Flag Waveforms

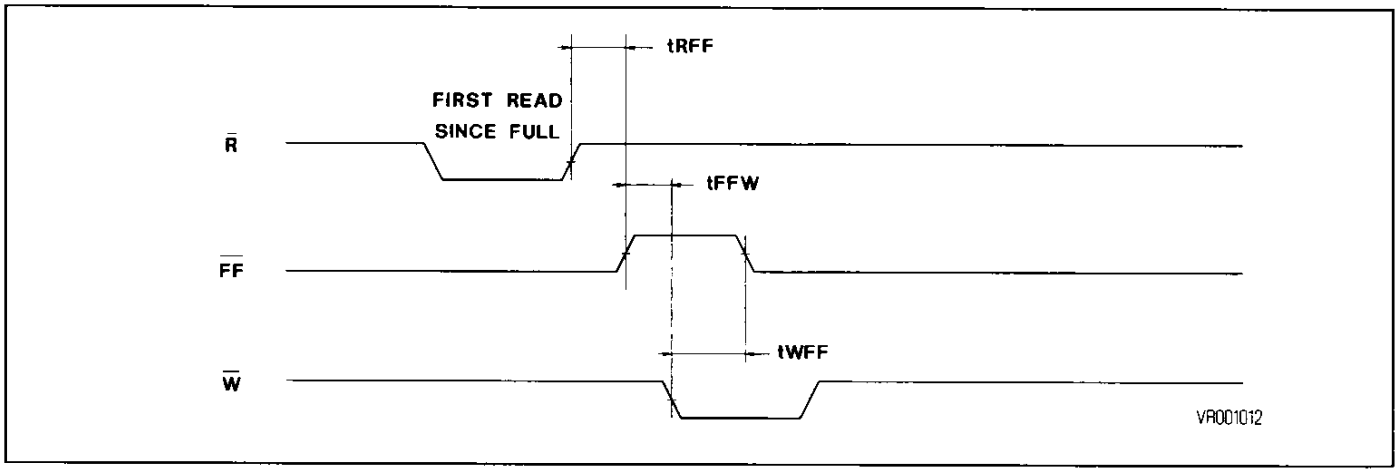
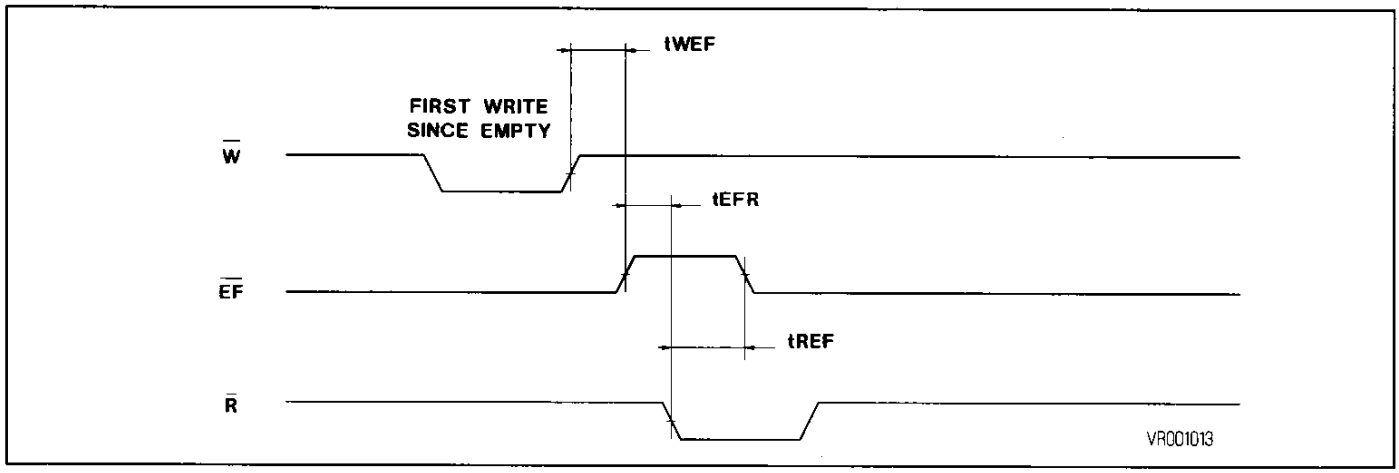


Figure 6. Write/Read to Empty Flag Waveforms

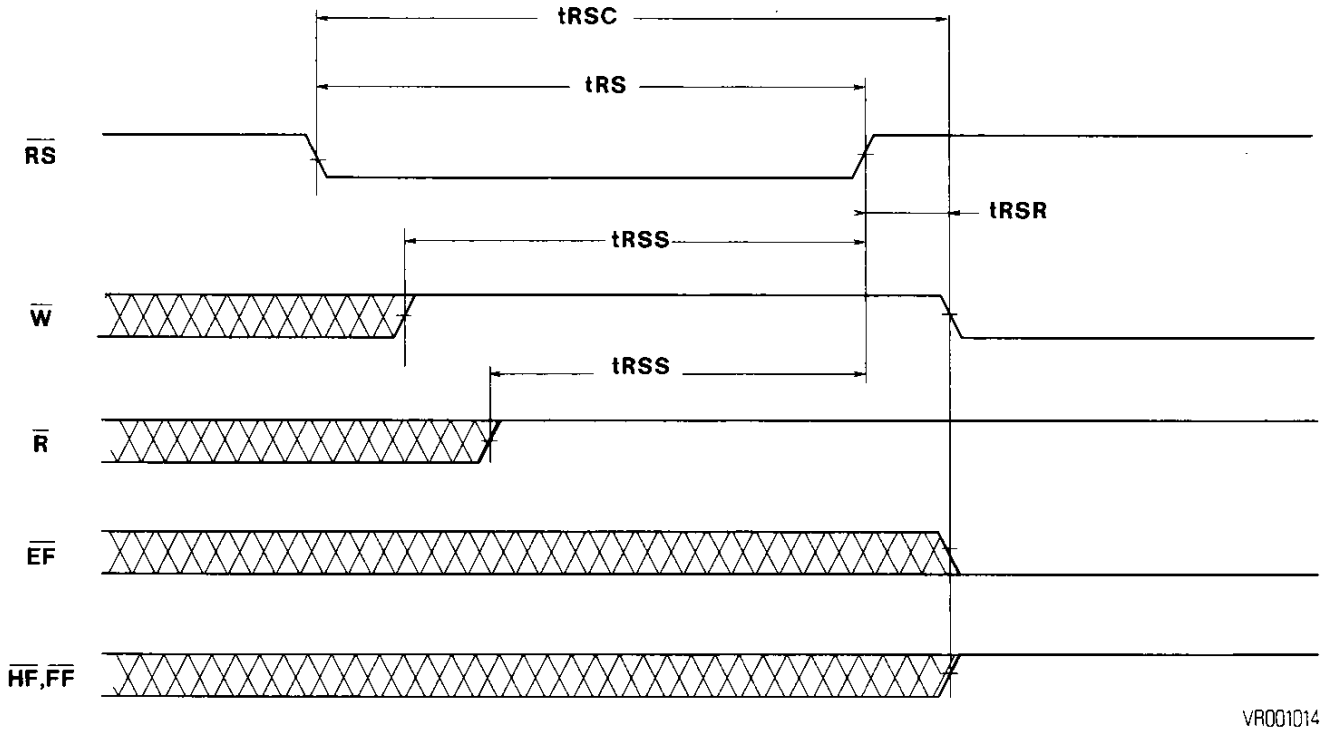


RESET

The MK45HXX is reset (see Figure 7) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a WRITE operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{R}$ and $\overline{W}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

Figure 7. Reset Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

Reset AC Operating Conditions ($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	Reset Cycle Time	35		45		65		80		140		ns	
t_{RS}	Reset Pulse Width	25		35		50		65		120		ns	1
t_{RSR}	Reset Recovery Time	10		10		15		15		20		ns	
t_{RSS}	Reset Set Up Time	25		30		30		45		100		ns	

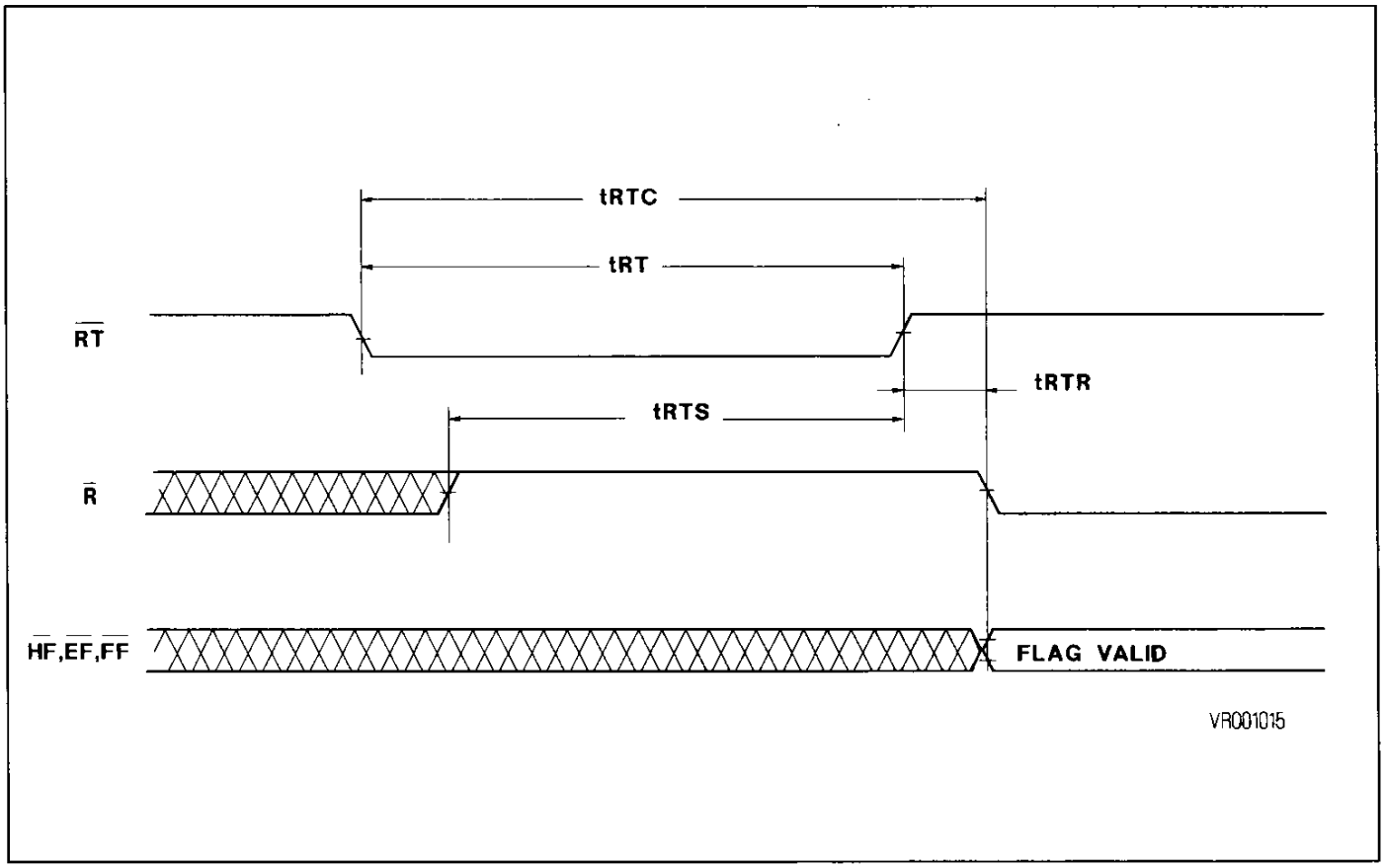
Note: 1. Pulse widths less than minimum values are not allowed

RETRANSMIT

The MK45HXX can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 8). A Retransmit operation sets the internal read pointer to the first location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than the total FIFO depth are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

Figure 8. Retransmit Waveforms



Note : $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Retransmit AC Operating Conditions

($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RTC}	Retransmit Cycle Time	35		45		65		80		140		ns	
t_{RT}	Retransmit Pulse Width	25		35		50		65		120		ns	1
t_{RTR}	Retransmit Recovery Time	10		10		15		15		20		ns	
t_{RTS}	Retransmit Set Up Time	25		30		30		45		100		ns	

Note: 1. Pulse widths less that minimum values are not allowed

SINGLE DEVICE CONFIGURATION

A single MK45HXX may be used when application requirements are for a depth of the device depth or less. The MK45HXX is placed in the Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 9).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two MK45HXXs. Any word width can be attained by adding additional MK45HXXs. The half full flag ($\overline{HF}$) operates the same as in single device configuration.

Figure 9. A Single MK45HXX FIFO Configuration

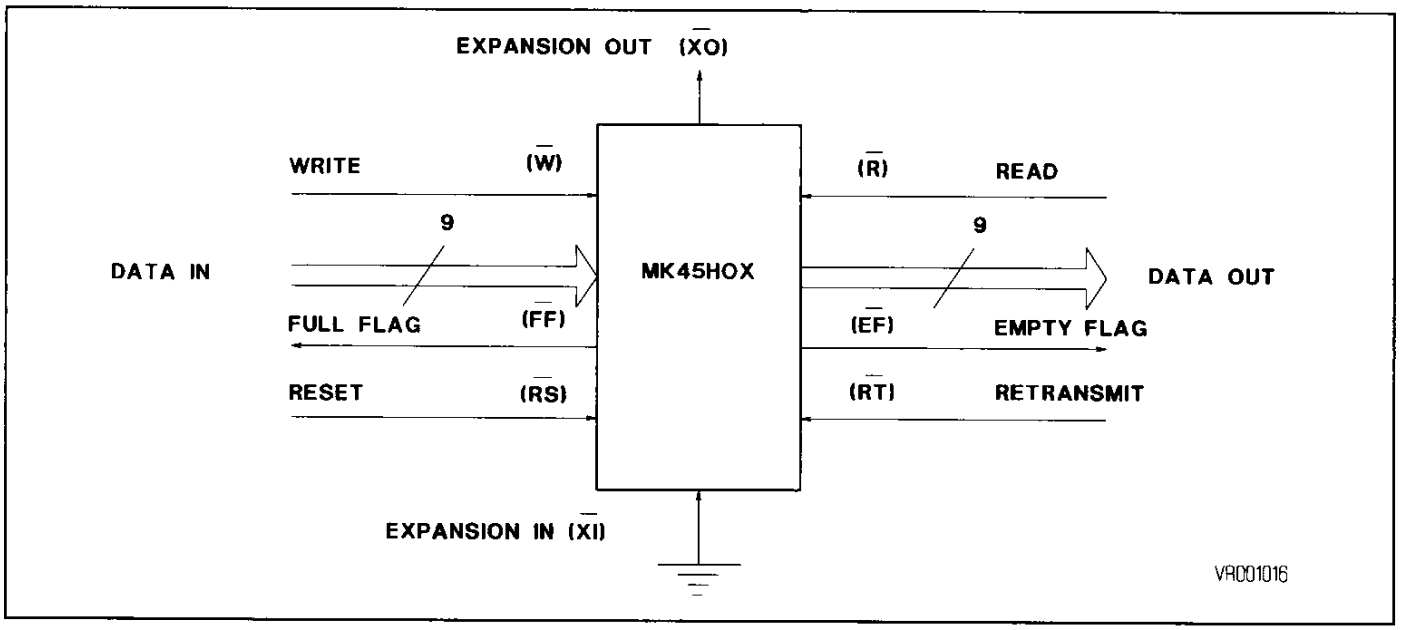
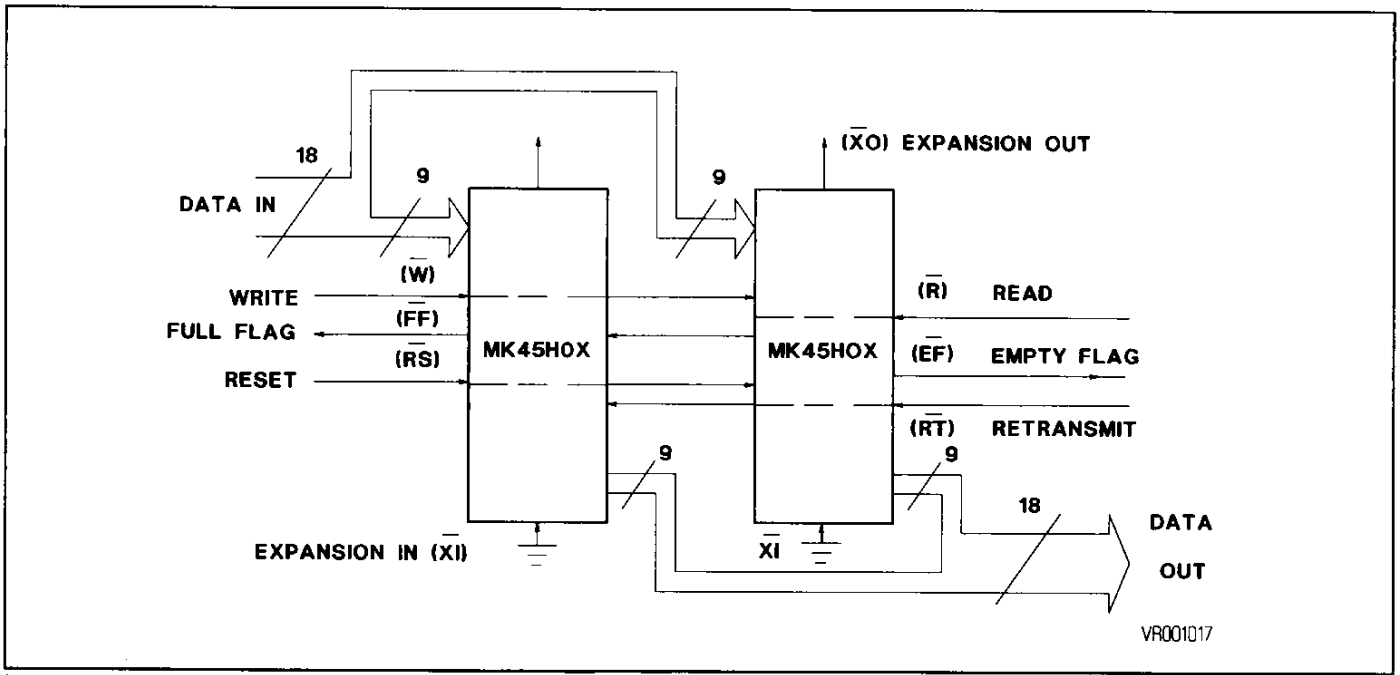


Figure 10. A Two Device Width Expansion FIFO Configuration



Note : Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

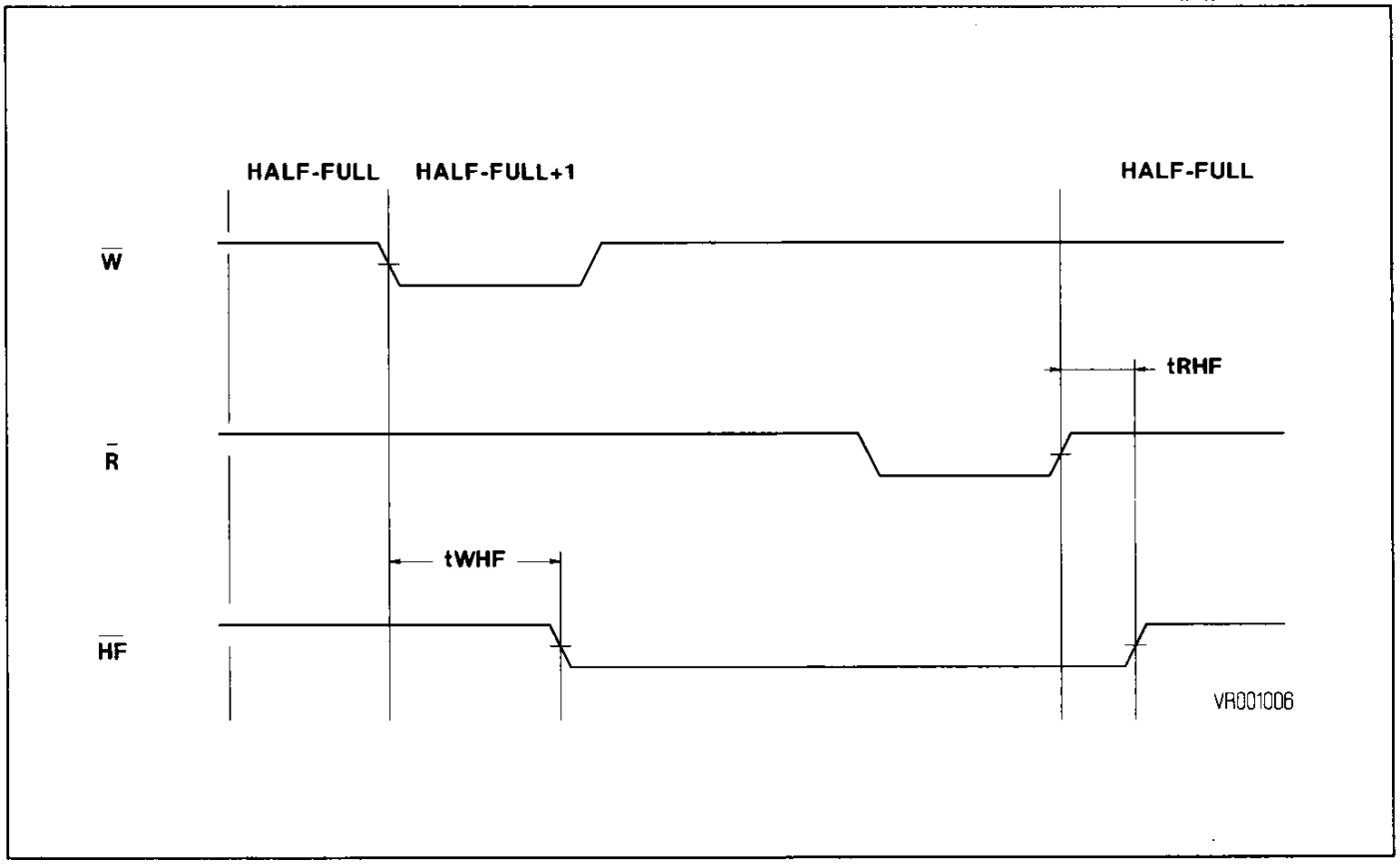
When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation (see Figure 11).

DEPTH EXPANSION (Daisy Chain)

The MK45HXX can be easily adapted to applications when the requirements are greater than the individual device word depth. Figure 12 demonstrates Depth Expansion using two MK45HXXs. Any depth can be attained by adding additional MK45HXXs.

External logic is needed to generate a composite Full and Empty Flag. This requires the ORing of all the $\overline{EF}$s and the ORing of all the $\overline{FF}$s (i.e., all must be set to generate the composite $\overline{FF}$ or $\overline{EF}$).

Figure 11. Half Full Flag Waveforms



Half Full Flag AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WHF}	Write Low to Half Full Flag Low		30		35		45		60		60	ns	
t_{RHF}	Read High to Half Full Flag High		30		35		45		60		60	ns	

The MK45HXX operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions :

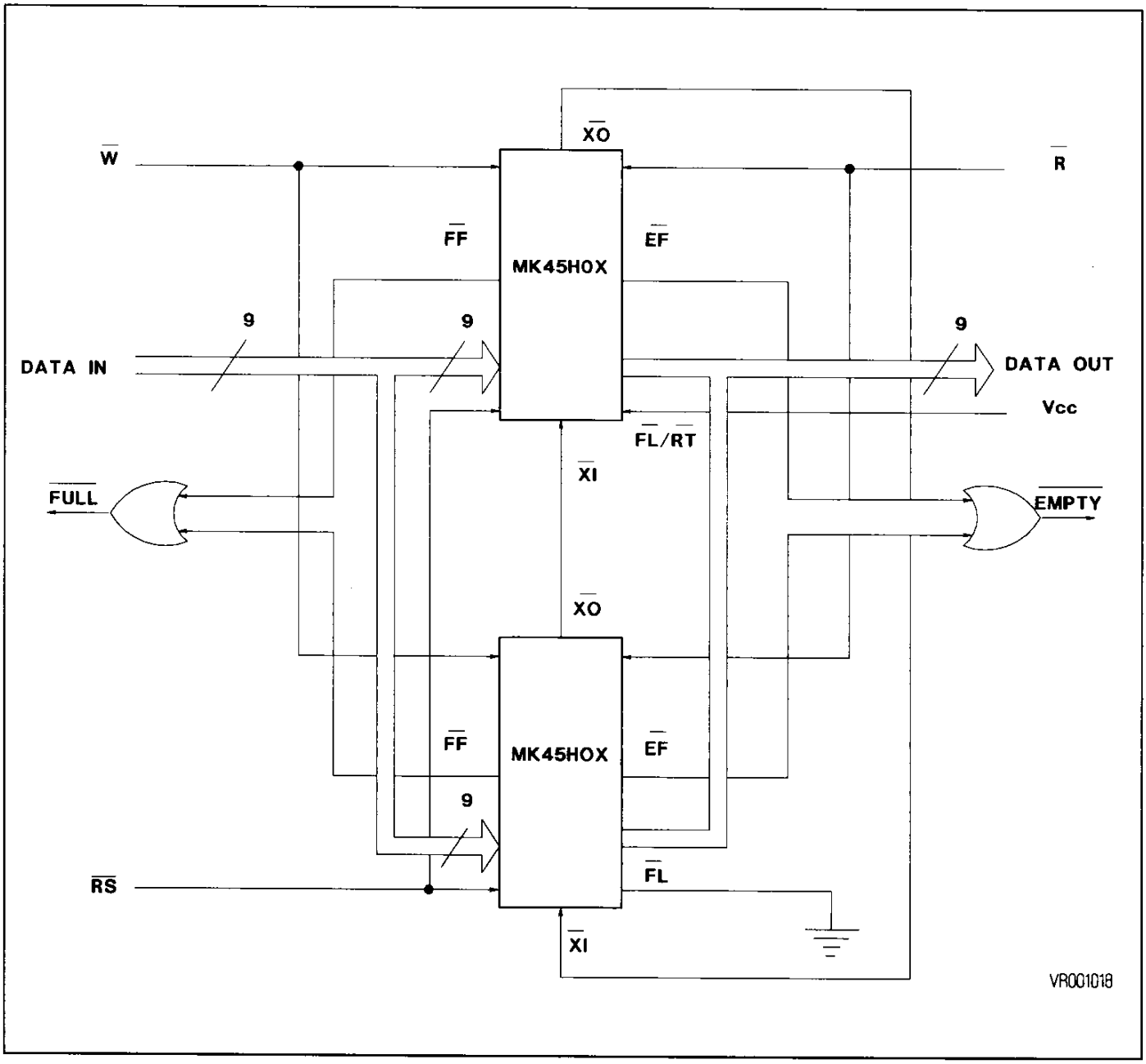
1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not available in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

EXPANSION TIMING

Figures 13 and 14 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Due to the fact that Expansion Out pins are generally connected only to Expansion In pins, the user does not need to be concerned with the actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the identical to the WRITE and READ signals but ; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

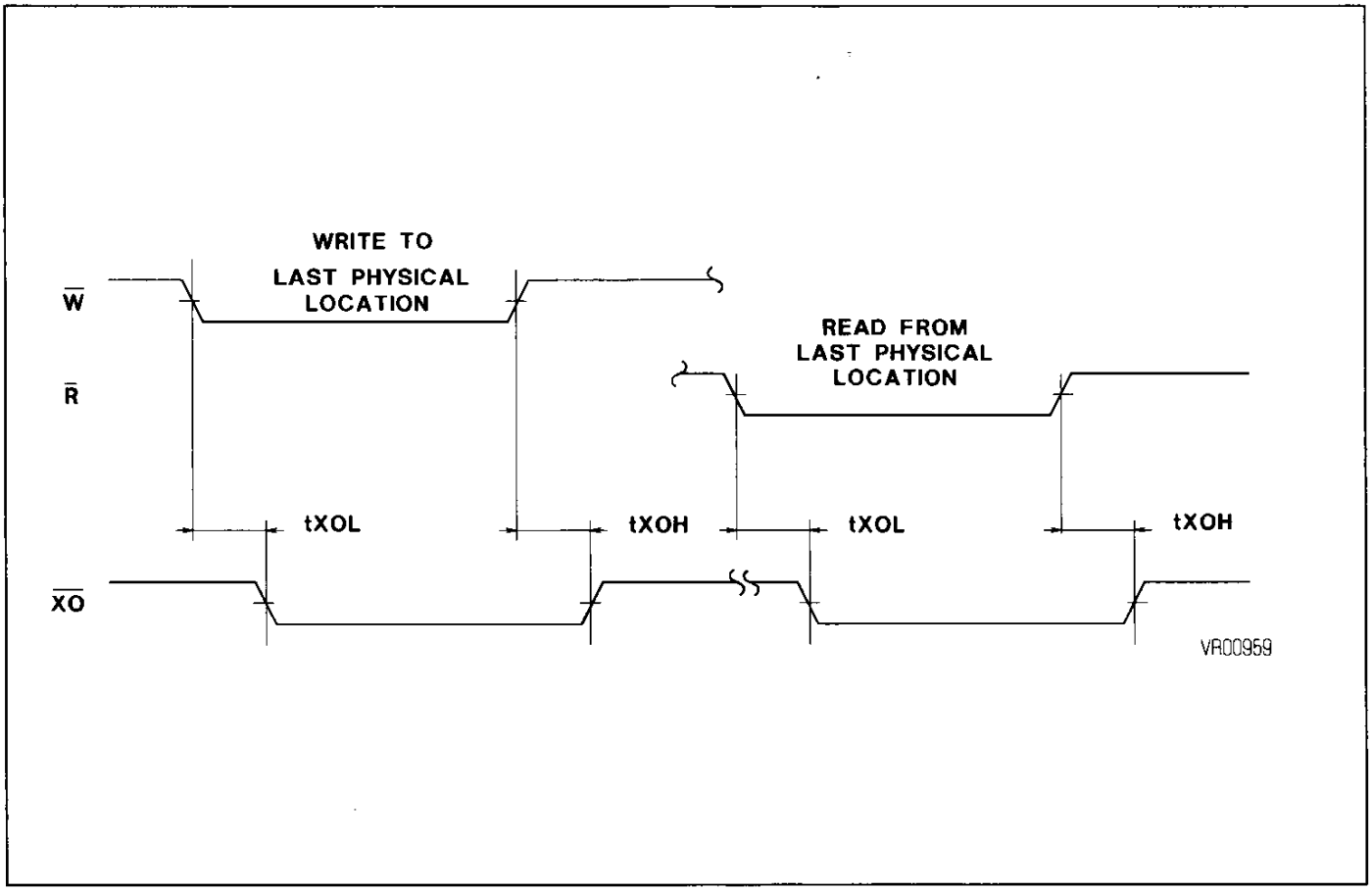
Figure 12. A Two Device Depth Expansion Configuration



When in Depth Expansion mode, a given MK45HXX will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK45HXX in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs.

It will not begin reading until a second Expansion In pulse and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

Figure 13. Expansion Out Waveforms

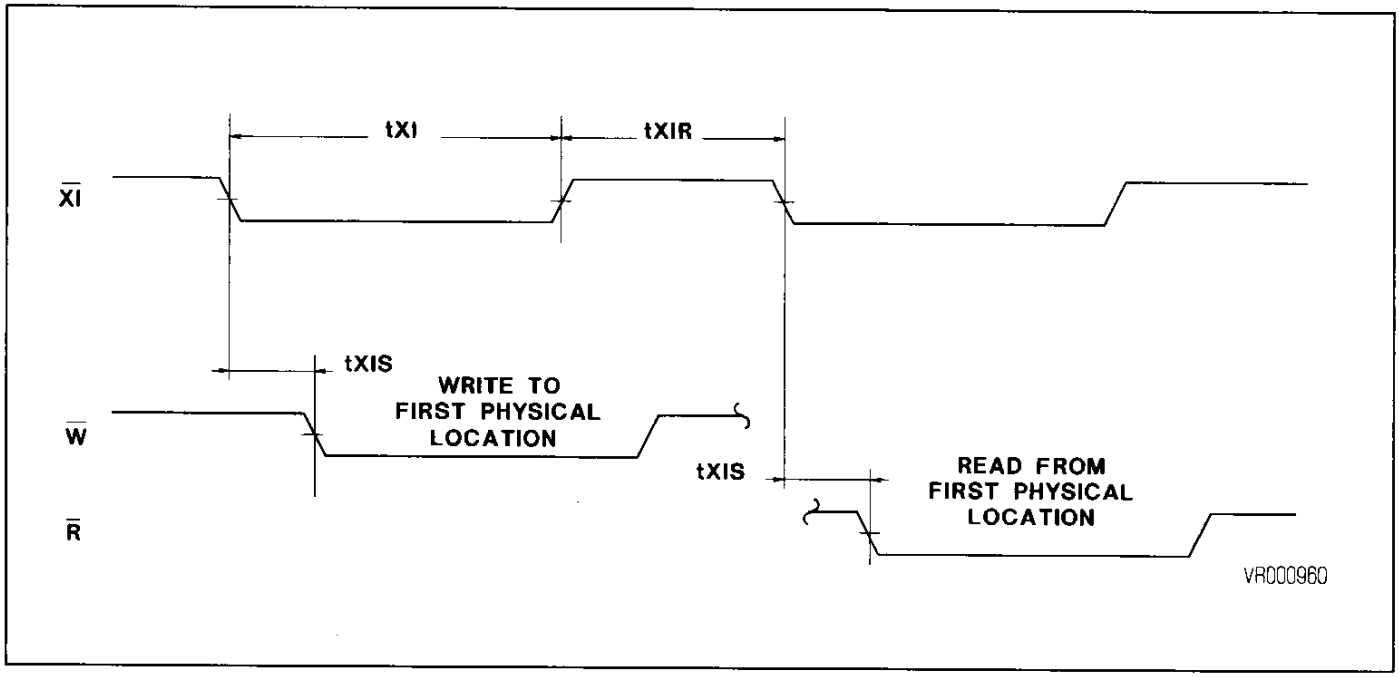


Expansion Out AC Operating Conditions

(0°C ≤ T_A ≤ +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XOL}	Expansion Out Low		25		35		40		55		90	ns	
t_{XOH}	Expansion Out High		25		35		40		55		90	ns	

Figure 14. Expansion In Waveforms



Expansion In AC Operating Conditions

($0°C \leq T_A \leq +70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	-25		-35		-50		-65		-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{XI}	Expansion in Pulse Width	25		35		45		60		115		ns	1
t_{XIR}	Expansion In Recovery Time	10		10		10		10		10		ns	
t_{XIS}	Expansion In Setup Time	15		15		15		15		15		ns	

Note: 1. Pulse widths less than minimum values are not allowed

COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK45HXXs, as shown in Figure 16. Care must be taken to ensure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used ; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

Figure 15. Compound FIFO Expansion Configuration

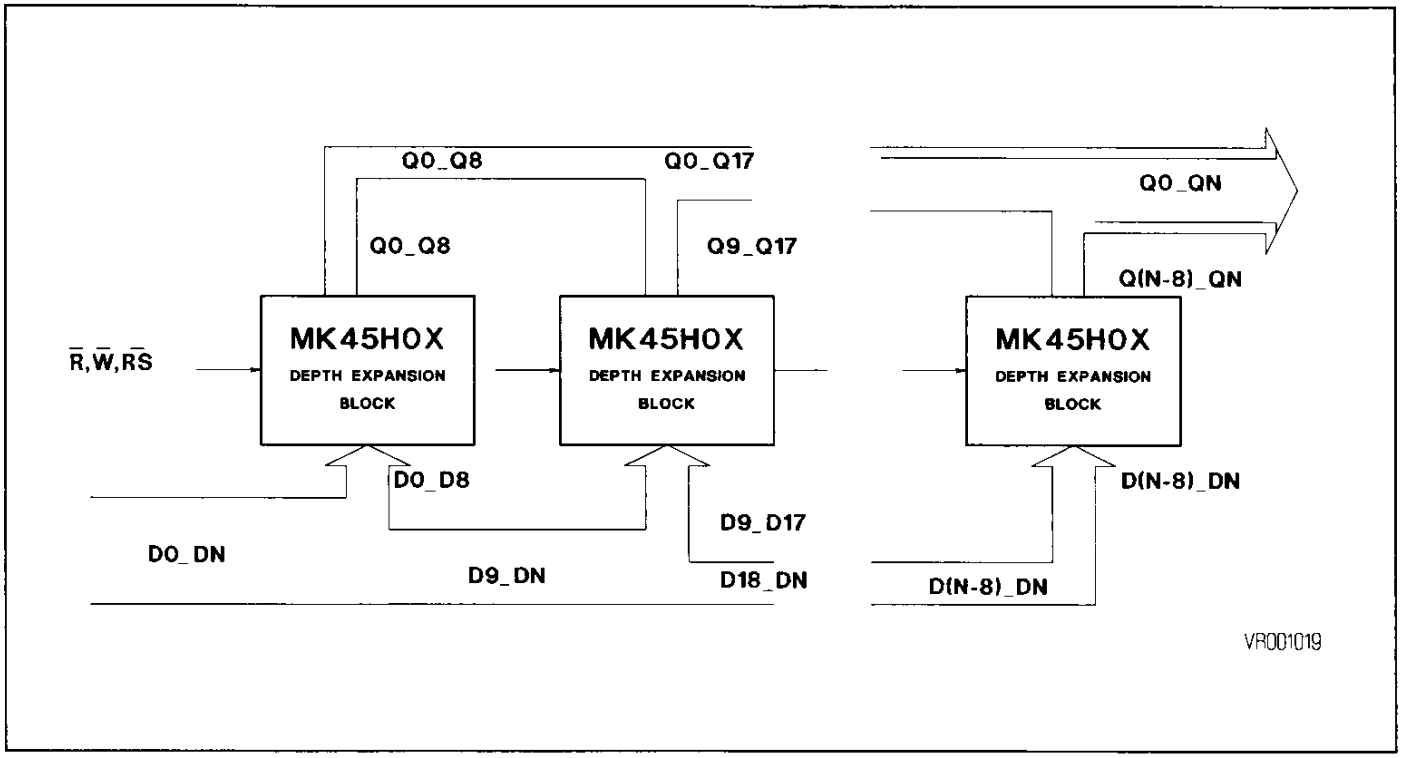
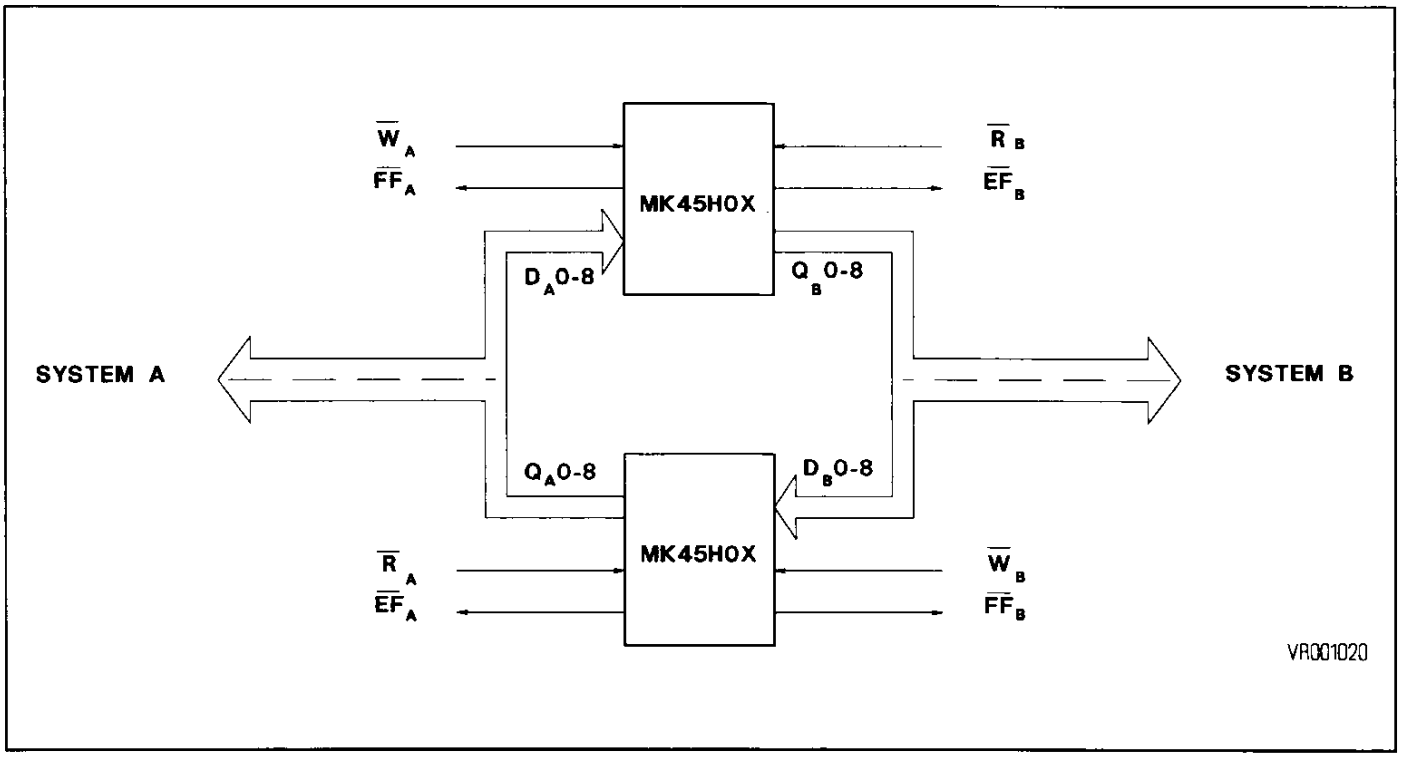


Figure 16. Bidirectional FIFO Application



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	–0.3 to +7	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	20	mA

Note : This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this spefication in not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq +70°C$)

Symbol	Parameter	Min.	Max.	Units	Note
V_{CC}	Supply Voltage	4.5	5.5	V	1
GND	Ground	0	0	V	
V_{IH}	Logic 1 All Inputs	2	V_{CC} + 0.3	V	1,2
V_{IL}	Logic 0 All Inputs	–0.3	0.8	V	1

Notes: 1. All Voltages are referenced to ground
2. V_{IH} = 2.5V on the RS pin for MK45H01,11, 02,12

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$, V_{CC}= +5V± 10%)

Symbol	Parameter	Min.	Max.	Units	Note
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	1
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ /$\overline{RT}$ = V_{IH})		12	mA	1
I_{CC3}	Power Down Current (Inputs ≥ V_{CC} -0.2V)		2	mA	1
I_{IL}	Input Leakage Current (Any Input)	–1	1	µA	2
I_{OL}	Output Leakage Current	–10	10	µA	3
V_{OH}	Output Logic 1 Voltage (I_{OUT} = -4.0mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 8.0mA)		0.4	V	4

Notes : 1. I_{CC} measurements are made with outputs open.
2. Measured with $0.4V \leq V_{IN} \leq V_{CC}$.
3. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
4. All voltages are referenced to ground.

CAPACITANCE (T_A= 25°C, f= 1MHz)

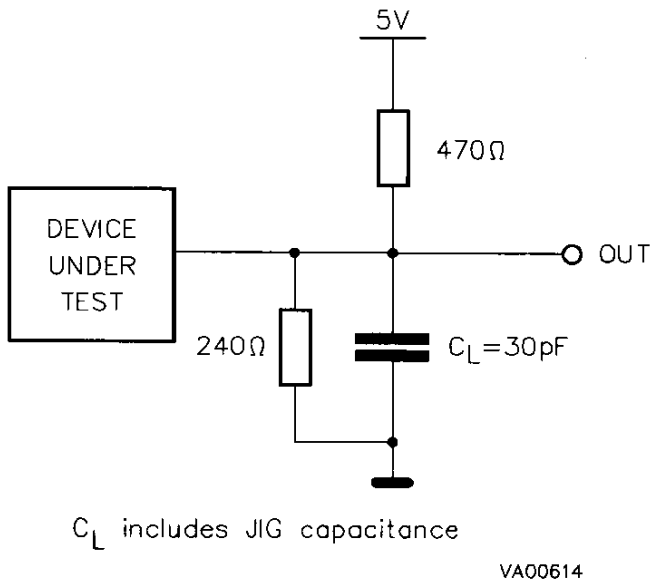
Symbol	Parameter	Typ.	Max.	Unit	Note
C_1	Capacitance on Input Pins		8	pF	1
C_0	Capacitance on Output Pins		12	pF	1,2

Notes : 1. This parameter is only sampled and not 100% tested
2. Output buffer deselected

AC TEST CONDITIONS

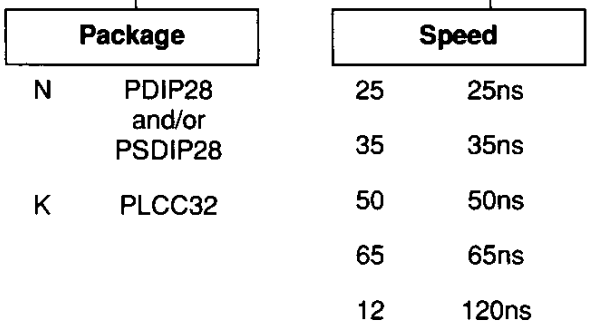
Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	5	ns
Input Signal Timing Reference Level	1.5	V
Output Signal Timing Reference Levels	1.5 and 1.9	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ±10%	V

Figure 17. Equivalent Output Load Circuit



ORDERING INFORMATION

Example: MK45H02 N 25



For a list of available options of Package and Speed, refer to the Selector Guide in this Data Book or to the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact our Sales Office nearest you.