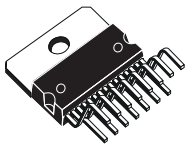
L5950

MULTIPLE MULTIFUNCTION VOLTAGE REGULATOR FOR CAR RADIO

- 5 REGULATORS
  10V (350mA); 8.5V (175mA); 5V (350mA); 5V (250mA); 8V/10V (1A)
- ALL REGULATORS ARE LOW DROPOUT OUPUTS
- 3 HIGH SIDE DRIVERS:
  2A (HSD1), 0.45A (HSD2 & HSD3)
- NO EXTERNAL CHARGE PUMP CAPACITORS ARE REQUIRED
- STAND BY MODE CONTROLLED BY 3 INPUT PINS:
  ENABLE FOR REG2 AND REG3,
  I^2C BUS FOR REG1, REG4, REG5, HSD1, HSD2, HSD3
- INDIVIDUAL THERMAL SHUTDOWN
- INDEPENDENT CURRENT LIMITING
- SHORT CIRCUIT PROTECTION
- LOAD DUMP PROTECTION AND OVERVOLTAGE SHUTDOWN
- ESD PROTECTED



Multiwatt15

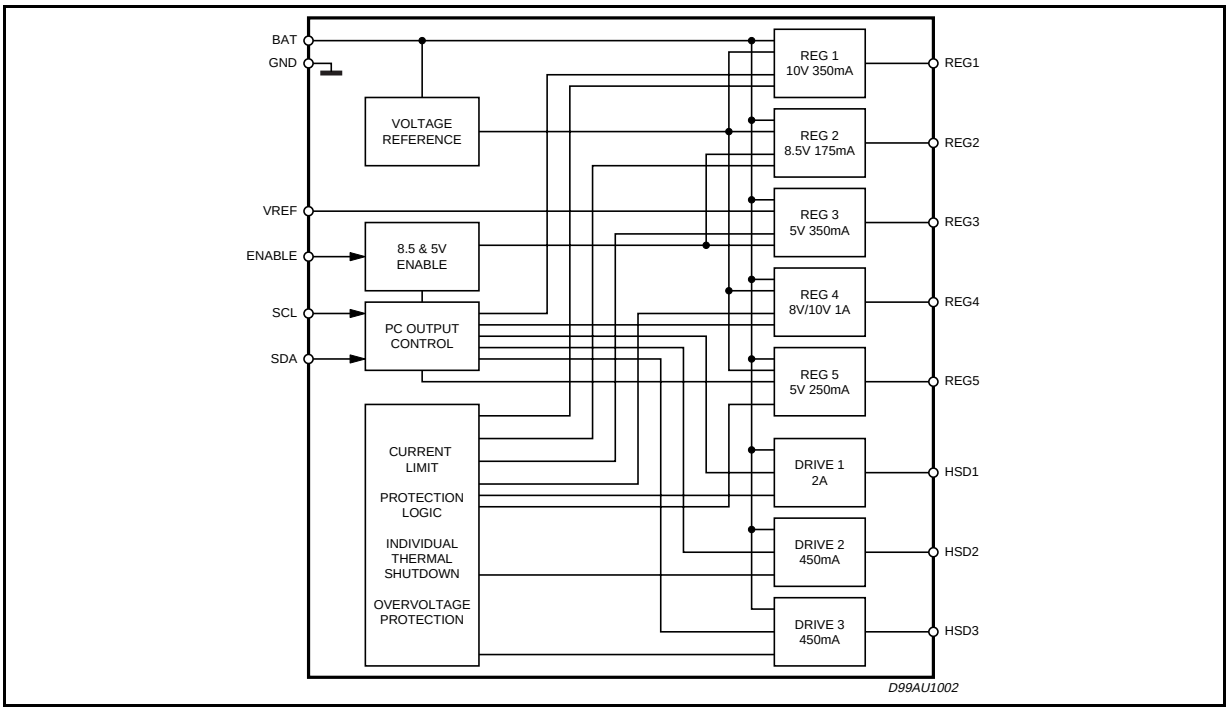
DESCRIPTION

The ASPM (Audio System Power Module) is an integration of three high side drivers and five regulators developed to provide the power for an audio system.

The outputs of the IC are controlled via the I^2C bus and the Enable input.

External protection must be provided for reverse battery protection.

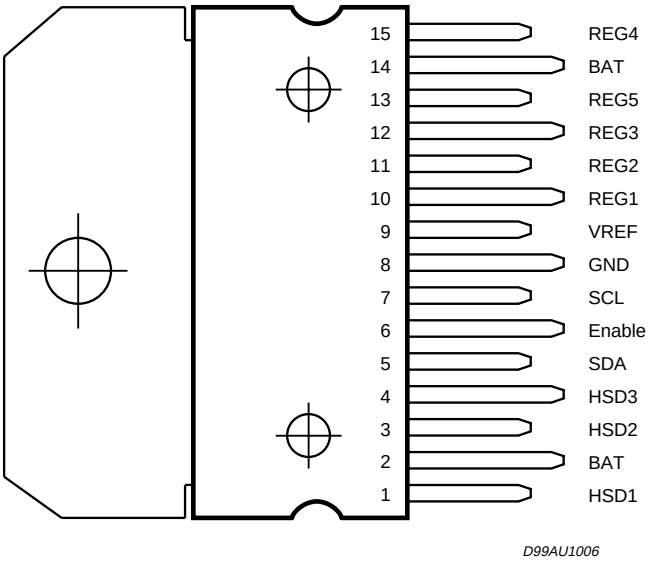
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Operating Supply Voltage	-0.6 to 26.5	V
V_S	Transient Supply Overvoltages, rise time = 10ms delay time = 115ms	34	V
V_{in}	Input Voltages (EN, SDA, SCL)	-0.6 to 9	V
V_{out}	Output Control Voltage	-0.6 to 6.0	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-40 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
Rth j-case	Thermal Resistance Junction-case	2	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_S = 14.4V; T_{amb} = 25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{q,ST-BY}$	Standby Quiescent Current	All Outputs Off, V_{BAT} = 14V			2	µA
I_q	Maximum Quiescent Current	V_{BAT} = 14V, I_{REG1} = 350mA, I_{REG2} = 175mA, I_{REG3} = 350mA, I_{REG4} = 1A, I_{REG5} = 250mA, I_{HSD1} = 2A, $I_{HSD2,3}$ = 450mA			150	mA
I_{EN}	Enable Input Current	V_{BAT} = 14V, Enable ≥ 2V V_{BAT} = 14V, Enable ≥ 0.8V	 -10		10	µA µA
V_{IL}, V_{IH}	Enable Threshold Voltage	V_{BAT} = 14V, V_{IL} V_{BAT} = 14V, V_{IH}	 2		0.8	V V
10V/350mA REG 1 OUTPUT						
V_{REG1}	Output Voltage	I_{REG1} = 350mA 11V ≤ V_{CC} ≤ 16V	9.50	10	10.5	V
ΔV_{line}	Line Regulation	11V ≤ V_{CC} ≤ 26V (Measure Δ V_{REG1} Across V_{CC} Range)			55	mV
ΔV_{load}	Load Regulation	5mA ≤ I_{REG1} ≤ 350mA			55	mV
$V_{DROPOUT}$	Dropout Voltage (Measure V_{BAT}- V_{REG1} when V_{REG1} drops 0.1V)	(Measure V_{BAT}- V_{REG1} when V_{REG1} drops 0.1V) I_{REG1} = 350mA I_{REG1} = 5mA			 900 300	 mV mV
I_{lim1}	Current Limit		0.51		1.1	A
SVR	Ripple Rejection	f_o = 1kHz, V_{BAT} = 14V with 1Vpp AC I_{REG1} = 175mA	50			dB
8.5V/175mA REG 2 OUTPUT						
V_{REG2}	Output Voltage	I_{REG2} = 175mA 9.5V ≤ V_{BAT} ≤ 16V	8.3	8.5	8.7	V
ΔV_{line}	Line Regulation	9.5V ≤ V_{BAT} ≤ 26V (Measure Δ V_{REG2} Across V_{BAT} Range)			50	mV
ΔV_{load}	Load Regulation	5mA ≤ I_{REG2} ≤ 175mA			50	mV
$V_{DROPOUT}$	Dropout Voltage	(Measure VBAT- V_{REG2} when V_{REG2} drops 0.1V) I_{REG2} = 175mA I_{REG2} = 5mA			 900 300	 mV mV
I_{lim2}	Current Limit		280		525	mA
SVR	Ripple Rejection	f_o = 1kHz, V_{BAT} = 14V with 1Vpp AC I_{REG2} = 100mA	50			dB
5V/350mA REG 3 OUTPUT						
V_{REG3}	Voltage Offset from VREF			10	40	mV
ΔV_{line}	Line Regulation	7V ≤ V_{BAT} ≤ 26V (Measure Δ V_{REG3} Across V_{BAT} Range)			40	mV
ΔV_{load}	Load Regulation	5mA ≤ I_{REG3} ≤ 350mA			100	mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{DROPOUT}$	Dropout Voltage (Measure VBAT- V_{REG3} when V_{REG3} drops 0.1V)	(Measure VBAT- V_{REG3} when V_{REG3} drops 0.1V) I_{REG3} = 175mA I_{REG3} = 5mA			 950 600	 mV mV
I_{lim3}	Current Limit		0.5		1	A
SVR	Ripple Rejection	f_o = 1kHz, V_{BAT} = 14V with 1Vpp AC I_{REG3} = 175mA	50			dB
8/10V/1A REG 4 OUTPUT						
V_{REG4}	Output Voltage	I_{REG4} = 1A b5 = 0 b5 = 1	 7.6 9.50	 8 10	 8.4 10.5	 V V
ΔV_{line}	Line Regulation	11V ≤ V_{BAT} ≤ 26V, b5 = 1 (Measure Δ V_{REG2} Across V_{BAT} Range)			50	mV
ΔV_{load}	Load Regulation	5mA ≤ I_{REG4} ≤ 1A			150	mV
$V_{DROPOUT}$	Dropout Voltage	(Measure VBAT- V_{REG2} when V_{REG2} drops 0.1V) I_{REG4} = 1A I_{REG4} = 5mA			 950 600	 mV mV
I_{lim4}	Current Limit		1.3		2.4	A
SVR	Ripple Rejection	f_o = 1kHz, V_{BAT} = 14V with 1Vpp AC I_{REG4} = 500mA	50			dB
5V/250mA REG 5 OUTPUT						
V_{REG5}	Output Voltage	I_{REG5} = 250mA	4.75	5	5.25	V
ΔV_{line}	Line Regulation	7V ≤ V_{BAT} ≤ 26V (Measure Δ V_{REG5} Across V_{BAT} Range)			40	mV
ΔV_{load}	Load Regulation	5mA ≤ I_{REG5} ≤250mA			100	mV
$V_{DROPOUT}$	Dropout Voltage	(Measure VBAT- V_{REG5} when V_{REG5} drops 0.1V) I_{REG5} = 250A I_{REG5} = 5mA			 1.6 1.2	 V V
I_{lim5}	Current Limit		320		700	mA
SVR	Ripple Rejection	f_o = 1kHz, V_{BAT} = 14V with 1Vpp AC I_{REG5} = 125mA	50			dB
2A HSD1						
V_{sat}	Output Saturation Voltage	IHSD1 = 1A Continuous Time Operation			0.5	V
I_{leak1}	Output Leakage Current	All Driver Outputs are Off	-50		50	µA
I_{lim}	Current Limiting	R_{HSD1} = 0.5Ω	2.4		4	A
0.45A HSD2 & HSD3						
V_{sat}	Output Saturation Voltage	IHSD2,3 = 300mA Continuous Time Operation			0.6	V
$I_{leak2,3}$	Output Leakage Current	All Driver Outputs are Off	-50		50	µA
I_{lim}	Current Limiting	$R_{HSD2,3}$ = 0.5Ω	0.56		1	A

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CHARACTERISTICS FOR I^2C						
V_{IL}	LOW Level Input Voltage				1.5	V
V_{IH}	HIGH Level Input Voltage		3			V
V_{HYS}	Input Hysteresis		0.2			V
V_{OL1}	LOW Level Output	Sink Current = 3mA			0.4	V
V_{OL2}		Sink Current = 6mA			0.6	V
I_I	Input Current	$0.4V \le V_I \le 0.9V_{DDmax}$	-10		10	µA
f_{SCL}	SCL Clock Frequency				400	kHz

FUNCTIONAL DESCRIPTION

The three high side drivers are a 2.0A output (HSD1), and two 450mA outputs (HSD2 & 3). The five regulator outputs are a 10V at 350mA (REG1), an 8.5V at 175mA (REG2), a 5V at 350mA (REG3), an 8V/10V at 1A (REG4), and 5V at 250mA (REG5). The regulators are low drop-out. The regulators will operate with output capacitors with ESR of 0.1Ω to 5Ω.

The 8.5V regulator output (REG2) is a tighter tolerance output than the other regulator outputs. The 8.5V output is a ±2.5% (5% total range) output over temperature. This is required on the regulator to improve performance and reduce cost on the 8.5V driven IC's in the radio. The tighter tolerance is possible by performing a trim of the bandgap reference to the 8.5V output. The other outputs are ±5% variation over temperature.

REG3 is referenced from the VREF input not the internal bandgap. This is done to minimize the voltage offset between individual 5V supplies.

The REG2 and REG3 outputs are turned on and off with the Enable input, a '1' turns the outputs on and a '0' turns them off. When Enable is "1", the other outputs can be independently controlled via the I^2C bus. When a given regulator is turned off it must be guaranteed to be lower than 0.2V. The output voltage of REG4 is selected via bit 5 of the I^2C data byte: 8V is the output voltage if bit5 = '0' while 10V is the output voltage when bit5 = '1'. When all outputs are turned off the total current draw must be minimized. I^2C will run at a clock speed range of 100kHz to 400kHz. This device should be capable of operating at any frequency within this range.

Protection

The L5950 can survive under the following conditions: shorting the outputs to BAT and GND, loss of BAT, loss of IC GND, double battery(+26.5V), 4000V ESD, 34V load dump. L5950 will not handle a reverse battery condition. External components must be implemented for reverse battery protection.

Thermal Shutdown: REG1, REG2, REG3, REG4, REG5 outputs shutdown at 160°C and return to normal operation at 130°C. The HSD2 and HSD3 shutdown at 160°C and return to normal operation at 130°C. The HSD1 with go into thermal shutdown at 170°C and returns to operation at 120°C.

Current Limiting: each voltage regulator will contain its own current protection.

Short Circuit: If the outputs are short circuited, the IC will go into current limiting and eventually the thermal shutdown will kick in. Current limiting will not disable the outputs.

Overvoltage: The IC will not operate if the BAT voltage reaches 27V typ. or above.

Figure 1. Definition of Timing on the I^2C Bus.

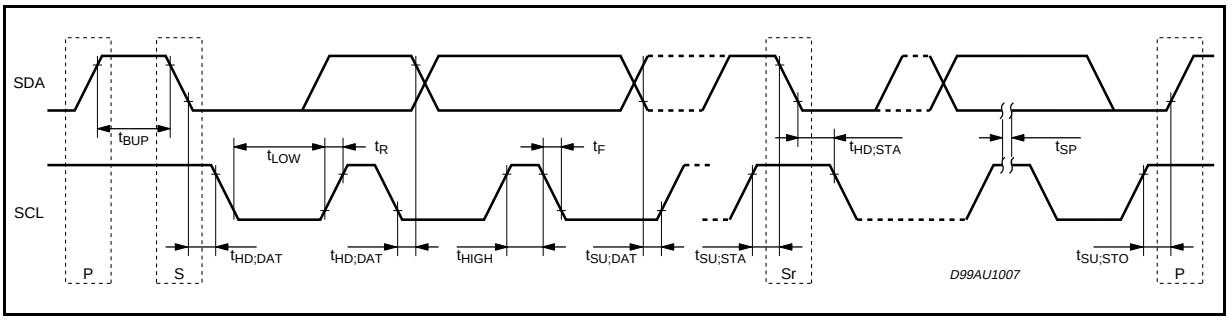
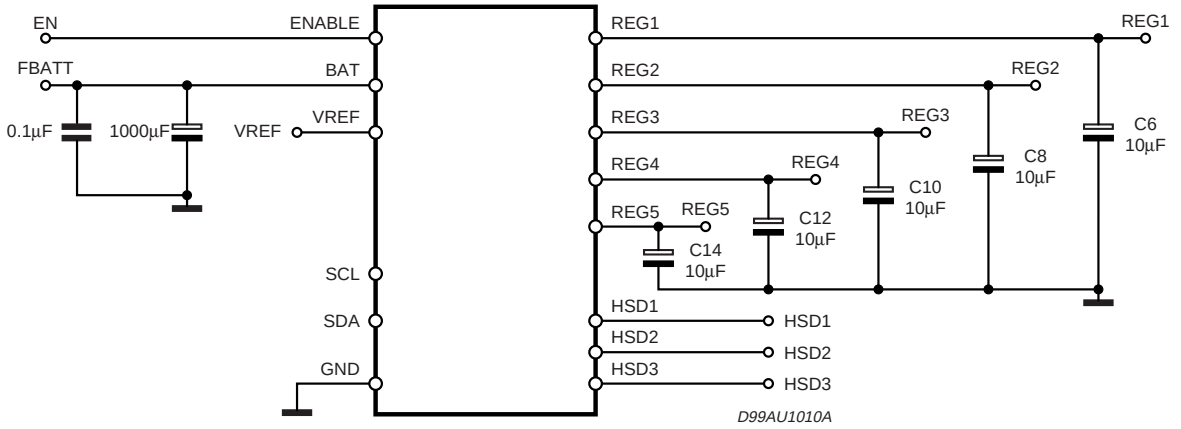


Figure 2. Typical Application Circuit.



(*) ESR of output capacitors should be between 0.1Ω and 5.0Ω.

WRITE MODE:

	CHIP ADDRESS										DATA BYTE										
S								0	A									A	..	..	P
	MSB							LSB		MSB							LSB				

S = START condition - SDA goes from high to low while SCL is high

A = Acknowledge - the device being written to, pulls down on data line (SDA) during the acknowledge clock pulse.

P = STOP condition - SDA goes from low to high while SCL is high.

CHIP ADDRESS BYTE:

CHIP ADDRESS							READ/WRITE
A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	1	0	0	0	0

DATA BYTE:

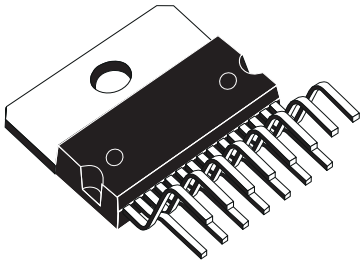
DATA BYTE							
REG1		R4 10V	REG4	REG5	HSD1	HSD2	HSD3
b7	b6	b5	b4	b3	b2	b1	b0
	X						

Default mode is 0000 0000 which corresponds to all outputs being off, low power mode.

Bit 5 Controls the output voltage of REG4. A '0' corresponds to 8V and a '1' corresponds to 10V.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt15 V