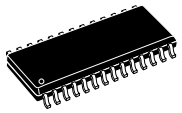
L6917B

5 BIT PROGRAMMABLE DUAL-PHASE CONTROLLER

- 2 PHASE OPERATION WITH SYNCRHONOUS RECTIFIER CONTROL
- ULTRA FAST LOAD TRANSIENT RESPONSE
- INTEGRATED HIGH CURRENT GATE DRIVERS: UP TO 2A GATE CURRENT
- TTL-COMPATIBLE 5 BIT PROGRAMMABLE OUTPUT COMPLIANT WITH VRM 9.0
- 0.8% INTERNAL REFERENCE ACCURACY
- 10% ACTIVE CURRENT SHARING ACCURACY
- DIGITAL 2048 STEP SOFT-START
- OVERVOLTAGE PROTECTION
- OVERCURRENT PROTECTION REALIZED USING THE LOWER MOSFET'S R_{dsON} OR A SENSE RESISTOR
- 300 kHz INTERNAL OSCILLATOR
- OSCILLATOR EXTERNALLY ADJUSTABLE UP TO 600kHz
- POWER GOOD OUTPUT AND INHIBIT FUNCTION
- REMOTE SENSE BUFFER
- PACKAGE: SO-28

APPLICATIONS

- POWER SUPPLY FOR SERVERS AND WORKSTATIONS
- POWER SUPPLY FOR HIGH CURRENT MICROPROCESSORS
- DISTRIBUTED DC-DC CONVERTERS



SO-28

ORDERING NUMBERS:L6917BD

L6917BDTR (Tape & Reel)

DESCRIPTION

The device is a power supply controller specifically designed to provide a high performance DC/DC conversion for high current microprocessors.

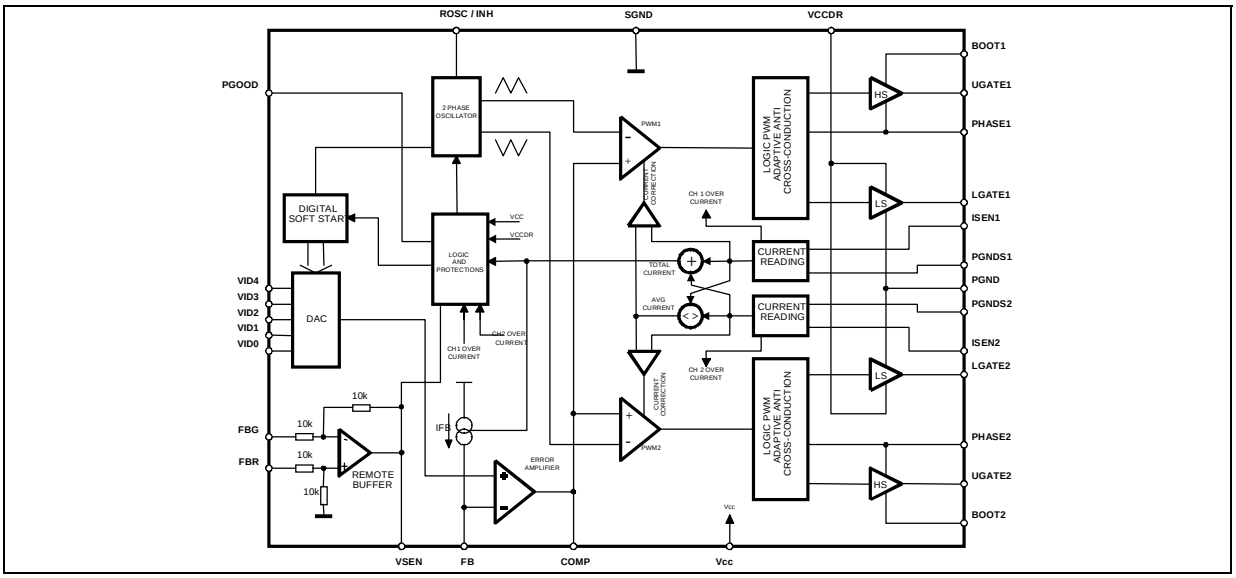
The device implements a dual-phase step-down controller with a 180° phase-shift between each phase.

A precise 5-bit digital to analog converter (DAC) allows adjusting the output voltage from 1.100V to 1.850V with 25mV binary steps.

The high precision internal reference assures the selected output voltage to be within ±0.8%. The high peak current gate drive affords to have fast switching to the external power mos providing low switching losses.

The device assures a fast protection against load over current and load over/under voltage. An internal crowbar is provided turning on the low side mosfet if an over-voltage is detected. In case of over-current, the system works in Constant Current mode.

BLOCK DIAGRAM



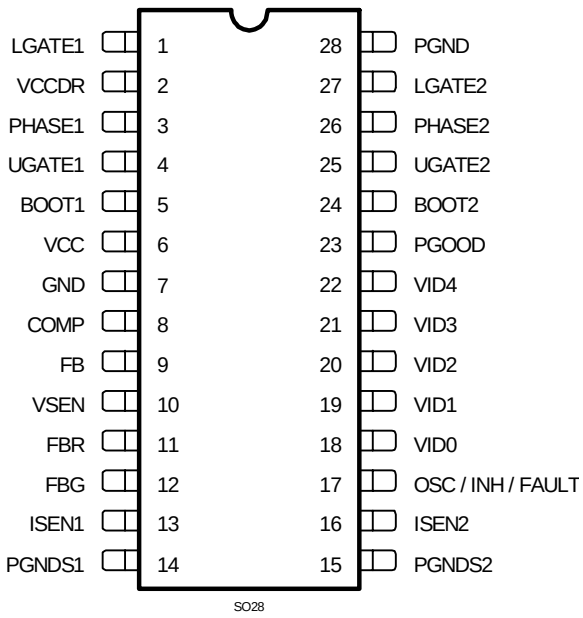
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc, V_{CCDR}	to PGND	15	V
V_{BOOT}-V_{PHASE}	Boot Voltage	15	V
V_{UGATE1}-V_{PHASE1} V_{UGATE2}-V_{PHASE2}		15	V
	LGATE1, PHASE1, LGATE2, PHASE2 to PGND	-0.3 to Vcc+0.3	V
	All other pins to PGND	-0.3 to 7	V
V_{phase}	Sustainable Peak Voltage t < 20ns @ 600kHz	26	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	60	°C/W
T_{max}	Maximum junction temperature	150	°C
$T_{storage}$	Storage temperature range	-40 to 150	°C
T_j	Junction Temperature Range	-25 to 125	°C
P_{MAX}	Max power dissipation at T_{amb} = 25°C	2	W

PIN CONNECTION



SO28

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V ±10%, T_J = 0 to 70°C unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vcc SUPPLY CURRENT						
I_{CC}	Vcc supply current	HGATEx and LGATEx open V_{CCDR}=V_{BOOT}=12V	7.5	10	12.5	mA
I_{CCDR}	V_{CCDR} supply current	LGATEx open; V_{CCDR}=12V	2	3	4	mA
I_{BOOTx}	Boot supply current	HGATEx open; PHASEx to PGND V_{CC}=V_{BOOT}=12V	0.5	1	1.5	mA
POWER-ON						
	Turn-On V_{CC} threshold	V_{CC} Rising; V_{CCDR}=5V	7.8	9	10.2	V
	Turn-Off V_{CC} threshold	V_{CC} Falling; V_{CCDR}=5V	6.5	7.5	8.5	V
	Turn-On V_{CCDR} Threshold	V_{CCDR} Rising V_{CC}=12V	4.2	4.4	4.6	V
	Turn-Off V_{CCDR} Threshold	V_{CCDR} Falling V_{CC}=12V	4.0	4.2	4.4	V
OSCILLATOR/INHIBIT/FAULT						
f_{OSC}	Initial Accuracy	OSC = OPEN OSC = OPEN; Tj=0°C to 125°C	278 270	300	322 330	kHz kHz
$f_{OSC,Rosc}$	Total Accuracy	R_T to GND=74kΩ	450	500	550	kHz
INH	Inhibit threshold	I_{SINK}=5mA	0.8	0.85	0.9	V
d_{MAX}	Maximum duty cycle	OSC = OPEN	70	75		%
ΔVosc	Ramp Amplitude		1.8	2	2.2	V
FAULT	Voltage at pin OSC	OVP or UVP Active	4.75	5.0	5.25	V
REFERENCE AND DAC						
	Output Voltage Accuracy	VID0, VID1, VID2, VID3, VID4 see Table1; FBR = V_{OUT}; FBG = GND	-0.8	-	0.8	%
I_{DAC}	VID pull-up Current	VIDx = GND	4	5	6	µA
	VID pull-up Voltage	VIDx = OPEN	3.1	-	3.4	V
ERROR AMPLIFIER						
	DC Gain			80		dB
SR	Slew-Rate	COMP=10pF		15		V/µs
DIFFERENTIAL AMPLIFIER (REMOTE BUFFER)						
	DC Gain			1		V/V
CMRR	Common Mode Rejection Ratio			40		dB

ELECTRICAL CHARACTERISTICS (continued)
V_{CC} = 12V ±10%, T_J = 0 to 70°C unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Input Offset	FBR=1.100V to1.850V; FBG=GND	-12		12	mV
SR	Slew Rate	VSEN=10pF		15		V/µs
DIFFERENTIAL CURRENT SENSING						
I_{ISEN1}, I_{ISEN2}	Bias Current	Iload=0	45	50	55	µA
I_{PGNDSx}	Bias Current		45	50	55	µA
I_{ISEN1}, I_{ISEN2}	Bias Current at Over Current Threshold		80	85	90	µA
I_{FB}	Active Droop Current	Iload<0% Iload=100%	 47.5	0 50	1 52.5	µA µA
GATE DRIVERS						
$t_{RISE\ HGATE}$	High Side Rise Time	V_{BOOTx}-V_{PHASEx}=10V; C_{HGATEx} to PHASEx=3.3nF		15	30	ns
I_{HGATEx}	High Side Source Current	V_{BOOTx}-V_{PHASEx}=10V		2		A
R_{HGATEx}	High Side Sink Resistance	V_{BOOTx}-V_{PHASEx}=12V;	1.5	2	2.5	Ω
$t_{RISE\ LGATE}$	Low Side Rise Time	V_{CCDR}=10V; C_{LGATEx} to PGNDx=5.6nF		30	55	ns
I_{LGATEx}	Low Side Source Current	V_{CCDR}=10V		1.8		A
R_{LGATEx}	Low Side Sink Resistance	V_{CCDR}=12V	0.7	1.1	1.5	Ω
P GOOD and OVP/UVP PROTECTIONS						
PGOOD	Upper Threshold (V_{SEN}/DACOUT)	V_{SEN} Rising	108	112	116	%
PGOOD	Lower Threshold (V_{SEN}/DACOUT)	V_{SEN} Falling	84	88	92	%
OVP	Over Voltage Threshold (V_{SEN})	V_{SEN} Rising	2.0		2.25	V
UVP	Under Voltage Trip (V_{SEN}/DACOUT)	V_{SEN} Falling	56	60	64	%
V_{PGOOD}	PGOOD Voltage Low	I_{PGOOD} = -4mA	0.3	0.4	0.5	V

Table 1. VID Settings

VID4	VID3	VID2	VID1	VID0	Output Voltage (V)
1	1	1	1	1	OUTPUT OFF
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

PIN FUNCTION

N	Name	Description
1	LGATE1	Channel 1 low side gate driver output.
2	VCCDR	Mosfet driver supply. It can be varied from 5V to 12V.
3	PHASE1	This pin is connected to the source of the upper mosfet and provides the return path for the high side driver of channel 1.
4	UGATE1	Channel 1 high side gate driver output.
5	BOOT1	Channel 1 bootstrap capacitor pin. Through this pin is supplied the high side driver and the upper mosfet. Connect through a capacitor to the PHASE1 pin and through a diode to Vcc (cathode vs. boot).
6	VCC	Device supply voltage. The operative supply voltage is 12V.
7	GND	All the internal references are referred to this pin. Connect it to the PCB signal ground.
8	COMP	This pin is connected to the error amplifier output and is used to compensate the control feedback loop.
9	FB	This pin is connected to the error amplifier inverting input and is used to compensate the voltage control feedback loop. A current proportional to the sum of the current sensed in both channel is sourced from this pin (50µA at full load, 70µA at the Over Current threshold). Connecting a resistor between this pin and VSEN pin allows programming the droop effect.
10	VSEN	Connected to the output voltage it is able to manage Over & Under-voltage conditions and the PGOOD signal. It is internally connected with the output of the Remote Sense Buffer for Remote Sense of the regulated voltage. If no Remote Sense is implemented, connect it directly to the regulated voltage in order to manage OVP, UVP and PGOOD.
11	FBR	Remote sense buffer non-inverting input. It has to be connected to the positive side of the load to perform a remote sense. If no remote sense is implemented, connect directly to the output voltage (in this case connect also the VSEN pin directly to the output regulated voltage).
12	FBG	Remote sense buffer inverting input. It has to be connected to the negative side of the load to perform a remote sense. Pull-down to ground if no remote sense is implemented.
13	ISEN1	Channel 1 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet Rds_{ON}. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the positive current limit at 140% as follow: $$I_{MAX} = \frac{35\mu A \cdot R_g}{R_{sense}}$$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS1 net in order to couple in common mode any picked-up noise.
14	PGNDS1	Channel 1 Power Ground sense pin. The net connecting the pin to the sense point (*) must be routed as close as possible to the ISEN1 net in order to couple in common mode any picked-up noise.
15	PGNDS2	Channel 2 Power Ground sense pin. The net connecting the pin to the sense point (*) must be routed as close as possible to the ISEN2 net in order to couple in common mode any picked-up noise.

(*) Through a resistor Rg.

PIN FUNCTION (continued)

N	Name	Description
16	ISEN2	Channel 2 current sense pin. The output current may be sensed across a sense resistor or across the low-side mosfet Rds_{ON}. This pin has to be connected to the low-side mosfet drain or to the sense resistor through a resistor Rg in order to program the positive current limit at 140% as follow: $$I_{MAX} = \frac{35\mu A \cdot R_g}{R_{sense}}$$ Where 35µA is the current offset information relative to the Over Current condition (offset at OC threshold minus offset at zero load). The net connecting the pin to the sense point must be routed as close as possible to the PGNDS2 net in order to couple in common mode any picked-up noise.
17	OSC/ INH/ FAULT	Oscillator switching frequency pin. Connecting an external resistor from this pin to GND, the external frequency is increased according to the equation: $$f_S = 300KHz + \frac{14.82 \cdot 10^6}{R_{OSC(K\Omega)}}$$ Connecting a resistor from this pin to Vcc (12V), the switching frequency is reduced according to the equation: $$f_S = 300KHz - \frac{12.91 \cdot 10^7}{R_{OSC(K\Omega)}}$$ If the pin is not connected, the switching frequency is 300KHz. Forcing the pin to a voltage lower than 0.8V, the device stop operation and enter the inhibit state. The pin is forced high when an over or under voltage is detected. This condition is latched; to recover it is necessary turn off and on VCC.
18-22	VID4-0	Voltage IDentification pins. These input are internally pulled-up and TTL compatible. They are used to program the output voltage as specified in Table 1 and to set the power good thresholds. Connect to GND to program a ‘0’ while leave floating to program a ‘1’.
23	PGOOD	This pin is an open collector output and is pulled low if the output voltage is not within the above specified thresholds. If not used may be left floating.
24	BOOT2	Channel 2 bootstrap capacitor pin. Through this pin is supplied the high side driver and the upper mosfet. Connect through a capacitor to the PHASE2 pin and through a diode to Vcc (cathode vs. boot).
25	UGATE2	Channel 2 high side gate driver output.
26	PHASE2	This pin is connected to the source of the upper mosfet and provides the return path for the high side driver of channel 2.
27	LGATE2	Channel 2 low side gate driver output.
28	PGND	Power ground pin. This pin is common to both sections and it must be connected through the closest path to the low side mosfets source pins in order to reduce the noise injection into the device.

Device Description

The device is an integrated circuit realized in BCD technology. It provides complete control logic and protections for a high performance dual-phase step-down DC-DC converter optimized for microprocessor power supply. It is designed to drive N Channel MOSFETs in a dual-phase synchronous-rectified buck topology. A 180 deg phase shift is provided between the two phases allowing reduction in the input capacitor current ripple, reducing also the size and the losses. The output voltage of the converter can be precisely regulated, programming the VID pins, from 1.100V to 1.850V with 25mV binary steps, with a maximum tolerance of ±0.8% over temperature and line voltage variations. The device provides an average current-mode control with fast transient response. It includes a 300kHz free-running oscillator adjustable up to 600kHz. The error amplifier features a 15V/µs slew rate that permits high converter bandwidth for fast transient performances. Current information is read across the lower mosfets r_{DSON} or across a sense resistor in fully differential mode. The current information corrects the PWM output in order to equalize the average current carried by each phase. Current sharing between the two phases is then limited at ±10% over static and dynamic conditions. The device protects against over-current, with an OC threshold for each phase, entering in constant current mode. Since the current is read across the low side mosfets, the constant current keeps constant the bottom of the inductors current triangular waveform. When an under voltage is detected the device latches and the FAULT pin is driven high. The device performs also over voltage protection that disable immediately the device turning ON the lower driver and driving high the FAULT pin.

Oscillator

The device has been designed in order to operate an each phase at the same switching frequency of the internal oscillator. So, input and output resulting frequency is doubled.

The switching frequency is internally fixed to 300kHz. The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The current delivered to the oscillator is typically 25µA and may be varied using an external resistor (R_{OSC}) connected between OSC pin and GND or Vcc. Since the OSC pin is maintained at fixed voltage (typ). 1.235V, the frequency is varied proportionally to the current sunk (forced) from (into) the pin considering the internal gain of 12KHz/µA.

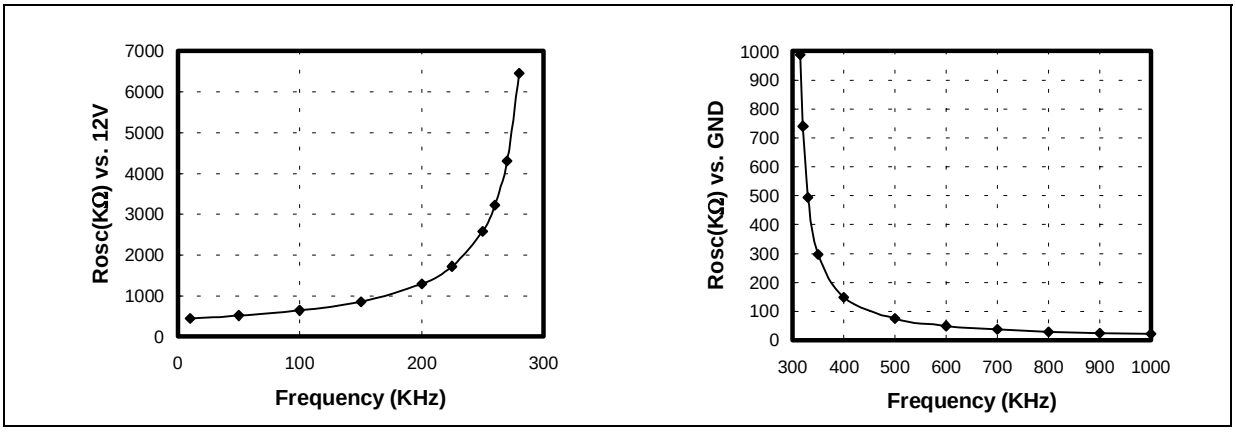
In particular connecting it to GND the frequency is increased (current is sunk from the pin), while connecting ROSC to Vcc=12V the frequency is reduced (current is forced into the pin), according to the following relationships:

$$R_{OSC}\text{vs. GND: } f_S = 300kHz + \frac{1.237}{R_{OSC}(K\Omega)} \cdot 12\frac{kHz}{\mu A} = 300kHz + \frac{14.82 \cdot 10^6}{R_{OSC}(K\Omega)}$$

$$R_{OSC}\text{vs. 12V: } f_S = 300kHz - \frac{12 - 1.237}{R_{OSC}(K\Omega)} \cdot 12\frac{kHz}{\mu A} = 300kHz - \frac{12.918 \cdot 10^7}{R_{OSC}(K\Omega)}$$

Note that forcing a 25µA current into this pin, the device stops switching because no current is delivered to the oscillator.

Figure 1. R_{OSC} vs. Switching Frequency



Digital to Analog Converter

The built-in digital to analog converter allows the adjustment of the output voltage from 1.100V to 1.850V with 25mV as shown in the previous table 1. The internal reference is trimmed to ensure the precision of 0.8% and a zero temperature coefficient around 70°C. The internal reference voltage for the regulation is programmed by the voltage identification (VID) pins. These are TTL compatible inputs of an internal DAC that is realized by means of a series of resistors providing a partition of the internal voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the VPROG voltage reference (i.e. the set-point of the error amplifier). Internal pull-ups are provided (realized with a 5µA current generator up to 3.3V max); in this way, to program a logic "1" it is enough to leave the pin floating, while to program a logic "0" it is enough to short the pin to GND. VID code “11111” programs the NOCPU state: all mosfets are turned OFF and the condition is latched.

The voltage identification (VID) pin configuration also sets the power-good thresholds (PGOOD) and the overvoltage protection (OVP) thresholds.

Soft Start and INHIBIT

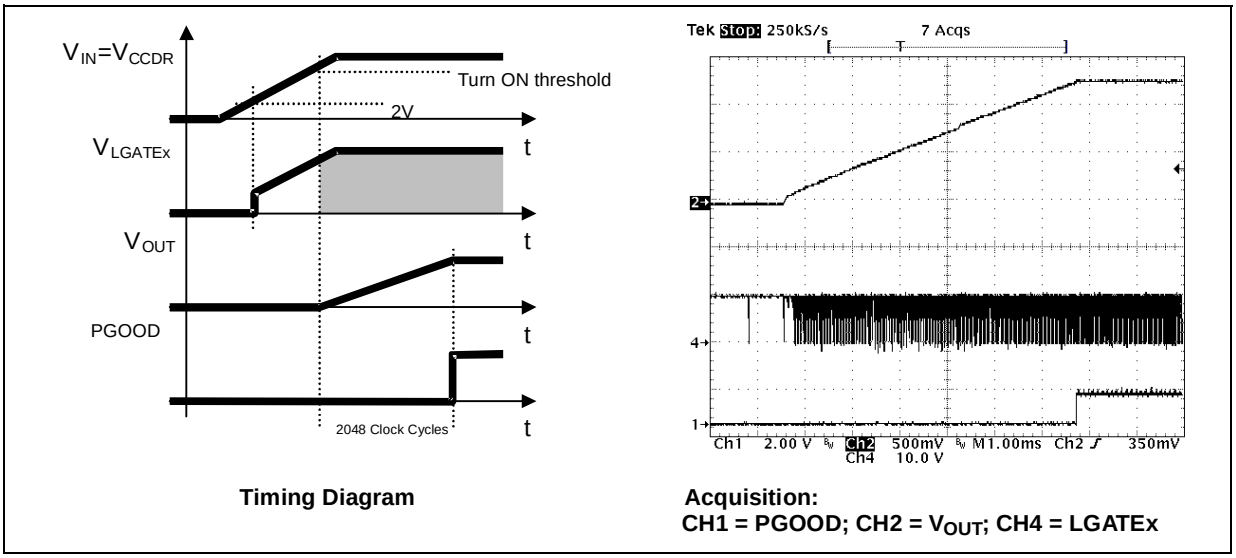
At start-up a ramp is generated increasing the loop reference from 0V to the final value programmed by VID in 2048 clock periods as shown in figure 2.

Before soft start, the lower power MOS are turned ON after that V_{CCDR} reaches 2V (independently by Vcc value) to discharge the output capacitor and to protect the load from high side mosfet failures. Once soft start begins, the reference is increased; when it reaches the bottom of the oscillator triangular waveform (1V typ) also the upper MOS begins to switch and the output voltage starts to increase with closed loop regulation.. At the end of the digital soft start, the Power Good comparator is enabled and the PGOOD signal is then driven high (See fig. 2). The Under Voltage comparator enabled when the reference voltage reaches 0.8V.

The Soft-Start will not take place, if both V_{CC} and VCCDR pins are not above their own turn-on thresholds. During normal operation, if any under-voltage is detected on one of the two supplies the device shuts down.

Forcing the OSC/INH/FAULT pin to a voltage lower than 0.8V the device enter in INHIBIT mode: all the power mosfets are turned off until this condition is removed. When this pin is freed, the OSC/INH/FAULT pin reaches the band-gap voltage and the soft start begins.

Figure 2. Soft Start



Timing Diagram

Acquisition:
CH1 = PGOOD; CH2 = V_{OUT}; CH4 = LGATEx

Driver Section

The integrated high-current drivers allow using different types of power MOS (also multiple MOS to reduce the RDSON), maintaining fast switching transition.

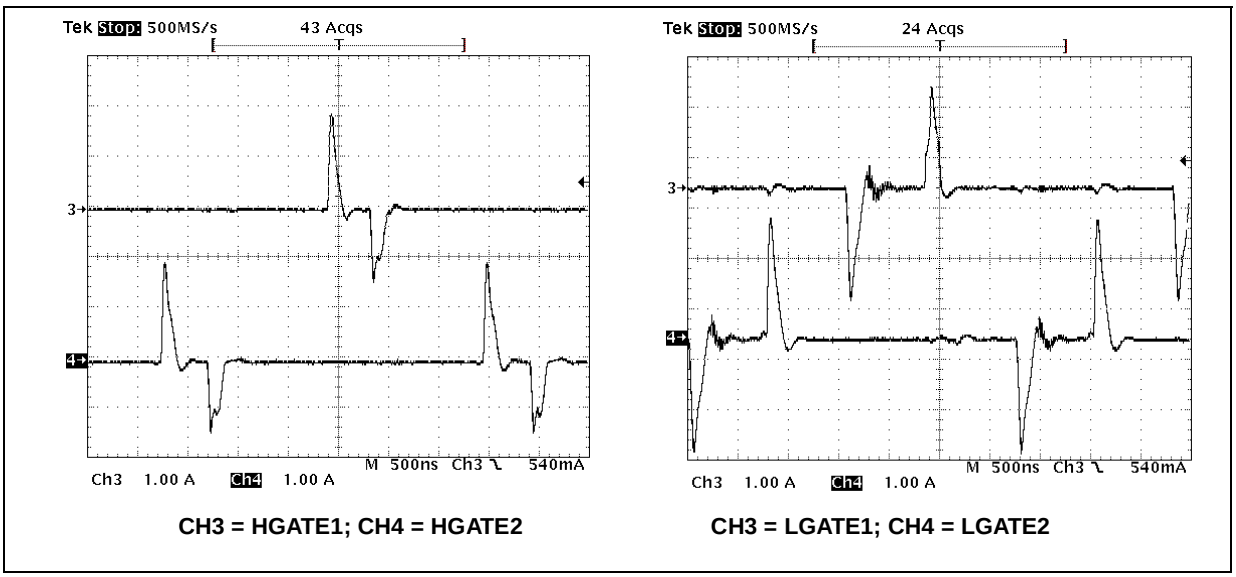
The drivers for the high-side mosfets use BOOTx pins for supply and PHASEx pins for return. The drivers for the low-side mosfets use VCCDRV pin for supply and PGND pin for return. A minimum voltage of 4.6V at VCCDRV pin is required to start operations of the device.

The controller embodies a sophisticated anti-shoot-through system to minimize low side body diode conduction time maintaining good efficiency saving the use of Schottky diodes. The dead time is reduced to few nanoseconds assuring that high-side and low-side mosfets are never switched on simultaneously: when the high-side mosfet turns off, the voltage on its source begins to fall; when the voltage reaches 2V, the low-side mosfet gate drive is applied with 30ns delay. When the low-side mosfet turns off, the voltage at LGATEx pin is sensed. When it drops below 1V, the high-side mosfet gate drive is applied with a delay of 30ns. If the current flowing in the inductor is negative, the source of high-side mosfet will never drop. To allow the turning on of the low-side mosfet even in this case, a watchdog controller is enabled: if the source of the high-side mosfet don't drop for more than 240ns, the low side mosfet is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

The BOOTx and VCCDR pins are separated from IC's power supply (VCC pin) as well as signal ground (SGND pin) and power ground (PGND pin) in order to maximize the switching noise immunity. The separated supply for the different drivers gives high flexibility in mosfet choice, allowing the use of logic-level mosfet. Several combination of supply can be chosen to optimize performance and efficiency of the application. Power conversion is also flexible, 5V or 12V bus can be chosen freely.

The peak current is shown for both the upper and the lower driver of the two phases in figure 3. A 10nF capacitive load has been used. For the upper drivers, the source current is 1.9A while the sink current is 1.5A with V_{BOOT}-V_{PHASE} = 12V; similarly, for the lower drivers, the source current is 2.4A while the sink current is 2A with VCCDR = 12V.

Figure 3. Drivers peak current: High Side (left) and Low Side (right)



CH3 = HGATE1; CH4 = HGATE2

CH3 = LGATE1; CH4 = LGATE2

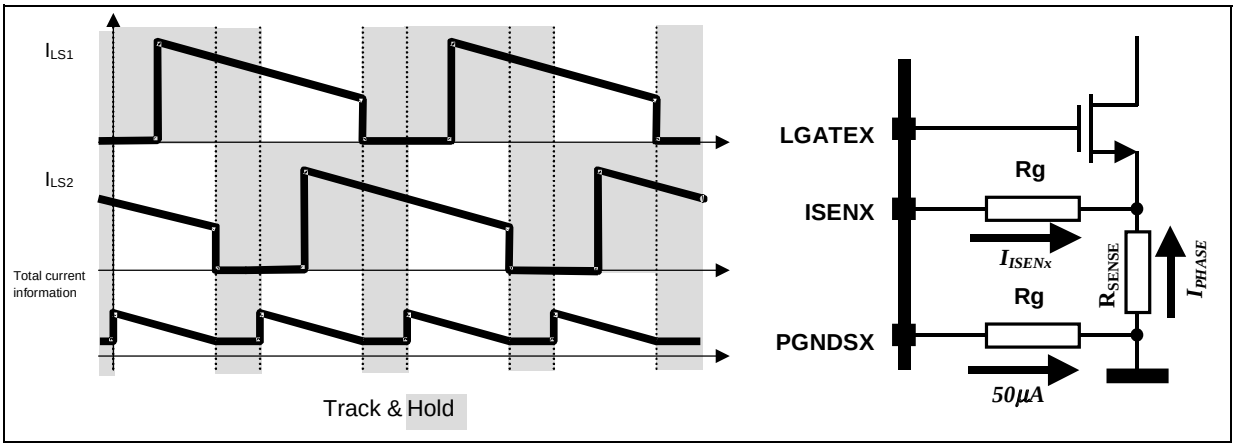
Current Reading and Over Current

The current flowing trough each phase is read using the voltage drop across the low side mosfets r_{DSON} or across a sense resistor (R_{SENSE}) and internally converted into a current. The transconductance ratio is issued by the external resistor Rg placed outside the chip between ISENx and PGNDSx pins toward the reading points. The full differential current reading rejects noise and allows to place sensing element in different locations without affecting the measurement's accuracy. The current reading circuitry reads the current during the time in

which the low-side mosfet is on (OFF Time). During this time, the reaction keeps the pin ISENx and PGNDSx at the same voltage while during the time in which the reading circuitry is off, an internal clamp keeps these two pins at the same voltage sinking from the ISENx pin the necessary current.

The proprietary current reading circuit allows a very precise and high bandwidth reading for both positive and negative current. This circuit reproduces the current flowing through the sensing element using a high speed Track & Hold transconductance amplifier. In particular, it reads the current during the second half of the OFF time reducing noise injection into the device due to the mosfet turn-on (See fig. 4). Track time must be at least 200ns to make proper reading of the delivered current.

Figure 4. Current Reading Timing (Left) and Circuit (Right)



This circuit sources a constant 50µA current from the PGNDSx pin and keeps the pins ISENx and PGNDSx at the same voltage. Referring to figure 4, the current that flows in the ISENx pin is then given by the following equation:

$$I_{ISENx} = 50\mu A + \frac{R_{SENSE} \cdot I_{PHASE}}{R_g} = 50\mu A + I_{INFOx}$$

Where R_{SENSE} is an external sense resistor or the rds,on of the low side mosfet and Rg is the transconductance resistor used between ISENx and PGNDSx pins toward the reading points; I_{PHASE} is the current carried by each phase and, in particular, the current measured in the middle of the oscillator period

The current information reproduced internally is represented by the second term of the previous equation as follow:

$$I_{INFOx} = \frac{R_{SENSE} \cdot I_{PHASE}}{R_g}$$

Since the current is read in differential mode, also negative current information is kept; this allow the device to check for dangerous returning current between the two phases assuring the complete equalization between the phase's currents.

From the current information of each phase, information about the total current delivered ($I_{FB} = I_{INFO1} + I_{INFO2}$) and the average current for each phase ($I_{AVG} = (I_{INFO1} + I_{INFO2})/2$) is taken. I_{INFOX} is then compared to I_{AVG} to give the correction to the PWM output in order to equalize the current carried by the two phases.

The transconductance resistor Rg has to be designed in order to have current information of 25µA per phase at full nominal load; the over current intervention threshold is set at 140% of the nominal (IINFOx = 35µA).

According to the above relationship, the limiting current (I_{LIM}) for each phase, which has to be placed at one half of the total delivered maximum current, results:

$$I_{LIM} = \frac{35\mu A \cdot Rg}{R_{SENSE}} \qquad Rg = \frac{I_{LIM} \cdot R_{SENSE}}{35\mu A}$$

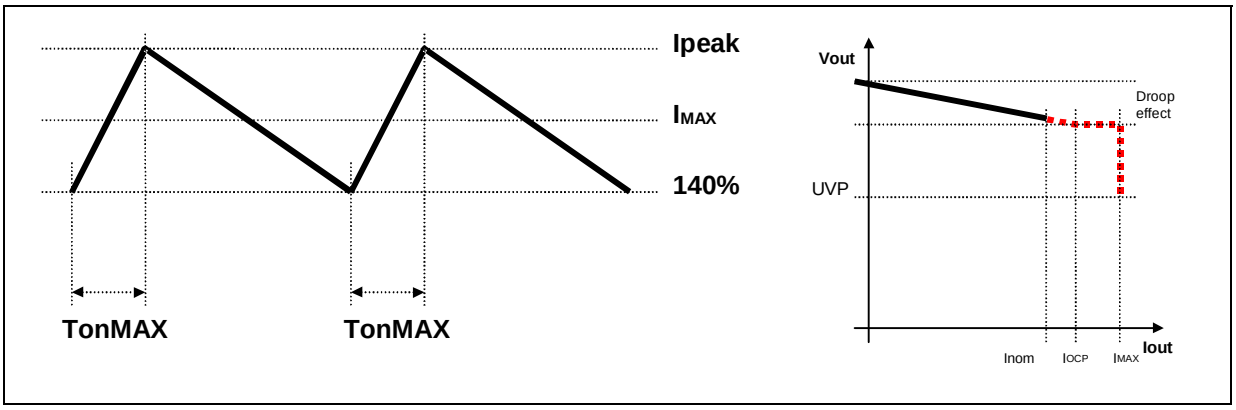
An over current is detected when the current flowing into the sense element is greater than 140% of the nominal

current (I_{INFOx}>35µA): the device enters in Quasi-Constant-Current operation. The low-side mosfets stays ON until I_{INFO} becomes lower than 35µA skipping clock cycles. The high side mosfets can be turned ON with a T_{ON} imposed by the control loop at the next available clock cycle and the device works in the usual way until another OCP event is detected.

The device limits the bottom of the inductor current triangular waveform. So the average current delivered can slightly increase also in Over Current condition since the current ripple increases. In fact, the ON time increases due to the OFF time rise because of the current has to reach the 140% bottom. The worst-case condition is when the duty cycle reaches its maximum value (d=75% internally limited). When this happens, the device works in Constant Current and the output voltage decrease as the load increase. Crossing the UVP threshold causes the device to latch (FAULT pin is driven high).

Figure 5 shows this working condition

Figure 5. Constant Current operation



It can be observed that the peak current (Ipeak) is greater than the 140% but it can be determined as follow:

$$Ipeak = 1.4 \cdot I_{NOM} + \frac{V_{IN} - Vout_{MIN}}{L} \cdot Ton_{MAX}$$

Where I_{NOM} is the nominal current and $Vout_{MIN}$ is the minimum output voltage (VID-40% as explained below).

The device works in Constant-Current, and the output voltage decreases as the load increase, until the output voltage reaches the under-voltage threshold ($Vout_{MIN}$). When this threshold is crossed, all mosfets are turned off, the FAULT pin is driven high and the device stops working. Cycle the power supply to restart operation.

The maximum average current during the Constant-Current behavior results:

$$I_{MAX} = 1.4 \cdot I_{NOM} + 2 \cdot \frac{Ipeak - 1.4 \cdot I_{NOM}}{2}$$

In this particular situation, the switching frequency results reduced. The ON time is the maximum allowed (Ton-MAX) while the OFF time depends on the application:

$$T_{OFF} = L \cdot \frac{Ipeak - 1.4 \cdot I_{NOM}}{Vout} \qquad f = \frac{1}{Ton_{MAX} + T_{OFF}}$$

Over current is set anyway when I_{INFOx} reaches 35µA. The full load value is only a convention to work with convenient values for I_{FB}. Since the OCP intervention threshold is fixed, to modify the percentage with respect to the load value, it can be simply considered that, for example, to have on OCP threshold of 170%, this will correspond to I_{INFOx} = 35µA (I_{FB} = 70µA). The full load current will then correspond to I_{INFOx} = 20.5µA (I_{FB} = 41µA).

Integrated Droop Function

The device uses a droop function to satisfy the requirements of high performance microprocessors, reducing the size and the cost of the output capacitor.

This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current

As shown in figure 6, the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimized. In practice the droop function introduces a static error (Vdroop in figure 6) proportional to the output current. Since the device has an average current mode regulation, the information about the total current delivered is used to implement the Droop Function. This current (equal to the sum of both I_{INFOx}) is sourced from the FB pin. Connecting a resistor between this pin and Vout, the total current information flows only in this resistor because the compensation network between FB and COMP has always a capacitor in series (See fig. 7). The voltage regulated is then equal to:

$$V_{OUT} = V_{ID} - R_{FB} \cdot I_{FB}$$

Since I_{FB} depends on the current information about the two phases, the output characteristic vs. load current is given by:

$$V_{OUT} = VID - R_{FB} \cdot \frac{R_{SENSE}}{Rg} \cdot I_{OUT}$$

Figure 6. Output transient response without (a) and with (b) the droop function

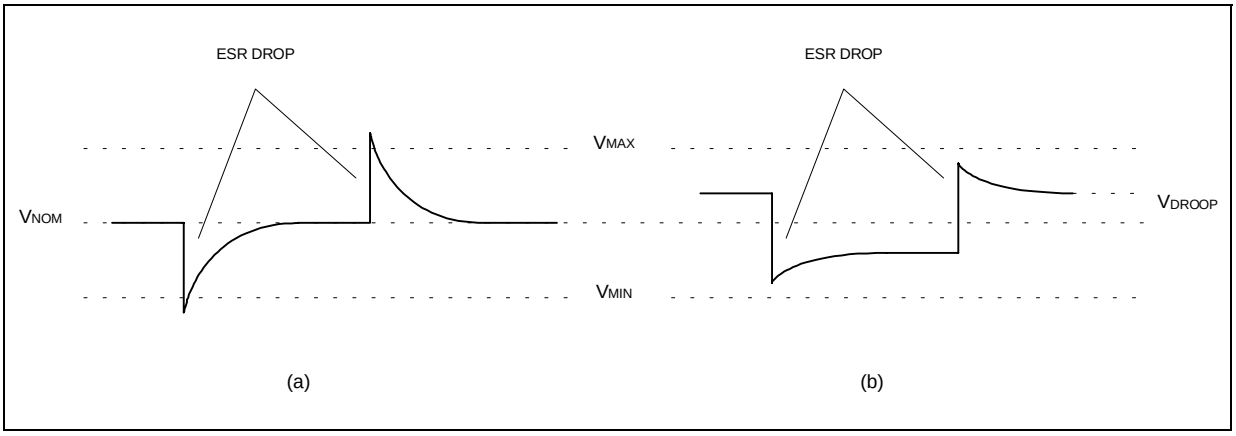
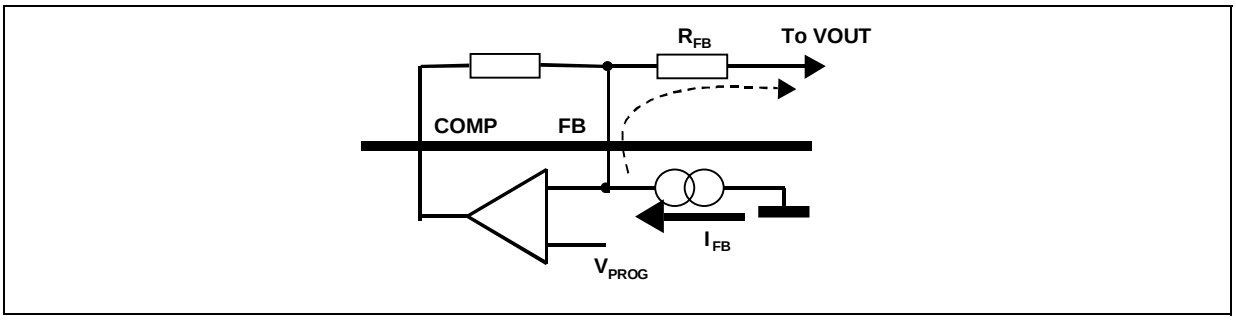


Figure 7. Active Droop Function Circuit



The feedback current is equal to 50µA at nominal full load ($I_{FB} = I_{INFO1} + I_{INFO2}$) and 70µA at the OC threshold, so the maximum output voltage deviation is equal to:

$$\Delta V_{FULL\_POSITIVE\_LOAD} = +R_{FB} \cdot 50\mu A \qquad \Delta V_{POSITIVE\_OC\_THRESHOLD} = +R_{FB} \cdot 70\mu A$$

Droop function is provided only for positive load; if negative load is applied, and then $I_{INFOx} < 0$, no current is sunk from the FB pin. The device regulates at the voltage programmed by the VID.

Output Voltage Protection and Power Good

The output voltage is monitored by pin VSEN. If it is not within +12/-10% (typ.) of the programmed value, the powergood output is forced low. Power good is an open drain output and it is enabled only after the soft start is finished (2048 clock cycles after start-up).

The device provides over voltage protection; when the voltage sensed by the V_{SEN} pin reaches 2.1V (typ.), the controller permanently switches on both the low-side mosfets and switches off both the high-side mosfets in order to protect the CPU. The OSC/INH/FAULT pin is driven high (5V) and power supply (Vcc) turn off and on is required to restart operations. The over Voltage percentage is set by the ratio between the OVP threshold (set at 2.1V) and the reference programmed by VID.

$$OVP[\%] = \frac{2.1V}{\text{Reference Voltage (VID)}} \cdot 100$$

Under voltage protection is also provided. If the output voltage drops below the 60% of the reference voltage for more than one clock period the device turns off and the FAULT pin is driven high.

Both Over Voltage and Under Voltage are active also during soft start (Under Voltage after than Vout reaches 0.8V). During soft-start the reference voltage used to determine the OV and UV thresholds is the increasing voltage driven by the 2048 soft start digital counter.

Remote Voltage Sense

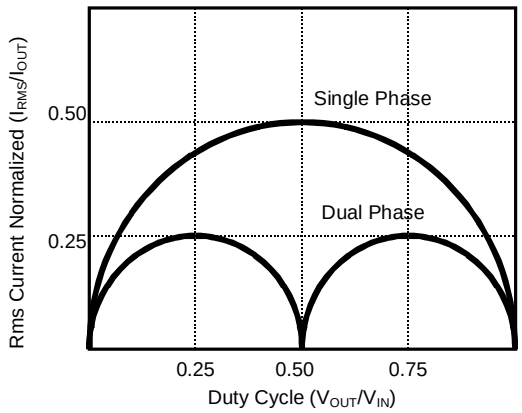
A remote sense buffer is integrated into the device to allow output voltage remote sense implementation without any additional external components. In this way, the output voltage programmed is regulated between the remote buffer inputs compensating motherboard trace losses or connector losses if the device is used for a VRM module. The very low offset amplifier senses the output voltage remotely through the pins FBR and FBG (FBR is for the regulated voltage sense while FBG is for the ground sense) and reports this voltage internally at VSEN pin with unity gain eliminating the errors.

If remote sense is not required, the output voltage is sensed by the VSEN pin connecting it directly to the output voltage. In this case the FBG and FBR pins must be connected anyway to the regulated voltage.

Input Capacitor

The input capacitor is designed considering mainly the input rms current that depends on the duty cycle as reported in figure 8. Considering the dual-phase topology, the input rms current is highly reduced comparing with a single phase operation.

Figure 8. Input rms Current vs. Duty Cycle (D) and Driving Relationships



$$I_{rms} = \begin{cases} \frac{I_{OUT}}{2} \cdot \sqrt{2D \cdot (1 - 2D)} & \text{if } D < 0.5 \\ \frac{I_{OUT}}{2} \cdot \sqrt{(2D - 1) \cdot (2 - 2D)} & \text{if } D > 0.5 \end{cases}$$

It can be observed that the input rms value is one half of the single-phase equivalent input current in the worst case condition that happens for D = 0.25 and D = 0.75.

The power dissipated by the input capacitance is then equal to:

$$P_{RMS} = ESR \cdot (I_{RMS})^2$$

Input capacitor is designed in order to sustain the ripple relative to the maximum load duty cycle. To reach the high rms value needed by the CPU power supply application and also to minimize components cost, the input capacitance is realized by more than one physical capacitor. The equivalent rms current is simply the sum of the single capacitor's rms current.

Input bulk capacitor must be equally divided between high-side drain mosfets and placed as close as possible to reduce switching noise above all during load transient. Ceramic capacitor can also introduce benefits in high frequency noise decoupling, noise generated by parasitic components along power path.

Output Capacitor

Since the microprocessors require a current variation beyond 50A doing load transients, with a slope in the range of tenth A/µs, the output capacitor is a basic component for the fast response of the power supply.

Dual phase topology reduces the amount of output capacitance needed because of faster load transient response (switching frequency is doubled at the load connections). Current ripple cancellation due to the 180° phase shift between the two phases also reduces requirements on the output ESR to sustain a specified voltage ripple.

When a load transient is applied to the converter's output, for first few microseconds the current to the load is supplied by the output capacitors. The controller recognizes immediately the load transient and increases the duty cycle, but the current slope is limited by the inductor value.

The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta V_{OUT} = \Delta I_{OUT} \cdot ESR$$

A minimum capacitor value is required to sustain the current during the load transient without discharge it. The voltage drop due to the output capacitor discharge is given by the following equation:

$$\Delta V_{OUT} = \frac{\Delta I_{OUT}^2 \cdot L}{2 \cdot C_{OUT} \cdot (V_{INMIN} \cdot D_{MAX} - V_{OUT})}$$

Where D_{MAX} is the maximum duty cycle value. The lower is the ESR, the lower is the output drop during load transient and the lower is the output voltage static ripple.

Inductor design

The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current ΔIL between 20% and 30% of the maximum output current. The inductance value can be calculated with this relationship:

$$L = \frac{V_{IN} - V_{OUT}}{fs \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

Where f_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage.

Increasing the value of the inductance reduces the ripple current but, at the same time, reduces the converter response time to a load transient. The response time is the time required by the inductor to change its current from initial to final value. Since the inductor has not finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required.

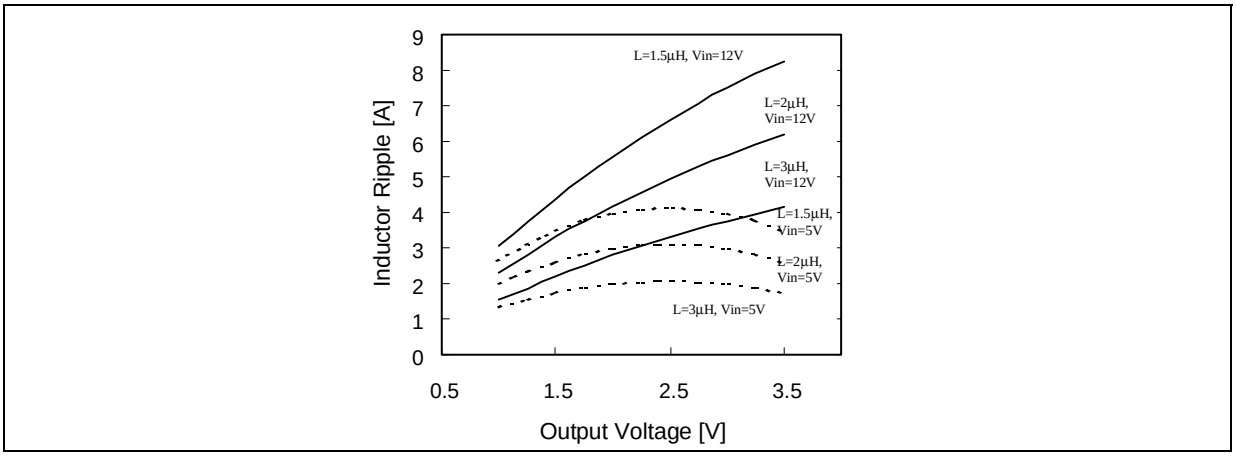
The response time to a load transient is different for the application or the removal of the load: if during the application of the load the inductor is charged by a voltage equal to the difference between the input and the output

voltage, during the removal it is discharged only by the output voltage. The following expressions give approximate response time for ΔI load transient in case of enough fast compensation network response:

$$t_{application} = \frac{L \cdot \Delta I}{V_{IN} - V_{OUT}} \qquad t_{removal} = \frac{L \cdot \Delta I}{V_{OUT}}$$

The worst condition depends on the input voltage available and the output voltage selected. Anyway the worst case is the response time after removal of the load with the minimum output voltage programmed and the maximum input voltage available.

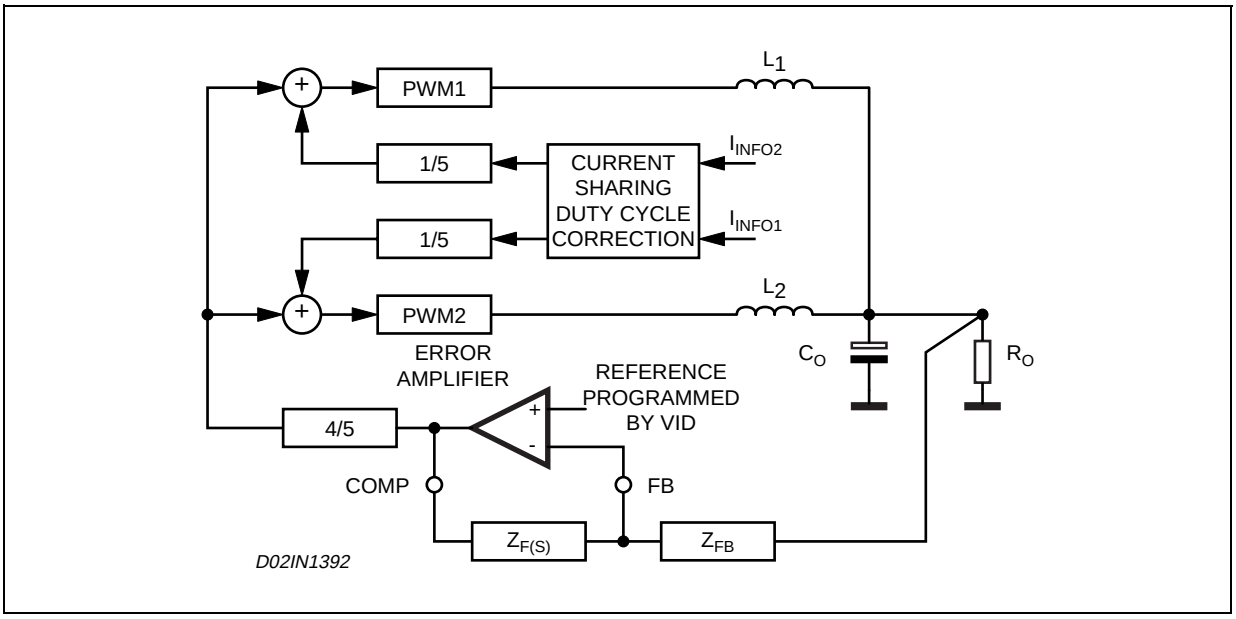
Figure 9. Inductor ripple current vs V_{out}



MAIN CONTROL LOOP

The L6917B control loop is composed by the Current Sharing control loop and the Average Current Mode control loop. Each loop gives, with a proper gain, the correction to the PWM in order to minimize the error in its regulation: the Current Sharing control loop equalize the currents in the inductors while the Average Current Mode control loop fixes the output voltage equal to the reference programmed by VID. Figure 10 reports the block diagram of the main control loop.

Figure 10. Main Control Loop Diagram



■ Current Sharing (CS) Control Loop

Active current sharing is implemented using the information from Tran conductance differential amplifier in an average current mode control scheme. A current reference equal to the average of the read current (I_{AVG}) is internally built; the error between the read current and this reference is converted to a voltage with a proper gain and it is used to adjust the duty cycle whose dominant value is set by the error amplifier at COMP pin (See fig. 11).

The current sharing control is a high bandwidth control loop allowing current sharing even during load transients.

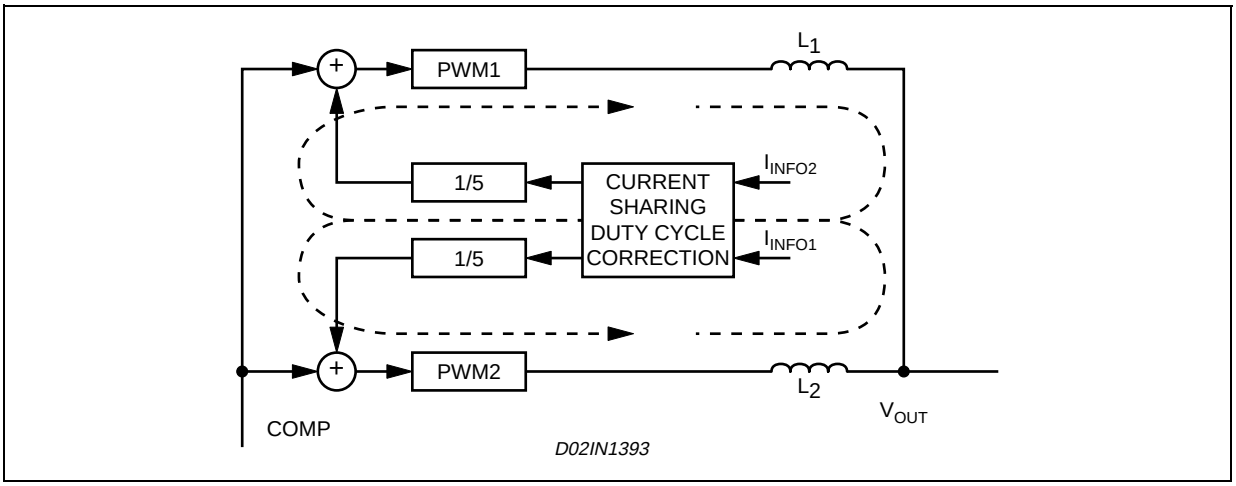
The current sharing error is affected by the choice of external components; choose precise Rg resistor (±1% is necessary) to sense the current. The current sharing error is internally dominated by the voltage offset of Tran conductance differential amplifier; considering a voltage offset equal to 2mV across the sense resistor, the current reading error is given by the following equation:

$$\frac{\Delta I_{READ}}{I_{MAX}} = \frac{2mV}{R_{SENSE} \cdot I_{MAX}}$$

Where ΔI_{READ} is the difference between one phase current and the ideal current ($I_{MAX}/2$).

For Rsense = 4mΩ and Imax = 40A the current sharing error is equal to 2.5%, neglecting errors due to Rg and Rsense mismatches.

Figure 11. Current Sharing Control Loop



■ Average Current Mode (ACM) Control Loop

The average current mode control loop is reported in figure 12. The current information IFB sourced by the FB pin flows into RFB implementing the dependence of the output voltage from the read current.

The ACM control loop gain results (obtained opening the loop after the COMP pin):

$$G_{LOOP}(s) = \frac{PWM \cdot Z_F(s) \cdot (R_{DROOP} + Z_P(s))}{(Z_P(s) + Z_L(s)) \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

Where:

– $R_{DROOP} = \frac{R_{sense}}{R_g} \cdot R_{FB}$ is the equivalent output resistance determined by the droop function;

– $Z_P(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load Ro;

– $Z_F(s)$ is the compensation network impedance;
– $Z_L(s)$ is the parallel of the two inductor impedance;
– A(s) is the error amplifier gain;
– $PWM = \frac{4}{5} \cdot \frac{\Delta V_{IN}}{\Delta V_{OSC}} \cdot$ is the ACM PWM transfer function where DVosc is the oscillator ramp amplitude and has a typical value of 2V

Removing the dependence from the Error Amplifier gain, so assuming this gain high enough, the control loop gain results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{Z_P(s) + Z_L(s)} \cdot \left(\frac{Rs}{Rg} + \frac{Z_P(s)}{R_{FB}} \right)$$

With further simplifications, it results:

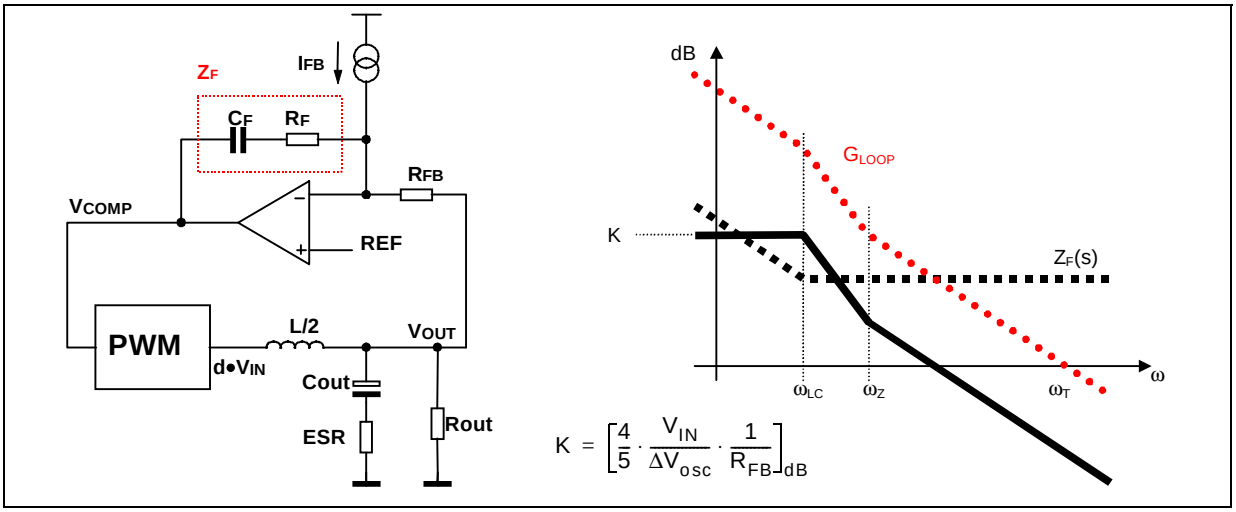
$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{Ro + R_{DROOP}}{Ro + \frac{R_L}{2}} \cdot \frac{1 + s \cdot Co \cdot (R_{DROOP} // Ro + ESR)}{s^2 \cdot Co \cdot \frac{L}{2} + s \cdot \left[\frac{L}{2 \cdot Ro} + Co \cdot ESR + Co \cdot \frac{R_L}{2} \right] + 1}$$

Considering now that in the application of interest it can be assumed that $Ro >> R_L$; $ESR << Ro$ and $R_{DROOP} << Ro$, it results:

$$G_{LOOP}(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{1 + s \cdot Co \cdot (R_{DROOP} + ESR)}{s^2 \cdot Co \cdot \frac{L}{2} + s \cdot \left[\frac{L}{2 \cdot Ro} + Co \cdot ESR + Co \cdot \frac{R_L}{2} \right] + 1}$$

The ACM control loop gain is designed to obtain a high DC gain to minimize static error and cross the 0dB axes with a constant -20dB/dec slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles. Both the poles are fixed once the output filter is designed and the zero is fixed by ESR and the Droop resistance. To obtain the desired shape an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F = 1/R_F C_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero in correspondence with the L-C resonance a simple -20dB/dec shape of the gain is assured (See Figure 12). In fact, considering the usual value for the output filter, the LC resonance results to be at frequency lower than the above reported zero.

Figure 12. ACM Control Loop Gain Block Diagram (left) and Bode Diagram (right)



Compensation network can be simply designed placing $\omega_Z = \omega_{LC}$ and imposing the cross-over frequency ω_T as desired obtaining:

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \omega_T \cdot \frac{L}{2 \cdot (R_{DROOP} + ESR)} \cdot \frac{5}{4} \qquad C_F = \frac{\sqrt{Co \cdot \frac{L}{2}}}{R_F}$$

LAYOUT GUIDELINES

Since the device manages control functions and high-current drivers, layout is one of the most important things to consider when designing such high current applications.

A good layout solution can generate a benefit in lowering power dissipation on the power paths, reducing radiation and a proper connection between signal and power ground can optimise the performance of the control loops.

Integrated power drivers reduce components count and interconnections between control functions and drivers, reducing the board space.

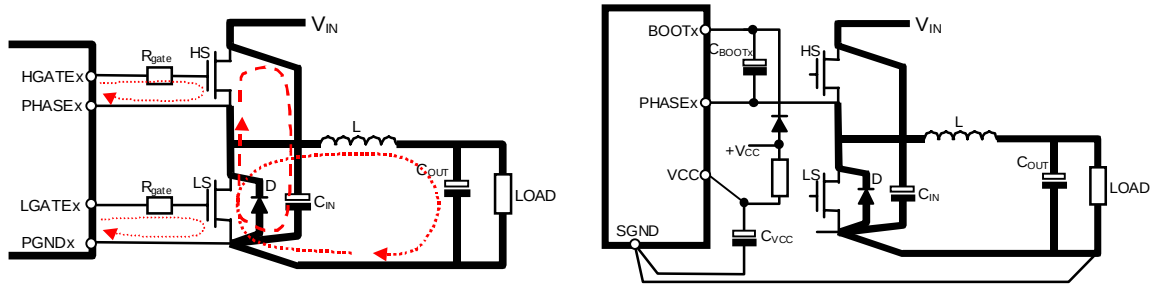
Here below are listed the main points to focus on when starting a new layout and rules are suggested for a correct implementation.

■ Power Connections.

These are the connections where switching and continuous current flows from the input supply towards the load. The first priority when placing components has to be reserved to this power section, minimizing the length of each connection as much as possible.

To minimize noise and voltage spikes (EMI and losses) these interconnections must be a part of a power plane and anyway realized by wide and thick copper traces. The critical components, i.e. the power transistors, must be located as close as possible, together and to the controller. Considering that the "electrical" components reported in fig. 13 are composed by more than one "physical" component, a ground plane or "star" grounding connection is suggested to minimize effects due to multiple connections.

Figure 13. Power connections and related connections layout guidelines (same for both phases)



a. PCB power and ground planes areas

b. PCB small signal components placement

Fig. 13a shows the details of the power connections involved and the current loops. The input capacitance (CIN), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors (electrolytic or Ceramic or both) are required.

■ Power Connections Related.

Fig.13b shows some small signal components placement, and how and where to mix signal and power ground planes.

The distance from drivers and mosfet gates should be reduced as much as possible. Propagation delay times

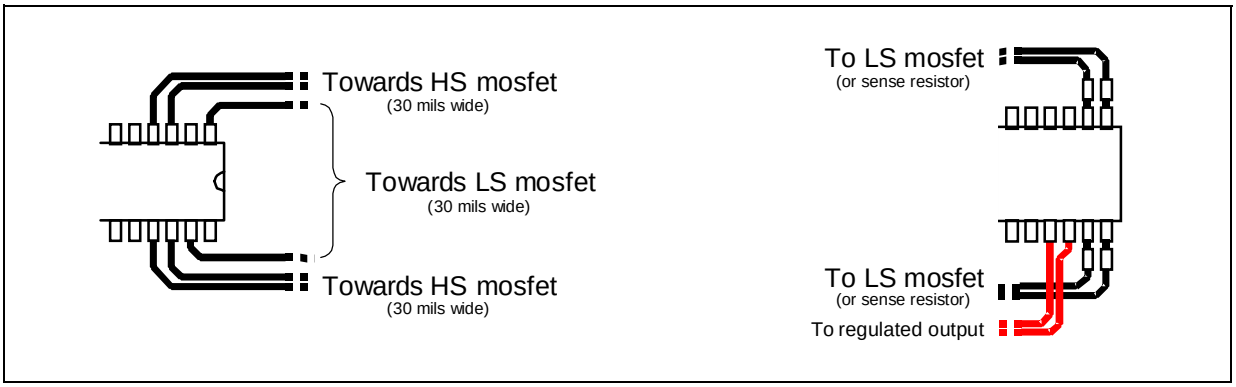
as well as for the voltage spikes generated by the distributed inductance along the copper traces are so minimized.

In fact, the further the mosfet is from the device, the longer is the interconnecting gate trace and as a consequence, the higher are the voltage spikes corresponding to the gate pwm rising and falling signals. Even if these spikes are clamped by inherent internal diodes, propagation delays, noise and potential causes of instabilities are introduced jeopardizing good system behavior. One important consequence is that the switching losses for the high side mosfet are significantly increased.

For this reason, it is suggested to have the device oriented with the driver side towards the mosfets and the GATEx and PHASEx traces walking together toward the high side mosfet in order to minimize distance (see fig 14). In addition, since the PHASEx pin is the return path for the high side driver, this pin must be connected directly to the High Side mosfet Source pin to have a proper driving for this mosfet. For the LS mosfets, the return path is the PGND pin: it can be connected directly to the power ground plane (if implemented) or in the same way to the LS mosfets Source pin. GATEx and PHASEx connections (and also PGND when no power ground plane is implemented) must also be designed to handle current peaks in excess of 2A (30 mils wide is suggested).

Gate resistors of few ohms help in reducing the power dissipated by the IC without compromising the system efficiency.

Figure 14. Device orientation (left) and sense nets routing (right)



The placement of other components is also important:

– The bootstrap capacitor must be placed as close as possible to the BOOTx and PHASEx pins to minimize the loop that is created.
– Decoupling capacitor from Vcc and SGND placed as close as possible to the involved pins.
– Decoupling capacitor from VCCDR and PGND placed as close as possible to those pins. This capacitor sustains the peak currents requested by the low-side mosfet drivers.
– Refer to SGND all the sensible components such as frequency set-up resistor (when present) and also the optional resistor from FB to GND used to give the positive droop effect.
– Connect SGND to PGND on the load side (output capacitor) to avoid undesirable load regulation effect and to ensure the right precision to the regulation when the remote sense buffer is not used.
– An additional 100nF ceramic capacitor is suggested to place near HS mosfet drain. This helps in reducing noise.
– PHASE pin spikes. Since the HS mosfet switches in hard mode, heavy voltage spikes can be observed on the PHASE pins. If these voltage spikes overcome the max breakdown voltage of the pin, the device can absorb energy and it can cause damages. The voltage spikes must be limited by proper layout, the use of gate resistors, Schottky diodes in parallel to the low side mosfets and/or snubber network on the low side mosfets, to a value lower than 26V, for 20nSec, at Fosc of 600kHz max.

■ **Current Sense Connections.**

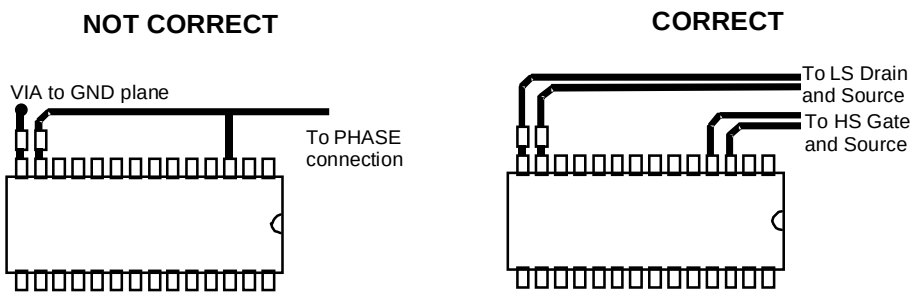
Remote Buffer: The input connections for this component must be routed as parallel nets from the FBG/FBR

pins to the load in order to compensate losses along the output power traces and also to avoid the pick-up of any common mode noise. Connecting these pins in points far from the load will cause a non-optimum load regulation, increasing output tolerance.

Current Reading: The Rg resistor has to be placed as close as possible to the ISENx and PGNDSx pins in order to limit the noise injection into the device. The PCB traces connecting these resistors to the reading point must be routed as parallel traces in order to avoid the pick-up of any common mode noise. It's also important to avoid any offset in the measurement and to get a better precision, to connect the traces as close as possible to the sensing elements, dedicated current sense resistor or low side mosfet Rdson.
Moreover, when using the low side mosfet RdsON as current sense element, the ISENx pin is practically connected to the PHASEx pin. DO NOT CONNECT THE PINS TOGETHER AND THEN TO THE HS SOURCE! The device won't work properly because of the noise generated by the return of the high side driver. In this case route two separate nets: connect the PHASEx pin to the HS Source (route together with HGATEx) with a wide net (30 mils) and the ISENx pin to the LS Drain (route together with PGNDSx). Moreover, the PGNDSx pin is always connected, through the Rg resistor, to the PGND: DO NOT CONNECT DIRECTLY TO THE PGND! In this case, the device won't work properly. Route anyway to the LS mosfet source (together with ISENx net). Right and wrong connections are reported in Figure 15.

Symmetrical layout is also suggested to avoid any unbalance between the two phases of the converter.

Figure 15. PCB layout connections for sense nets



Wrong (left) and correct (right) connections for the current reading sensing nets.

APPLICATION EXAMPLES

The dual-pahse topology can be applied to several different applications ranging from CPU power supply (for which the device has been designed) to standard high current DC-DC power supply. The application benefits of all the advantages due to the dual-phase topology ranging from output ripple reduction to dynamic performance increase. After a general demo board overview, the following application examples will be illustrated:

- CPU Power Supply: 5 to 12 V_{IN}; 1.7V_{OUT}; 45A
- CPU Power Supply: 12V_{IN}; VRM 9.0 Output; 50A
- High Current DC-DC: 12V_{IN}; 3.3 to 5V_{OUT}T; 35A

Demo Board Description

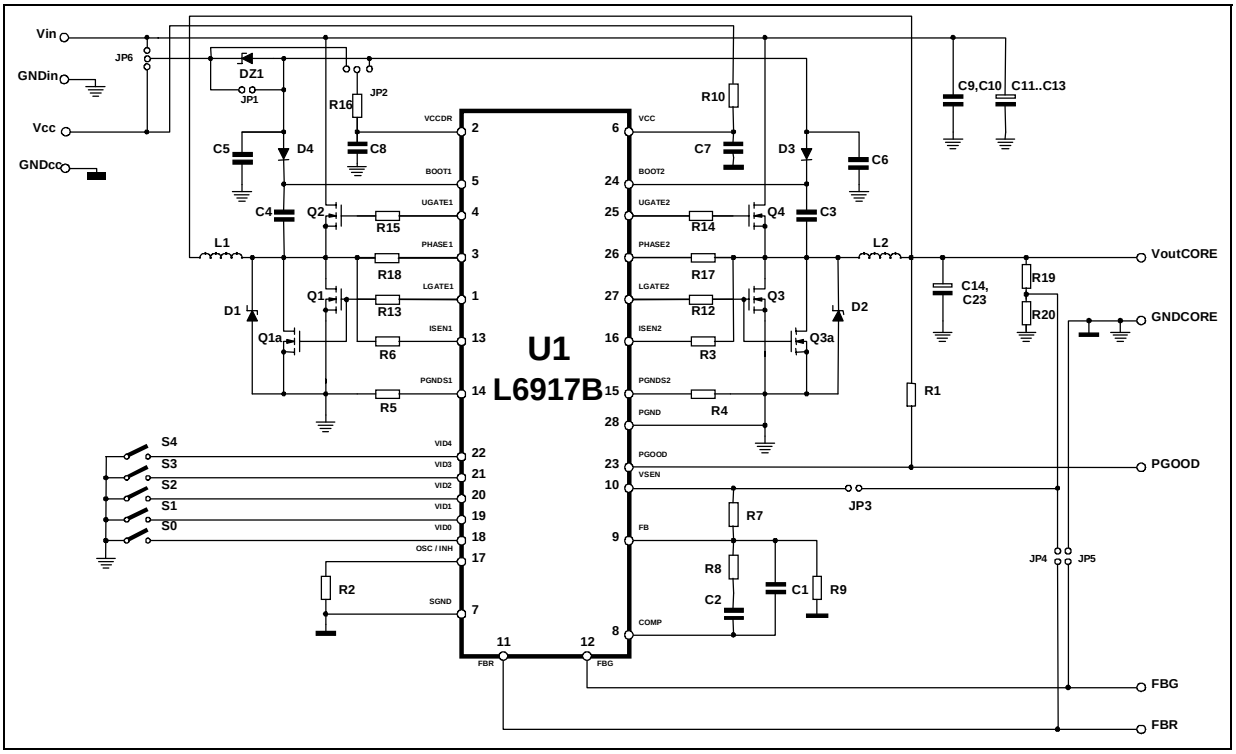
The demo board shows the operation of the device in a dual phase application. This evaluation board allows output voltage adjustability (1.100V - 1.850V) through the switches S0-S4 and high output current capability.

The board has been laid out with the possibility to use up to two D^2PACK mosfets for the low side switch in order to give maximum flexibility in the mosfet's choice.

The four layers demo board's copper thickness is of 70µm in order to minimize conduction losses considering the high current that the circuit is able to deliver.

Demo board schematic circuit is reported in Figure 16.

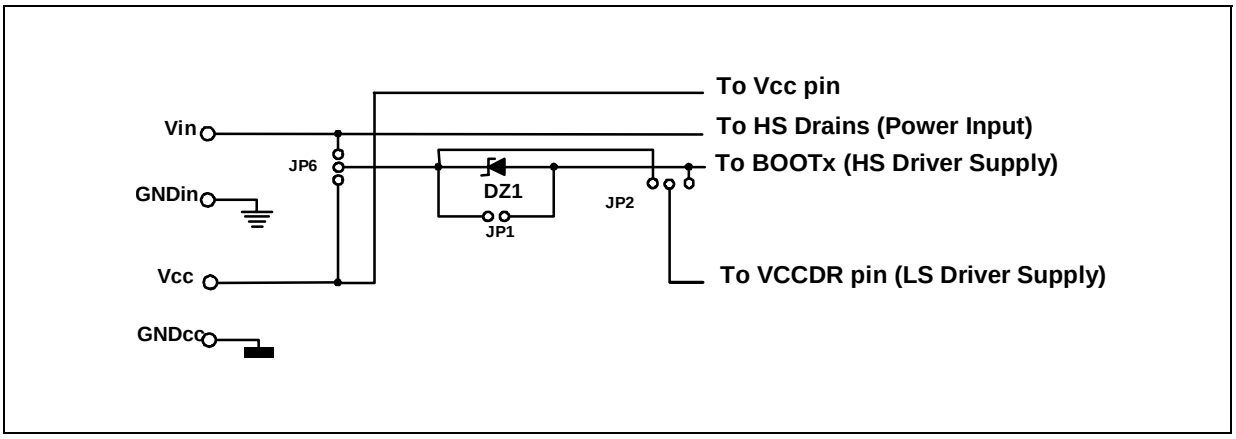
Figure 16. Demo Board Schematic



Several jumpers allow setting different configurations for the device: JP3, JP4 and JP5 allow configuring the remote buffer as desired. Simply shorting JP4 and JP5 the remote buffer is enabled and it senses the output voltage on-board; to implement a real remote sense, leave these jumpers open and connect the FBG and FBR connectors on the demo board to the remote load. To avoid using the remote buffer, simply short all the jumpers JP3, JP4 and JP5. Local sense through the R7 is used for the regulation.

The input can be configured in different ways using the jumpers JP1, JP2 and JP6; these jumpers control also the mosfet driver supply voltage. Anyway, power conversion starts from VIN and the device is supplied from V_{CC} (See Figure 17).

Figure 17. Power supply configuration

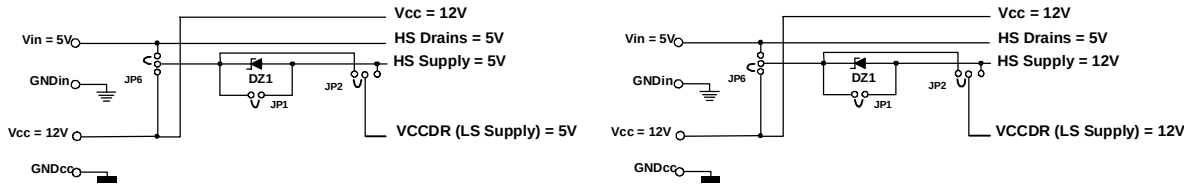


Two main configurations can be distinguished: Single Supply (V_{CC} = V_{IN} = 12V) and Double Supply (V_{CC} = 12V V_{IN} = 5V or different).

– Single Supply: In this case JP6 has to be completely shorted. The device is supplied with the same rail that is used for the conversion. With an additional zener diode DZ1 a lower voltage can be derived to supply the mosfets driver if Logic level mosfet are used. In this case JP1 must be left open so that the HS driver is supplied with V_{IN}-V_{DZ1} through BOOTx and JP2 must be shorted to the left to use V_{IN} or to the right to use V_{IN}-V_{DZ1} to supply the LS driver through VCCDR pin. Otherwise, JP1 must be shorted and JP2 can be freely shorted in one of the two positions.
– Double Supply: In this case V_{CC} supply directly the controller (12V) while V_{IN} supplies the HS drains for the power conversion. This last one can start indifferently from the 5V bus (Typ.) or from other buses allowing maximum flexibility in the power conversion. Supply for the mosfet driver can be programmed through the jumpers JP1, JP2 and JP6 as previously illustrated. JP6 selects now V_{CC} or V_{IN} depending on the requirements.

Some examples are reported in the following Figures 18 and 19.

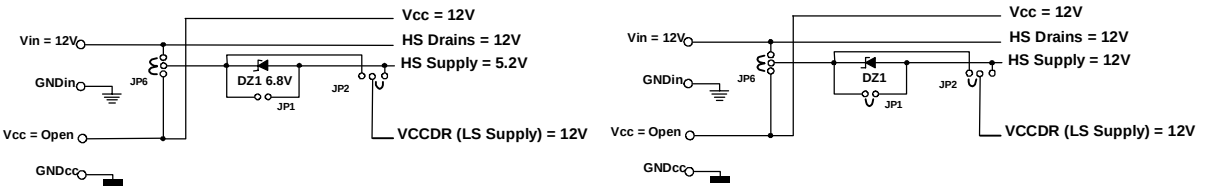
Figure 18. Jumpers configuration: Double Supply



(a) V_{CC} = 12V; V_{BOOTx} = VCCDR = V_{IN} = 5V

(b) V_{CC} = V_{BOOTx} = VCCDR =12V; V_{IN} = 5V

Figure 19. Jumpers configuration: Single Supply

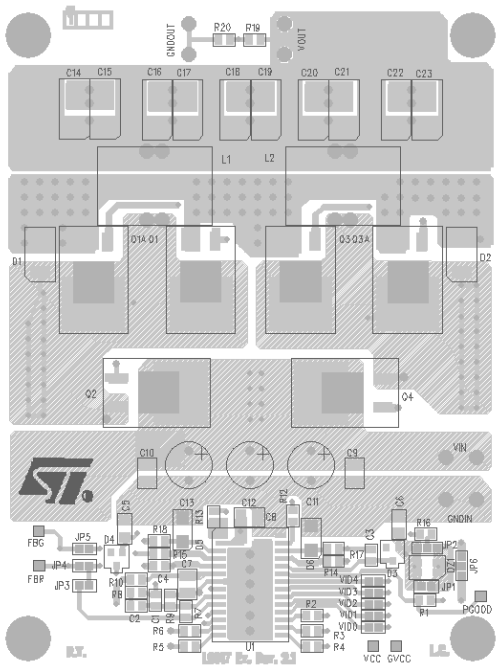


(a) V_{CC} = V_{IN} = VCCDR = 12V; V_{BOOTx} = 5.2V

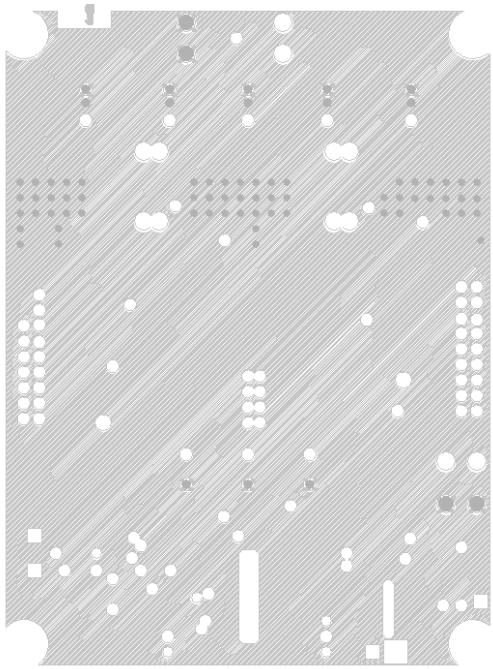
(b) V_{CC} = V_{IN}= V_{BOOTx} = VCCDR = 12V

PCB and Components Layouts

Figure 20. PCB and Components Layouts

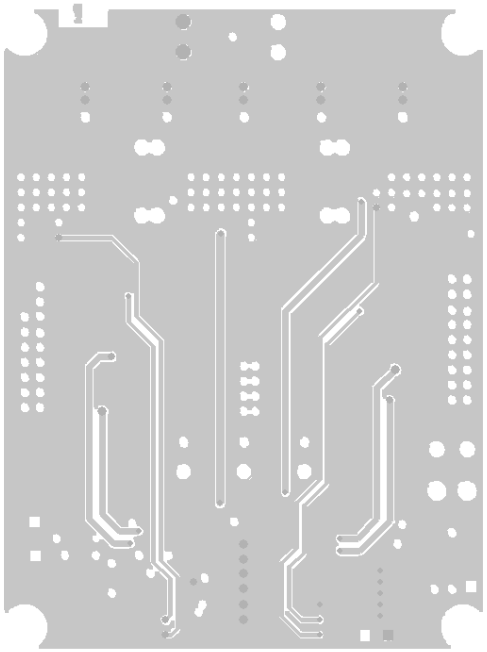


Component Side

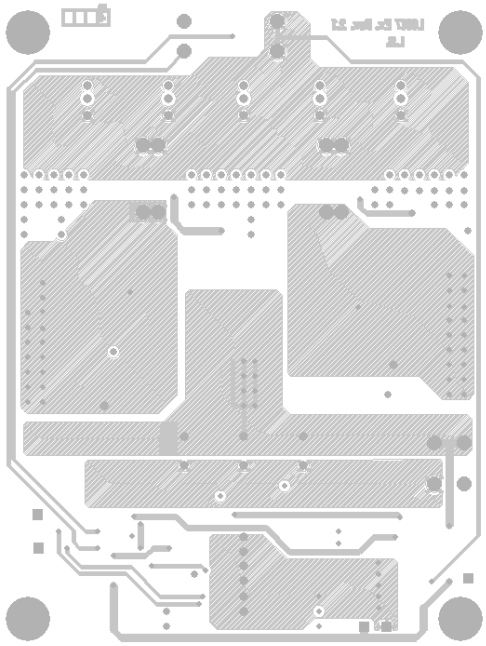


Internal PGND Plane

Figure 21. PCB and Components Layouts



Internal SGND Plane



Solder Side

CPU Power Supply: 5 to 12V_{IN}; 1.7V_{OUT}; 45A

Considering the high slope for the load transient, a high switching frequency has to be used. In addition to fast reaction, this helps in reducing output and input capacitor. Inductance value is also reduced.

A switching frequency of 200kHz for each phase is then considered allowing large bandwidth for the compensation network. It can be considered to use the 5V rail for the power conversion in order to allow compatibility with standard ATX power supply.

– Current Reading Network and Over Current:
Since the maximum output current is I_{MAX} = 45A, the over current threshold has been set to 46A (23A per phase) in the worst case (max mosfet temperature). This because the device limits the valley of the triangular ripple across the inductors. Considering to sense the output current across the low-side mosfet RdsON, STB90NF03L has 6.5mΩ max at 25°C that becomes 9.1mΩ considering the temperature variation (+40%); the resulting Tran conductance resistor Rg has to be:

$$Rg = \frac{I_{MAX}}{2} \cdot \frac{RdsON}{35\mu} = \frac{46}{2} \cdot \frac{9.1m}{35\mu} = 5.9k\Omega \qquad \text{(R3 to R6)}$$

– Droop function Design:
Considering a voltage drop of 100mv at full load, the feedback resistor RFB has to be:

$$R_{FB} = \frac{100mV}{70\mu A} = 1.43k\Omega \qquad \text{(R7)}$$

– Inductor design:
Each phase has to deliver up to 22.5A; considering a current ripple of 5A (<25%), the resulting inductance value is:

$$L = \frac{Vin - Vout}{\Delta I} \cdot \frac{d}{Fsw} = \frac{12 - 1.7}{5} \cdot \frac{1.7}{12} \cdot \frac{1}{300000} = 1\mu H \qquad \text{(L1, L2)}$$

– Output Capacitor:

Five Rubycon MBZ (2200µF / 6.3V / 12mΩ max ESR) has been used implementing a resulting ESR of 2.4mΩ resulting in an ESR voltage drop of 45A*2.4mΩ = 108mV after a 45A load transient.

– Compensation Network:

A voltage loop bandwidth of 20kHz is considered to let the device fast react after load transient.

The R_F C_F network results:

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{5}{4} \cdot \omega_T \cdot \frac{L}{2 \cdot (R_{DROOP} + ESR)} = \frac{1.43k \cdot 2}{12} \cdot \frac{5}{4} \cdot 20k \cdot 2\pi \cdot \frac{1\mu}{2 \cdot \left(\frac{9.1m}{5.9k} \cdot 1.43k + 2.4m\right)} = 6200\Omega \quad \text{(R8)}$$

$$C_F = \frac{\sqrt{Co \cdot \frac{L}{2}}}{R_F} = \frac{\sqrt{6 \cdot 2200\mu \cdot \frac{1\mu}{2}}}{6.2k} = 15nF \qquad \text{(C2)}$$

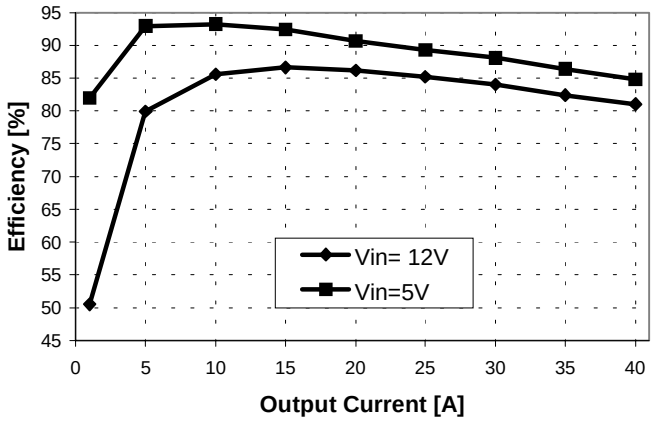
Part List

R1	10k		SMD 0805
R2, R20	Not Mounted		SMD 0805
R3, R4, R5, R6	5.1k	1%	SMD 0805
R7	1.43k	1%	SMD 0805
R8	6.2k		SMD 0805
R10	82Ω		SMD 0805
R12 to R16, R19	2.2Ω		SMD 0805
R17, R18	0Ω		SMD 0805
C2	15n		SMD 0805
C3, C4	100n		SMD 0805
C5, C6, C7	1µ	Ceramic	SMD 1206
C8, C9, C10	10µ	Ceramic	SMD 1206
C11, C12, C13	1800µ / 16V	Rubycon MBZ	Radial 23x10.5
C19 to C24	2200µ / 6.3V	Rubycon MBZ	Radial 23x10.5
L1, L2	1µ	TO50 – 52B – 6 Turns	
U1	L6917B	STMicroelectronics	SO28
Q1, Q3	STB90NF03L	STMicroelectronics	D^2PACK
Q2, Q4	STB70NF03L	STMicroelectronics	D^2PACK
D1, D2	STPS340U	STMicroelectronics	SMB
D3, D4	1N4148	STMicroelectronics	SOT23

System Efficiency

Figure 22 shows the demo board measured efficiency versus load current for different values of input voltage. Mosfet temperature is always lower than 115 °C, at T_{amb} = 25°C.

Figure 22. Efficiency (f_{osc} = 200kHz; Vout = 1.7V)

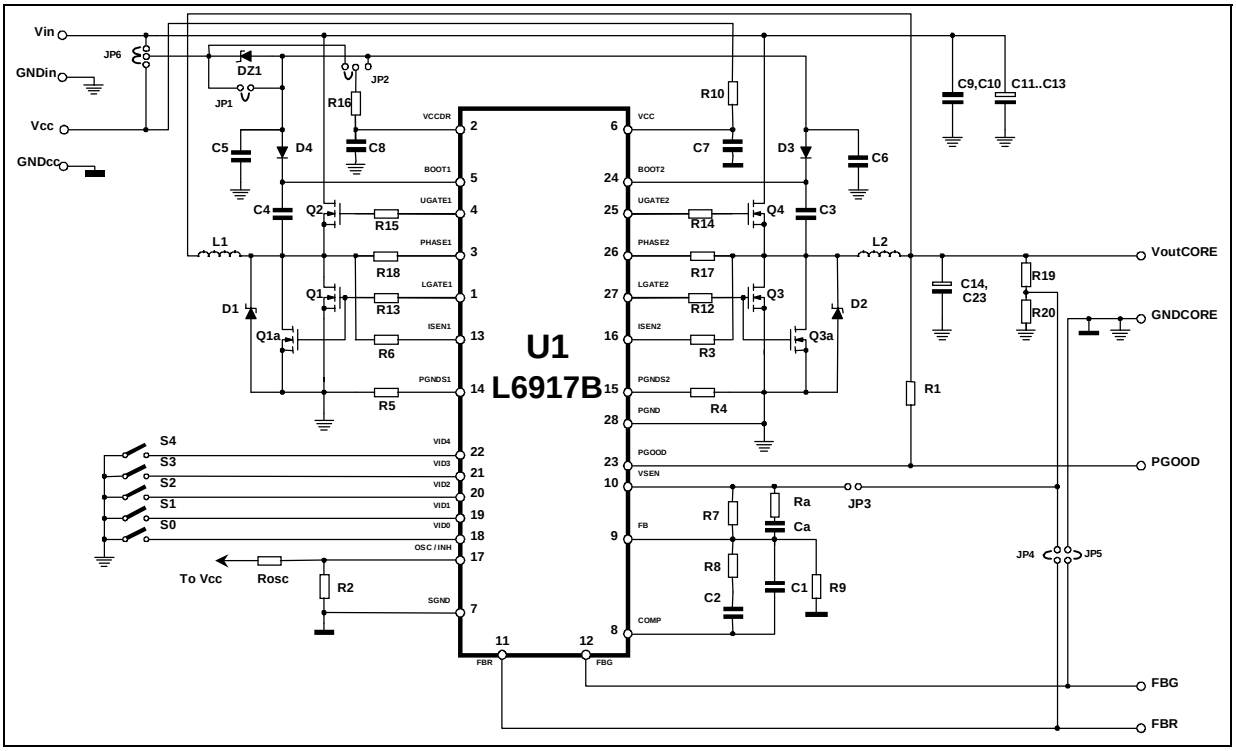


CPU Power Supply: $12V_{IN}$ - VRM 9.0 - 50A thermal

Figure 23 shows the device in a high current CPU core power supply solution.

The output voltage can be adjusted with binary step from 1.100V to 1.850V following VRM 9.0 specifications. The demo board assembled with the following part list is capable to deliver up to 50A in open air without any kind of airflow. Peak current can reach 60A without any limitations. For higher DC current, to avoid mosfet change, airflow or heat sink are required.

Figure 23. CPU Power Supply Schematic



Part List

R1	10k		SMD 0805
R2, R9	Not Mounted		SMD 0805
R3, R4, R5, R6	3.3k	1%	SMD 0805
R7	3.6k	1%	SMD 0805
R8	3.3k		SMD 0805
R10	82		SMD 0805
R12 to R15	2.2		SMD 0805
R16, R17, R18	0		SMD 0805
Ra	1k		SMD 0805
Rosc	1.3M	1%	SMD 0805
C1	Not Mounted		SMD 0805

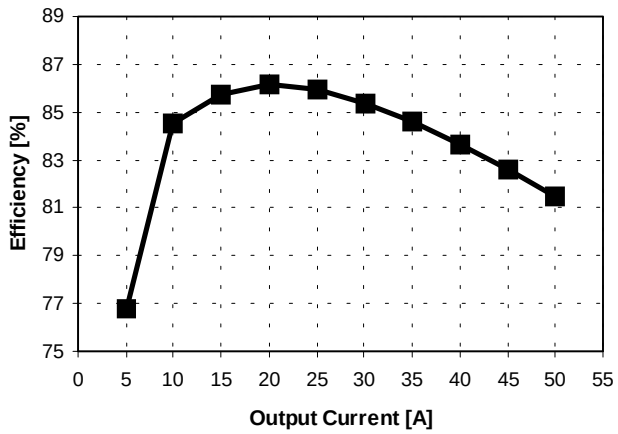
Part List (continued)

C2	47n		SMD 0805
C3, C4	100n	Ceramic	SMD 0805
C5, C6, C7, C8	1µ	Ceramic	SMD 1206
C9, C10	10µ	Ceramic	SMD 1206
C11 to C13	1800µ/ 16V	Rubycon MBZ	Radial 10x10.5
C14 to C23	2200µ/ 6.3V	Rubycon MBZ	Radial 10x10.5
Ca	68n		SMD 0805
L1, L2	0.5µ	77121 Core – 3 Turns	
U1	L6917B	STMicroelectronics	SO28
Q1,Q1a, Q3,Q3a	SUB85N03-04P	Vishay - Siliconix	D^2PACK
Q2, Q4	SUB70N03-09BP	Vishay - Siliconix	D^2PACK
D1, D2	STPS340U	STMicroelectronics	SMB
D3, D4	1N4148	STMicroelectronics	SOT23

Efficiency

Figure 24 showes the system efficiency for output current ranging form 5A up to 50A.

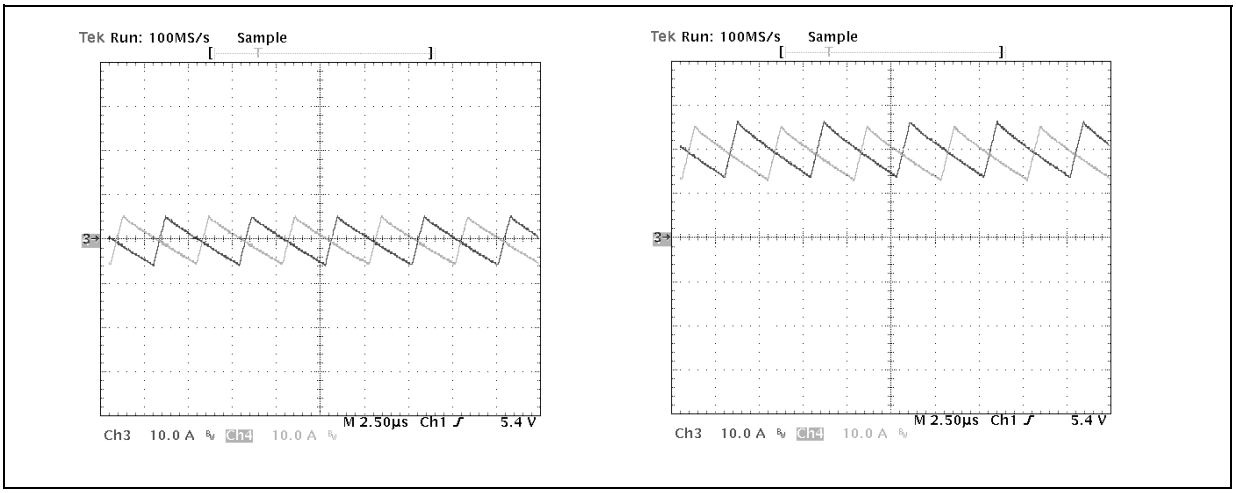
Figure 24. Efficiency (f_{osc} = 200kHz; Vout = 1.7V)



Current Sharing

Figure 25 shows the current balancing between the two phases for different values of output current.

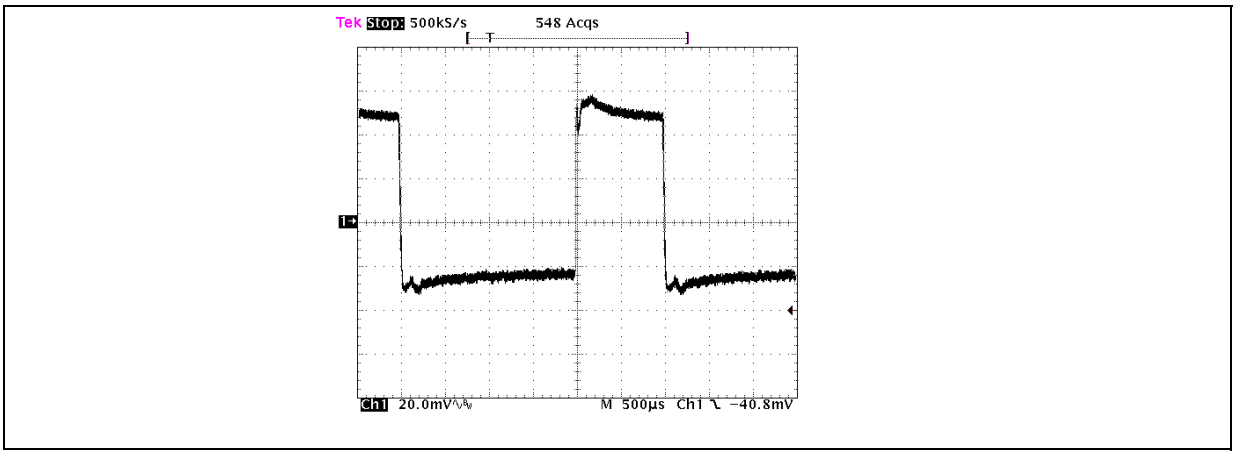
Figure 25.



Load Transient Response

Figure 26 shows the system response from 0 to 50A load transient. To obtain such a response, 5 additional capacitors have been added to the output filter to reproduce the motherboard output filter. Noise can be further reduced by adding ceramic decoupling capacitors.

Figure 26. 1.7V Output Voltage Ripple During 0 to 50A Load Transient



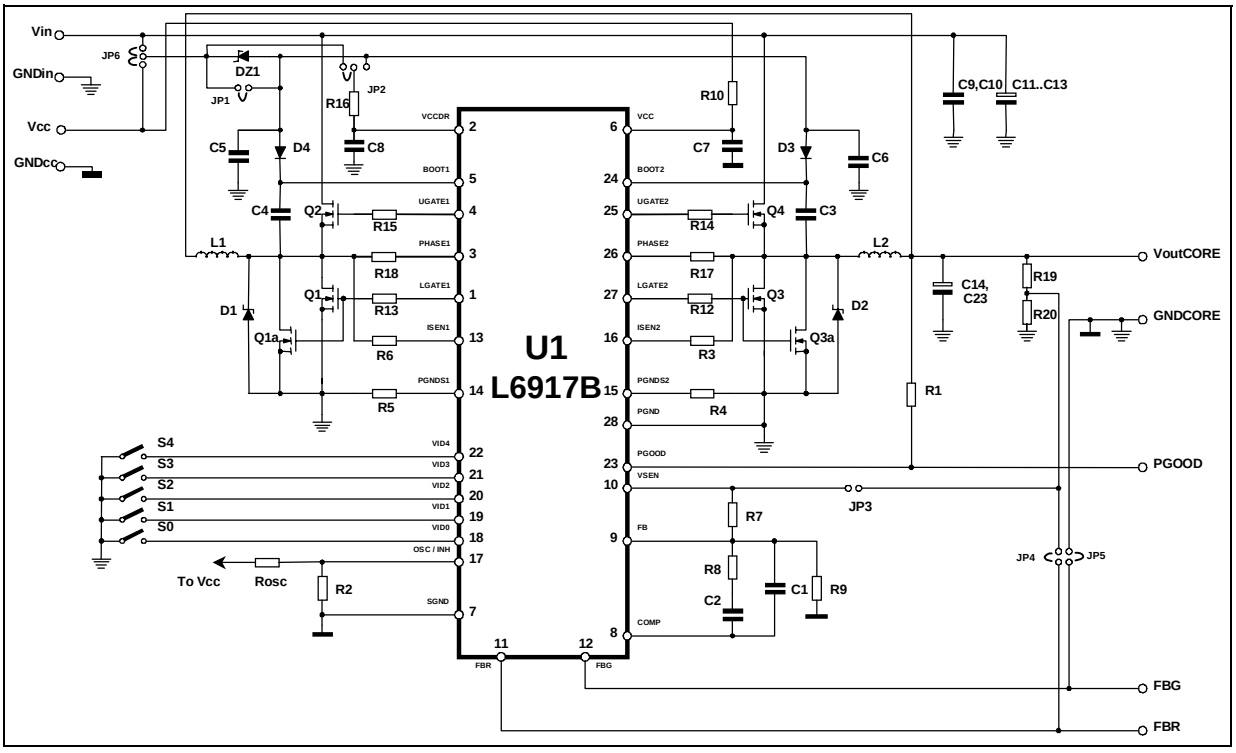
High Current DC-DC: 12V_{IN} - 3.3 (or 5V) OUT - 35A

Figure 27 shows the device in a high current server power supply application.

Adding an external resistor divider after the remote sense buffer gives the possibility to increase the regulated voltage. Considering for example a divider by two (two equal resistors) the DAC range is doubled from 2.200V to 3.700V with 50mV binary steps. The external resistor divider must be designed in order to give negligible effects to the remote buffer gain, this means that the resistors value must be much lower than the remote buffer input resistance (20kΩ). In this way, it is possible to regulate the 3.3V and 2.5V rails from the 12V available from the AC/DC converter. The 5V rail can be obtained with further modifications to the external divider. The regulator assures all the advantages of the dual phase conversion especially in the 5V conversion where the duty cycle is near the 50% and practically no ripple is present in the input capacitors.

The board is able to deliver up to 35A "thermal" at T_{amb} 25°C without airflow. Higher currents can be reached for reasonable times considering the overall dynamic thermal capacitance.

Figure 27. Server power supply schematic



The following part list refers to the following application:

- Input Voltage: 12V;
- Output voltage: 3.3V;
- Oscilator frequency: 200kHz;
- Output voltage tolerance (over static and dynamic conditions): ±2.5%.

Part List

R1	10k		SMD 0805
R2, R9	Not Mounted		SMD 0805
R3, R6	1.3k	1%	SMD 0805
R4, R5	390	1%	SMD 0805
R7	75	1%	SMD 0805
R8	750		SMD 0805
R10	82		SMD 0805
R12 to R15	2.2		SMD 0805
R16, R17, R18	0		SMD 0805
R19	300	1%	SMD 0805
R20	390	1%	SMD 0805
R_{OSC}	1.3M	1%	SMD 0805
C1	Not Mounted		SMD 0805
C2	220n		SMD 0805
C3, C4	100n	Ceramic	SMD 0805
C5, C6, C7, C8	1µ	Ceramic	SMD 1206
C9, C10	10µ	Ceramic	SMD 1206
C11 to C13	100µ/ 20V	OSCON 20SA100M	Radial 10x10.5
C14,C16,C18,C20,C22	2200µ/16V	SANYO	Radial 10x23
L1, L2	2.8µ	77121 Core – 9 Turns	
U1	L6917B	STMicroelectronics	SO28
Q1,Q1a,Q2, Q3,Q3a,Q4	STB90NF03L	STMicroelectronics	D^2PACK
D1, D2	STPS340U	STMicroelectronics	SMB
D3, D4	1N4148	STMicroelectronics	SOT23
DZ1	Not Mounted		Minimelf

Figure 28. System Efficiency for a 12V/3.3V Application (f_{osc} = 200kHz)

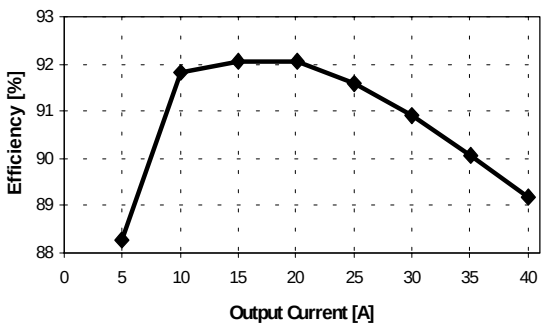
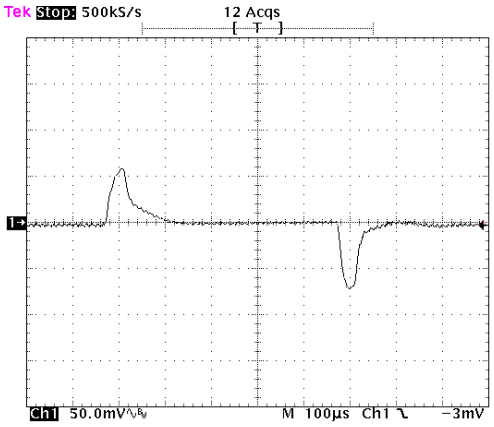
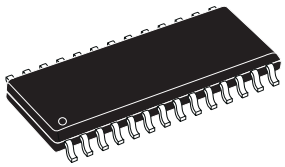


Figure 29. Load Transient Response: 0A to 35A @ 1A/µs



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO28