



HIGH PERFORMANCE 2A ULDO LINEAR REGULATOR

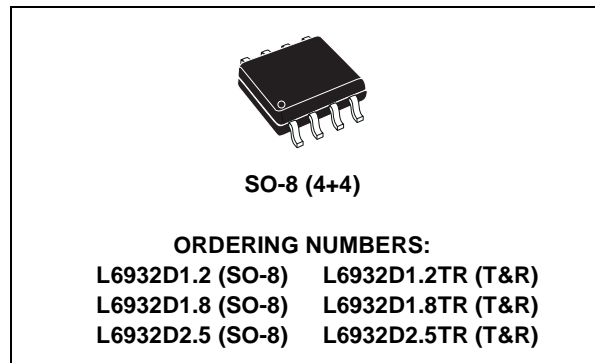
- 2V TO 14V INPUT VOLTAGE RANGE
- 200mΩ R_{dson} MAX.
- 200μA QUIESCENT CURRENT AT ANY LOAD
- EXCELLENT LOAD AND LINE REGULATION
- 1.8V AND 2.5V FIXED VOLTAGE
- ADJUSTABLE FROM 1.2V TO 5V (L6932D1.2)
- 1% VOLTAGE REGULATION ACCURACY
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN
- SO-8 (4+4) PACKAGE

APPLICATIONS

- MOTHERBOARDS
- MOBILE PC
- HAND-HELD INSTRUMENTS
- PCMCIA CARDS
- PROCESSORS I/O
- CHIPSET AND RAM SUPPLY

DESCRIPTION

The L6932 Ultra Low Drop Output linear regulator operates from 2V to 14V and is able to support 2A. Designed with an internal 50mΩ N-channel



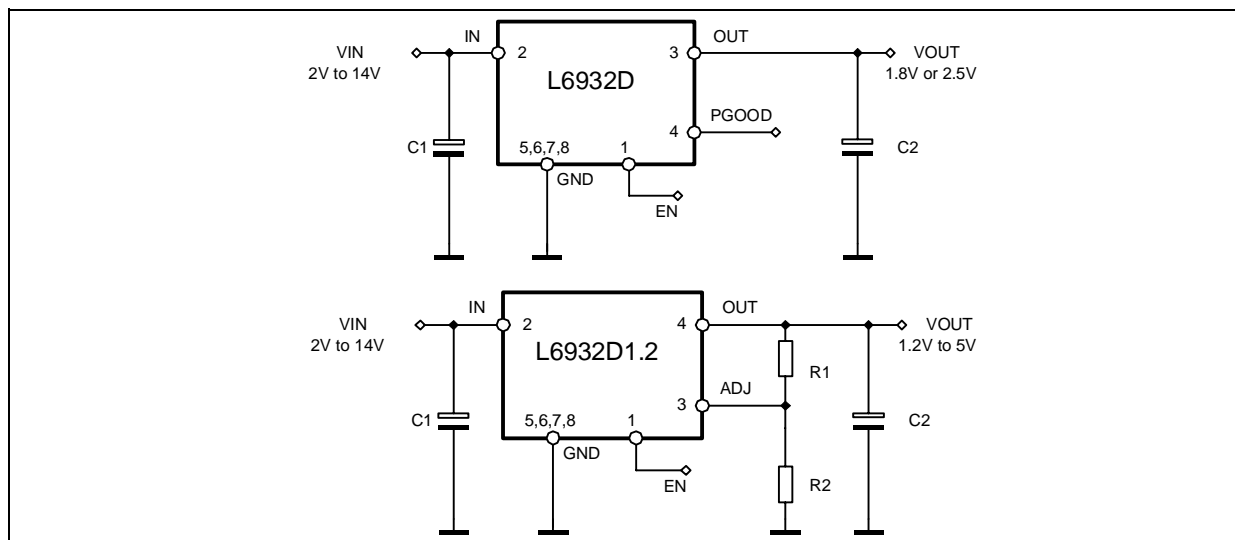
Mosfet, can be useful for the DC-DC conversion between 2.5V and 1.8V at 2A in portable applications reducing the power dissipation.

L6932 is available in 1.8V, 2.5V and adj version from 1.2V and ensure a voltage regulation accuracy of 1%.

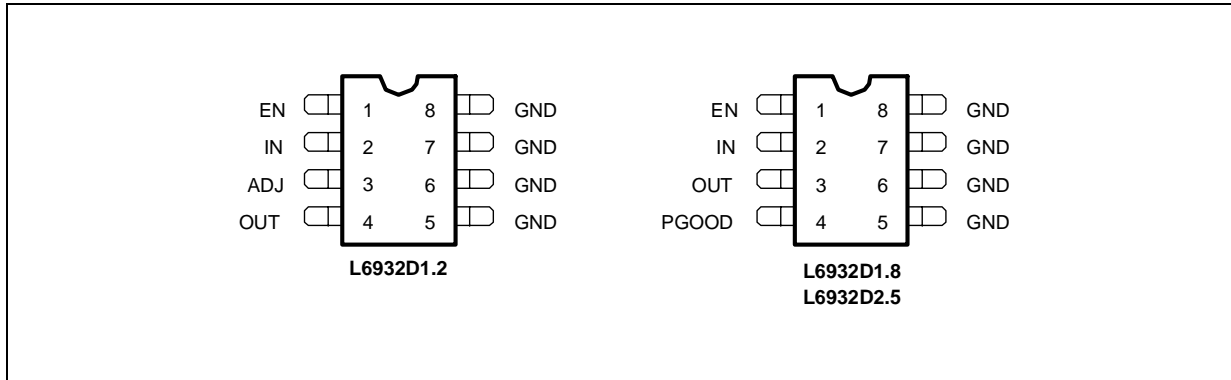
The current limit is fixed at 2.5A to control the current in short circuit condition within ±8%. The current is sensed in the power mos in order to limit the power dissipation.

The device is also provided of a thermal shut down that limits the internal temperature at 150°C with an hysteresis of 20°C. L6932 provides the Enable and the Power good functions.

TYPICAL OPERATING CIRCUIT



PIN CONNECTIONS



PIN FUNCTION

| N° | L6232D 1.2 | L6232D 1.8/2.5 | Description |
|------------|------------|----------------|--|
| 1 | EN | | Enables the device if connected to V_{in} and disables the device if forced to gnd. |
| 2 | IN | | Supply voltage. This pin is connected to the drain of the internal N-mos. Connect this pin to a capacitor larger than 10 μ F. |
| 3 | ADJ | – | Connecting this pin to a voltage divider it is possible to programme the output voltage between 1.2V and 5V. |
| | – | OUT | Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10 μ F. |
| 4 | OUT | – | Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10 μ F. |
| | – | PGOOD | Power good output. The pin is open drain and detects the output voltage. It is forced low if the output voltage is lower than 90% of the programmed voltage. |
| 5, 6, 7, 8 | GND | | Ground pin. |

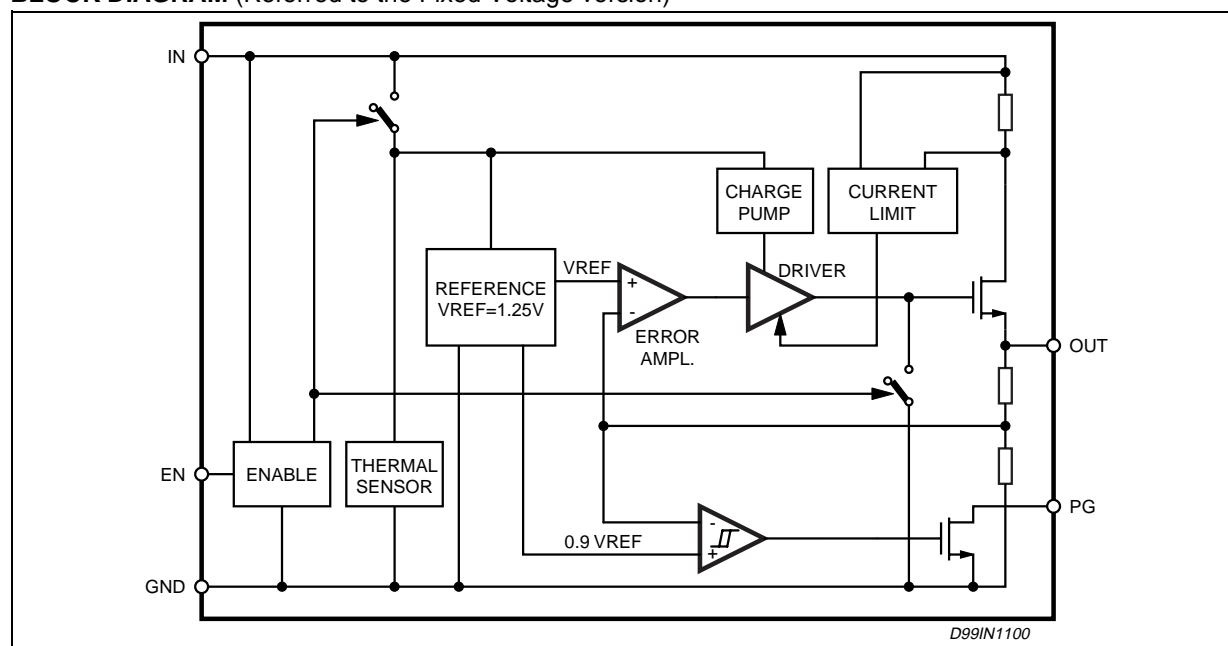
ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------|-----------------|----------------------------|------|
| V_{in} | VIN and Pgood | 14.5 | V |
| | EN, OUT and ADJ | -0.3 to ($V_{in} + 0.3$) | V |

THERMAL DATA

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|---------------|
| $R_{th J-amb}$ | Thermal Resistance Junction to Ambient | 62 (*) | $^{\circ}C/W$ |
| T_{max} | Maximum Junction Temperature | 150 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | -65 to 150 | $^{\circ}C$ |

(*) Measured on Demoboard with about 4 cm² of dissipating area 2 Oz.

BLOCK DIAGRAM (Referred to the Fixed Voltage version)**ELECTRICAL CHARACTERISTICS** ($T_j = 25^\circ\text{C}$, $V_{IN} = 5\text{V}$ unless otherwise specified)(*) Specification referred to T_j from -25°C to 125°C .

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------|------------------------------|--|-------|------|-------|---------------|
| V_{in} | Operating Supply Voltage | | 2 | | 14 | V |
| V_o | Output voltage L6932D1.2 | $I_o = 0.1\text{A}$; $V_{in} = 3.3\text{V}$ | 1.188 | 1.2 | 1.212 | V |
| | Output voltage L6932D1.8 | $I_o = 0.1\text{A}$; $V_{in} = 3.3\text{V}$ | 1.782 | 1.8 | 1.818 | V |
| | Output voltage L6932D2.5 | $I_o = 0.1\text{A}$; $V_{in} = 3.3\text{V}$ | 2.475 | 2.5 | 2.525 | V |
| | L6932D1.2 Line Regulation | $V_{in} = 2.5\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | | $V_{in} = 3.3\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | | $V_{in} = 5\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | L6932D1.8 Line Regulation | $V_{in} = 2.5\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | | $V_{in} = 3.3\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | | $V_{in} = 5\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | L6932D2.5 Line Regulation | $V_{in} = 3.3\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | | $V_{in} = 5\text{V} \pm 10\%$; $I_o = 10\text{mA}$ | | | 5 | mV |
| | L6932D1.2 Load Regulation | $V_{in} = 3.3\text{V}$; $0.1\text{A} < I_o < 2\text{A}$ | | | 15 | mV |
| | L6932D1.8 Load Regulation | $V_{in} = 3.3\text{V}$; $0.1\text{A} < I_o < 2\text{A}$ | | | 15 | mV |
| | L6932D2.5 Load Regulation | $V_{in} = 3.3\text{V}$; $0.1\text{A} < I_o < 2\text{A}$ | | | 15 | mV |
| R_{dson} | Drain Source ON resistance | | | | 200 | m Ω |
| I_{occ} | Current limiting | | 2.3 | 2.5 | 2.7 | A |
| I_q | Quiescent current | | | 0.2 | 0.4 | mA |
| I_{sh} | Shutdown current | $2\text{V} < V_{in} < 14\text{V}$ | * | | 25 | μA |
| | Ripple Rejection | $f = 120\text{Hz}$, $I_o = 1\text{A}$ $V_{in} = 5\text{V}$, $\Delta V_{in} = 2\text{Vpp}$ | 60 | 75 | | dB |
| V_{en} | EN Input Threshold | | 0.5 | 0.65 | 0.8 | V |

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--------|------------------|--------------------------|------|------|------|---------|
| | Pgood threshold | V_o rise | | 90 | | % V_o |
| | Pgood Hysteresis | | | 10 | | % V_o |
| | Pgood saturation | $I_{pgood} = 1\text{mA}$ | | 0.2 | 0.4 | V |

Figure 1. Output Voltage vs. Junction Temperature (L6932D1.2)

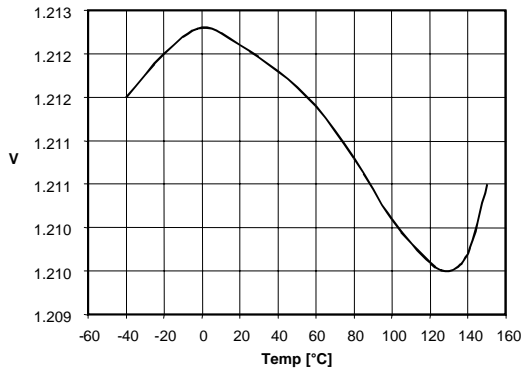


Figure 4. Quiescent Current vs. Junction Temperature

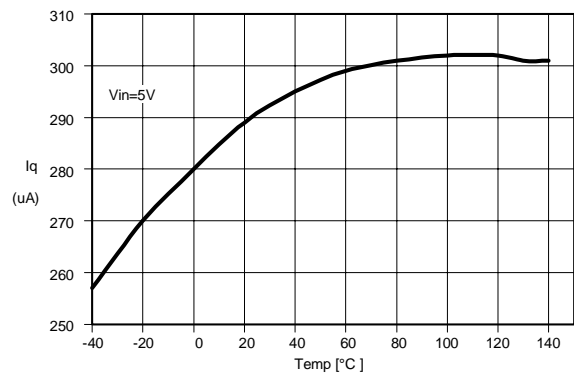


Figure 2. Output Voltage vs. Junction Temperature (L6932D1.8)

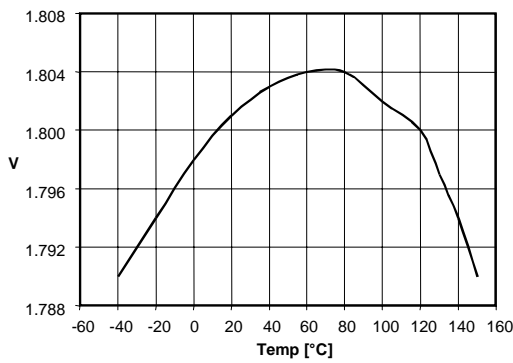


Figure 5. Shutdown Current vs. Junction Temperature

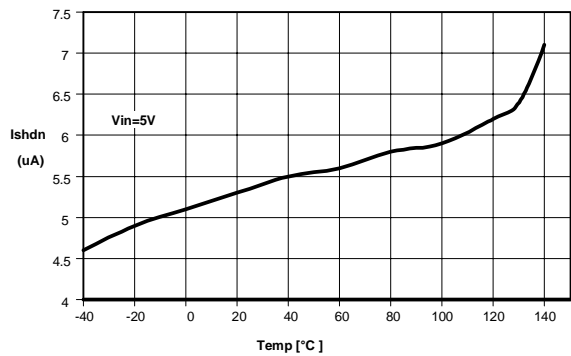
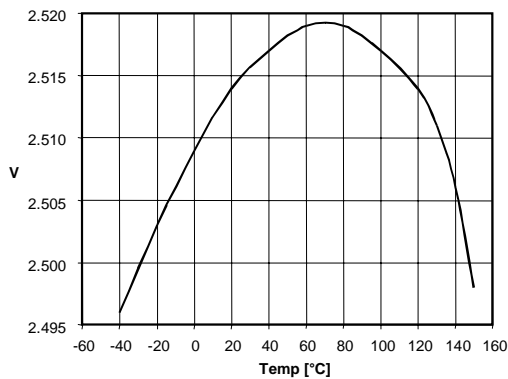


Figure 3. Output Voltage vs. Junction Temperature (L6932D2.5)

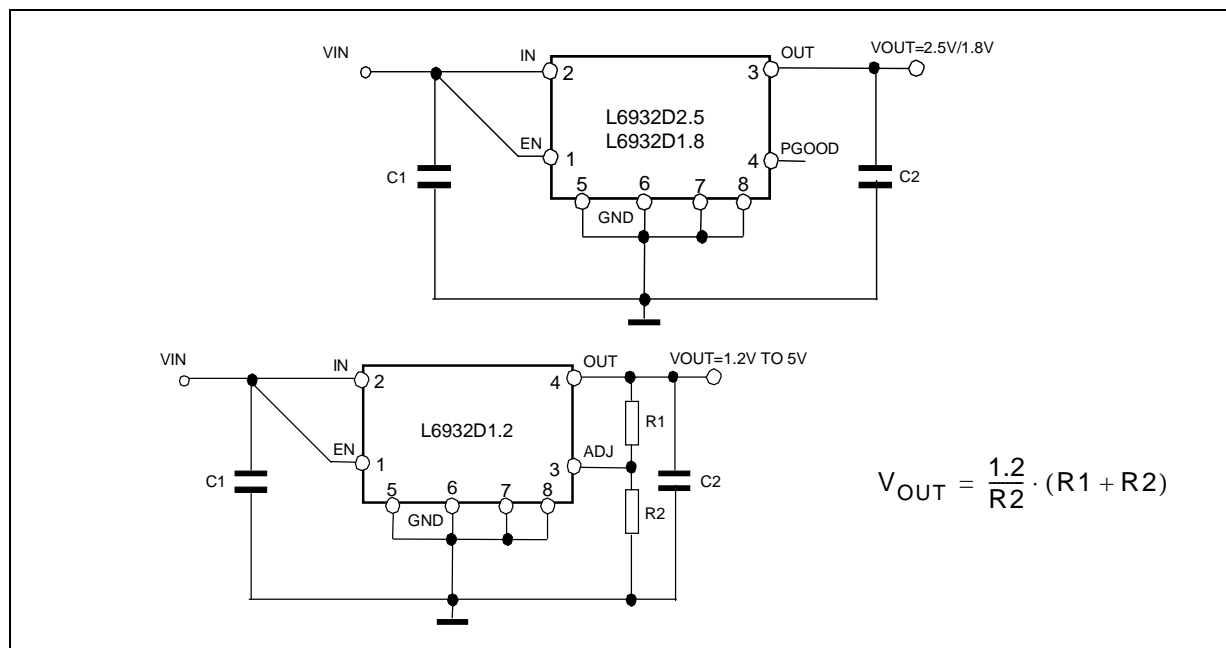


APPLICATION INFORMATION

APPLICATION CIRCUIT

In figure 6 the schematic circuit of the demoboards are shown.

Figure 6. Demoboards Schematic Circuit

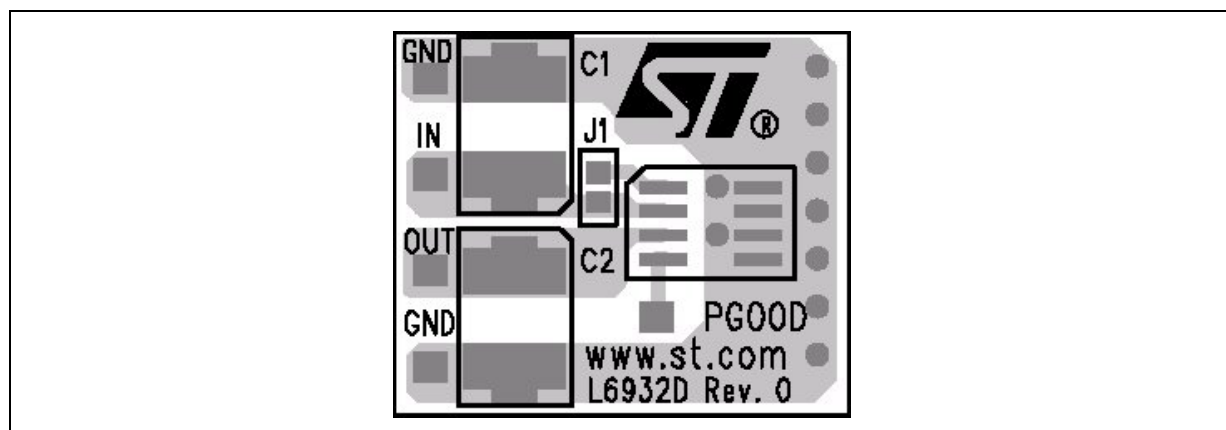


COMPONENT LIST

Fixed version

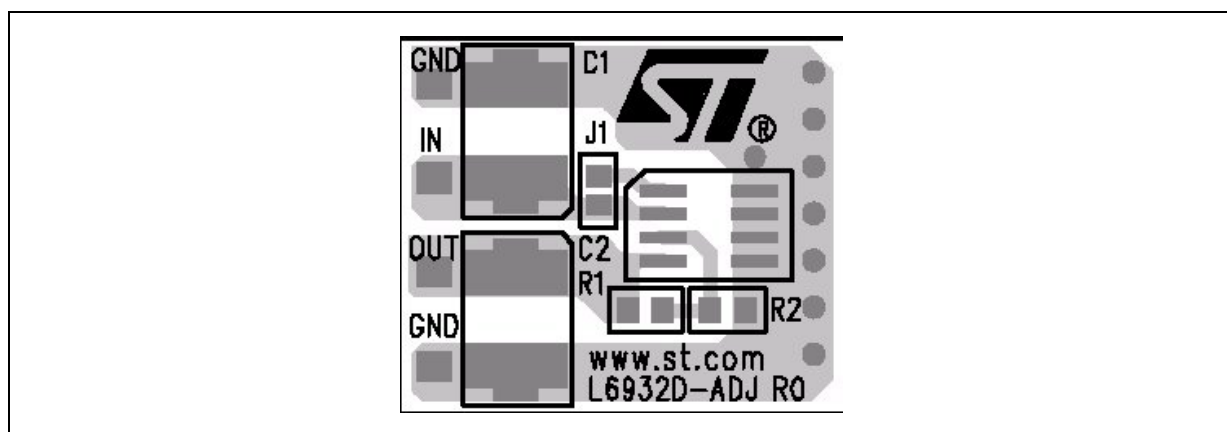
| Reference | Part Number | Description | Manufacturer |
|-----------|--------------|-------------|--------------|
| C1 | C34Y5U1E106Z | 10uF, 25V | TOKIN |
| C2 | C34Y5U1E106Z | 10uF, 25V | TOKIN |

Figure 7. Demoboard Layout (Fixed Version)



Adjustable version

| Reference | Part Number | Description | Manufacturer |
|-----------|--------------|-----------------|--------------|
| C1 | C34Y5U1E106Z | 10uF, 25V | TOKIN |
| C2 | C34Y5U1E106Z | 10uF, 25V | TOKIN |
| R1 | | 5.6K, 1%, 0.25W | Neohm |
| R2 | | 3.3K, 1%, 0.25W | Neohm |

Figure 8. Demoboard Layout (Adjustable Version)**COMPONENTS SELECTION****Input Capacitor**

The input capacitor value depends on a lot of factors such as load transient requirements, input source (battery or DC/DC converter) and its distance from the input cap. Usually a 47 μ F is enough for any application but a much lower value can be sufficient in many cases.

Output Capacitor

The output capacitor choice depends basically on the load transient requirements.

Tantalum, Speciality Polimer, POSCAP and aluminum capacitors are good and offer very low ESR values.

Multilayer ceramic caps have the lowest ESR and can be required for particular applications. Nevertheless in several applications they are ok, the loop stability issue has to be considered (see loop stability section).

Below a list of some suggested capacitor manufacturers.

| Manufacturer | Type | Cap Value (μ F) | Rated Voltage (V) |
|--------------|----------|----------------------|-------------------|
| PANASONIC | CERAMIC | 1 to 47 | 4 to 16 |
| TAYO YUDEN | CERAMIC | 1 to 47 | 4 to 16 |
| TDK | CERAMIC | 1 to 47 | 4 to 16 |
| TOKIN | CERAMIC | 1 to 47 | 4 to 16 |
| SANYO | POSCAP | 1 to 47 | 4 to 16 |
| PANASONIC | SP | 1 to 47 | 4 to 16 |
| KEMET | TANTALUM | 1 to 47 | 4 to 16 |

Loop Stability

The stability of the loop is affected by the zero introduced by the output capacitor.

The time constant of the zero is given by:

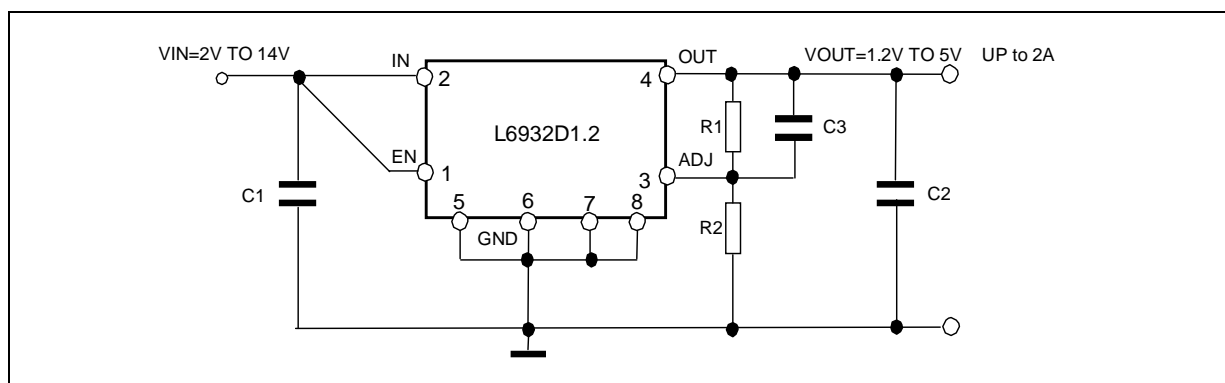
$$T = \text{ESR} \cdot C_{\text{OUT}} \quad F_{\text{ZERO}} = \frac{1}{2\pi \cdot \text{ESR} \cdot C_{\text{OUT}}}$$

This zero helps to increase the phase margin of the loop until the time constant is higher than some hundreds of nsec, depending also on the output voltage and current.

So, using very low ESR ceramic capacitors could produce oscillations at the output, in particular when regulating high output voltages (adjustable version).

To solve this issue is sufficient to add a small capacitor (e.g. 1nF to 10nF) in parallel to the high side resistor of the external divider, as shown in figure 9.

Figure 9. Compensation Network



Thermal Considerations

Since the device is housed in a small SO(4+2+2) package the thermal issue can be the bottleneck of many applications. The power dissipated by the device is given by:

$$P_{\text{DISS}} = (V_{\text{IN}} - V_{\text{OUT}}) \cdot I_{\text{OUT}}$$

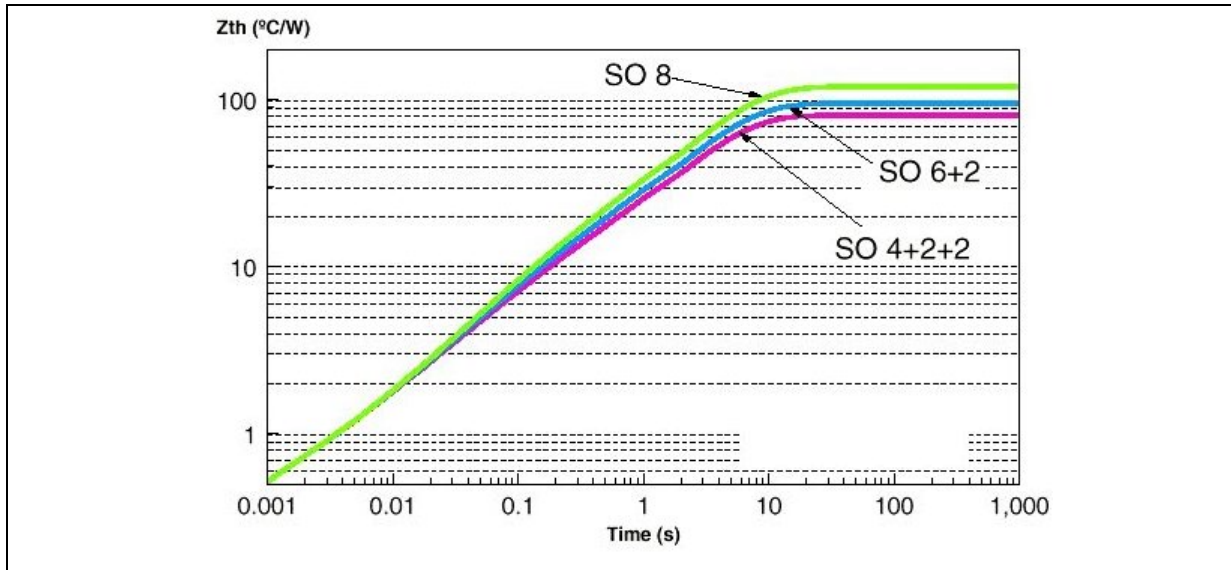
The thermal resistance junction to ambient of the demoboard is approximately 62°C/W. This means that, considering an ambient temperature of 60°C and a maximum junction temperature of 150°C, the maximum power that the device can handle is 1.5W.

This means that the device is able to deliver a DC output current of 2A only with a very low dropout.

In many applications, high output current pulses are required. If their duration is shorter than the thermal constant time of the board, the thermal impedance (not the thermal resistance) has to be considered.

In figure 10 the thermal impedance versus the duration of the current pulse for the SO(4+2+2) mounted on board is shown.

Figure 10. Thermal Impedance



Considering a pulse duration of 1sec, the thermal impedance is close to 20 $^{\circ}C/W$, allowing much bigger power dissipated.

Example:

$V_{in} = 3.3V$

$V_{out} = 1.8V$

$I_{out} = 2A$

Pulse Duration = 1 sec

The power dissipated by the device is:

$$P_{DISS} = (V_{IN} - V_{OUT}) \cdot I_{OUT} = 1.5 \cdot 2 = 3W$$

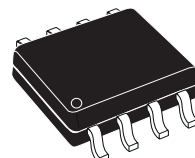
Considering a thermal impedance of 20 $^{\circ}C/W$, the maximum junction temperature will be:

$$T_J = T_A + Z_{THJA} \cdot P_{DISS} = 60 + 20 \cdot 3 = 120^{\circ}C$$

Obviously, with pulse durations longer than approximately 10sec the thermal impedance is very close to the thermal resistance (60 $^{\circ}C/W$ to 70 $^{\circ}C/W$).

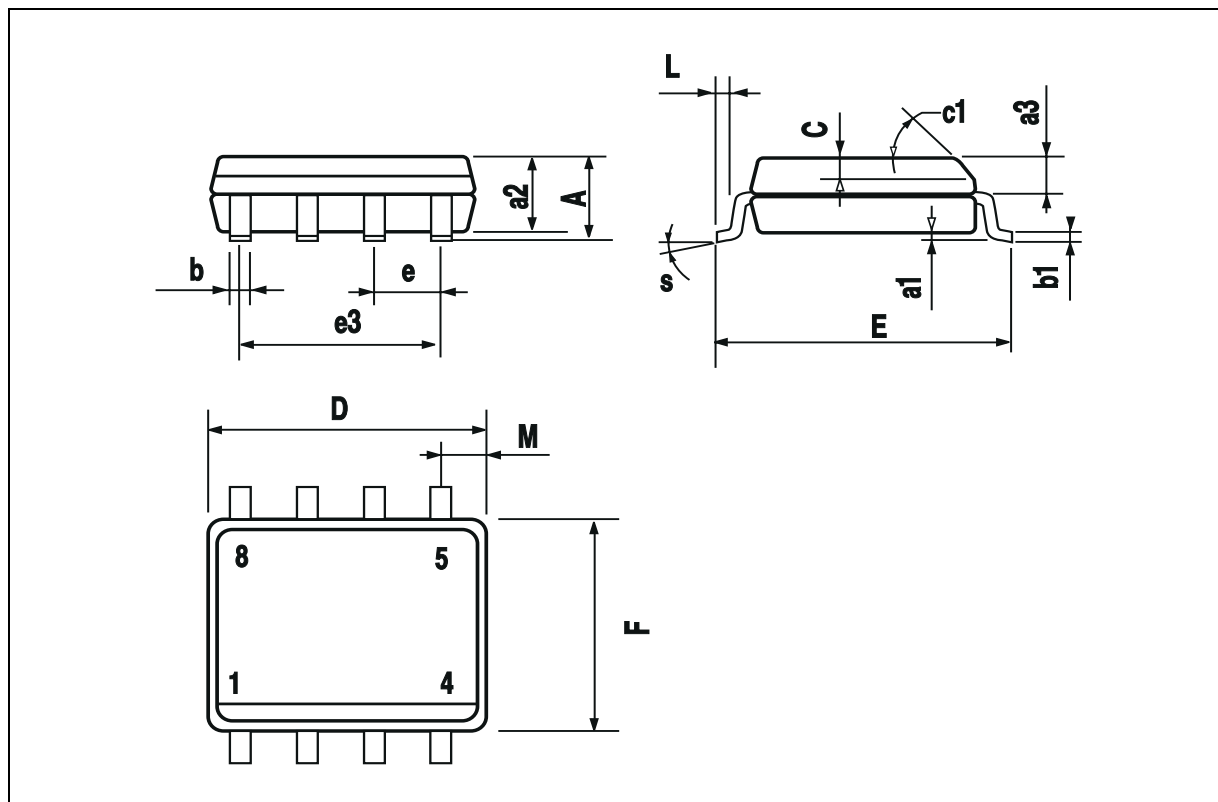
| DIM. | mm | | | inch | | |
|-------|------------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.65 | | | 0.065 |
| a3 | 0.65 | | 0.85 | 0.026 | | 0.033 |
| b | 0.35 | | 0.48 | 0.014 | | 0.019 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.020 |
| c1 | 45° (typ.) | | | | | |
| D (1) | 4.8 | | 5.0 | 0.189 | | 0.197 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F (1) | 3.8 | | 4.0 | 0.15 | | 0.157 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.6 | | | 0.024 |
| S | 8° (max.) | | | | | |

OUTLINE AND MECHANICAL DATA



SO8

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



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