# L7250

## 5V & 12V SPINDLE AND VCM MOTORS DRIVER

**PRODUCT PREVIEW**

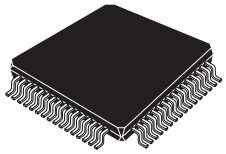
- 12V & 5V (±10%) OPERATION
- REGISTER BASED ARCHITECTURE
- 3 WIRE SERIAL COMMUNICATION INTERFACE UP TO 33 MHZ
- BCD TECHNOLOGY

**Spindle Motor Controller**

- INTERNAL POWER DEVICE 0.9 OHM MAX VALUE @ 125°C (SINK+SOURCE)
- 2.5A PEAK CURRENT CAPABILITY
- ST SMOOTHDRIVE SINUSOIDAL PWM COMMUTATION
- DEDICATED ADC FOR POWER SUPPLY VOLTAGE COMPENSATION
- SPINDLE CURRENT LIMITING VIA FIXED FREQUENCY PWM OF SPINDLE POWER OUTPUTS AT THE SMOOTHDRIVE PWM RATE
- SYNCHRONOUS RECTIFICATION DURING PWM TO REDUCE POWER DISSIPATION
- CURRENT SENSING VIA EXTERNAL CURRENT SENSE RESISTOR
- INDUCTIVE SENSE POSITION START UP DRIVEN BY µPROCESSOR
- SPINDLE BRAKING DURING POWER DOWN CONDITION

**Voice Coil Motor Driver with Ramp Load/Unload**

- INTERNAL POWER DEVICE 0.9 OHM MAX VALUE @ 125°C (SINK+SOURCE)
- 2A PEAK CURRENT CAPABILITY
- 15 BIT LINEAR DAC FOR CURRENT COMMAND, WITH INTERNAL REFERENCE VOLTAGE
- SENSE AMPLIFIER GAIN SWITCH
- CLASS AB OUTPUT STAGE WITH ZERO DEAD-BAND AND MINIMAL CROSSOVER DISTORTION
- RAMP LOAD AND UNLOAD CAPABILITY AS WELL AS CONSTANT VOLTAGE RETRACT
- EXTERNAL CURRENT SENSE RESISTOR IN SERIES WITH MOTOR.
- HIGH CMRR (>70DB) AND PSRR (>60DB) SENSE AMP
- EXTERNAL CURRENT CONTROL LOOP COMPENSATION
- HIGH BANDWIDTH VCM CURRENT CONTROL LOOP CAPABILITY
- HIGH PSRR, LOW OFFSET, LOW DRIFT GM LOOP



**TQFP64**
**ORDERING NUMBER: L7250**

- VCM VOLTAGE MODE, CONTROLLED BY VCM DAC
- GM LOOP OFFSET CALIBRATION SCHEME INCLUDES A COMPARATOR ON THE ERROR AMP

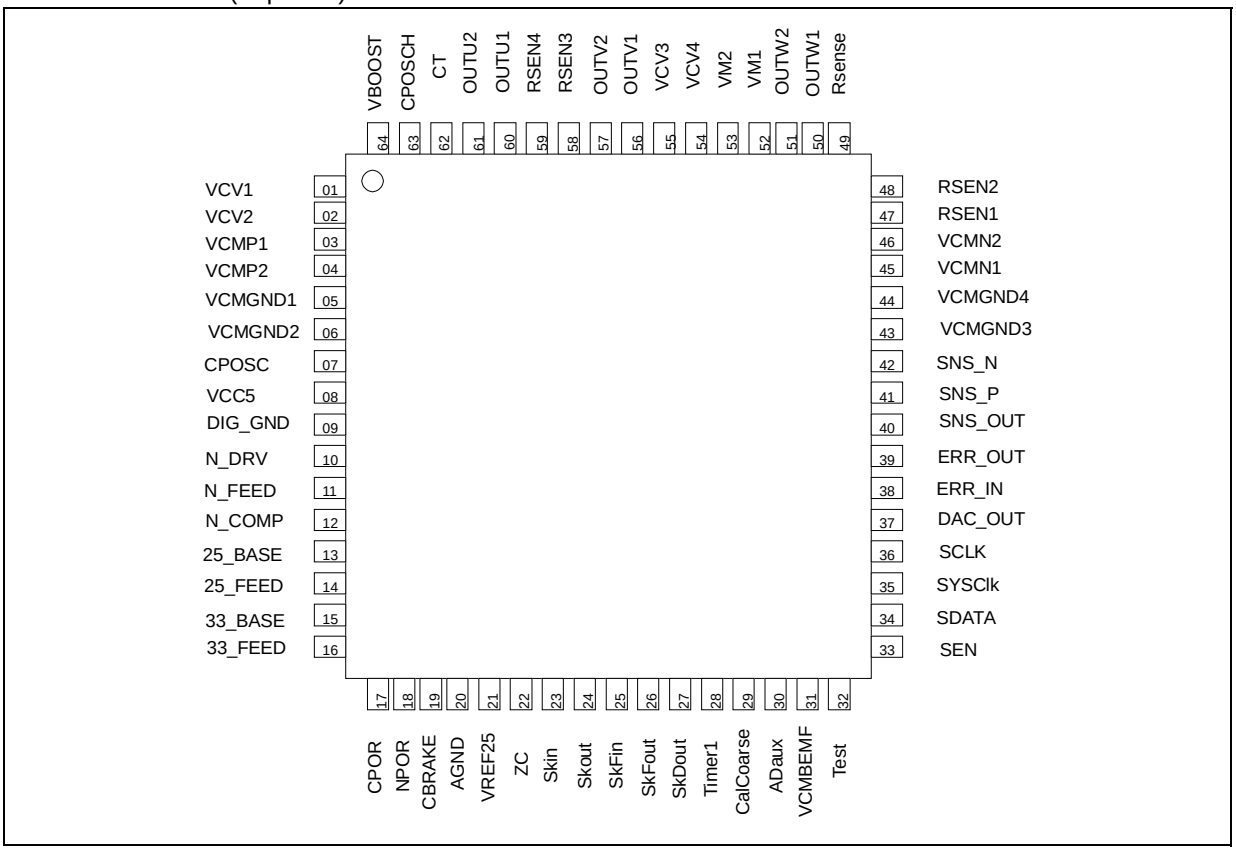
**Auxiliary Functions**

- 3.3V AND 1.8V LINEAR REGULATOR CONTROLLER
- NEGATIVE VOLTAGE REGULATOR
- INTERNAL ISOFET 0.1 OHM @125C
- POWER MONITOR OF 12V, 5V, 3.3V AND 1.8V
- SHOCK SENSOR CIRCUIT TAKES INPUTS FROM PIEZO OR CHARGING ELEMENT
- 10 BIT ADC WITH 4 MUXED INPUTS
- THERMAL SENSE CIRCUIT AND OVER TEMPERATURE SHUT DOWN
- CHARGE PUMP BOOST VOLTAGE GENERATOR FOR HIGH SIDE GATE DRIVE
- ANALOG PINS AVAILABLE TO ENTER SIGNALS TO BE CONVERTED BY THE INTERNAL ADC

**DESCRIPTION**

L7250 is a power IC for driving the SPINDLE and VCM motors, suitable for 5V & 12V application. The spindle system includes integrated power FETs which are driven using ST's Smoothdrive pseudo-sinusoidal commutation technology. The voice coil motor (VCM) system includes integrated power FETs, as well as ramp load and unload capability. Linear 3.3V and1.8V voltage regulators are included, as well as a negative regulator.
Power monitoring of VCC5, VCC12, and of the two positive voltage regulators is also included.L7250 uses a 3 wire serial interface: S_DATA, S_CLK and S_ENABLE

**PIN CONNECTION** (Top view)




**PIN DESCRIPTION**

| N° | Pin | V | Description |
|---|---|---|---|
| 1 | VCV1 | S12 | 12V power supply |
| 2 | VCV2 | S12 | 12V power supply and POR sensing threshold |
| 3 | VCMP1 | O12 | VCM positive output |
| 4 | VCMP2 | O12 | VCM positive output |
| 5 | VCMGND1 | gnd | VCM power ground |
| 6 | VCMGND2 | gnd | VCM power ground |
| 7 | CPOSC | O12 | Charge pump oscillator |
| 8 | VCC5 | S5 | 5V power supply |
| 9 | DIG_GND | gnd | Digital & Switching regulator ground |
| 10 | N_DRV | O5 | Neg Reg ext FET gate driver |
| 11 | N_FEED | I5 | Neg Reg feedback |
| 12 | N_COMP | IO5 | Neg Reg error output |

**PIN DESCRIPTION** (continued)

| N° | Pin | V | Description |
|---|---|---|---|
| 13 | 25_BASE | O5 | Reg 1.8V ext NPN base |
| 14 | 25_FEED | I5 | Reg 1.8V feedback |
| 15 | 33_BASE | O5 | Reg 3.3V ext NPN base |
| 16 | 33_FEED | IO5 | Reg 3.3 V feedback |
| 17 | CPOR | IO5 | POR delay capacitor |
| 18 | NPOR | O5 | POR output signal |
| 19 | CBRAKE | IO5 | Spindle brake capacitor |
| 20 | AGND | gnd | analog gnd |
| 21 | VREF25 | IO5 | 2.5V reference |
| 22 | ZC | O5 | Spindle zero crossing |
| 23 | Skin | I5 | Shock sensor input |
| 24 | Skout | O5 | Shock sensor 1st opamp output |
| 25 | SkFin | I5 | Shock sensor filter input |
| 26 | SkFout | O5 | Shock sensor filter output |
| 27 | SkDout | O5 | Shock sensor output |
| 28 | Timer1 | IO5 | Timer 1 for unload procedure |
| 29 | CalCoarse | I5 | VCM BEMF coarse calibration |
| 30 | ADaux | I5 | auxiliary input for the ADC |
| 31 | VCMBEMF | O5 | VCM BEMF processor output |
| 32 | Test | IO5 | used for testing porpouse (*) |
| 33 | SEN | I5 | Serial enable |
| 34 | SDATA | IO5 | Serial data |
| 35 | SYSClk | I5 | System clock |
| 36 | SCLK | I5 | Serial clock |
| 37 | DAC_OUT | O5 | VCM DAC output |
| 38 | ERR_IN | I5 | VCM error opamp input |
| 39 | ERR_OUT | O5 | VCM error opamp output |
| 40 | SNS_OUT | O5 | VCM sense opamp output |
| 41 | SNS_P | I12 | VCM sense opamp positive input |
| 42 | SNS_N | I12 | VCM sense opamp negative input |
| 43 | VCMGND3 | gnd | VCM power ground |

**PIN DESCRIPTION** (continued)

| N° | Pin | V | Description |
|---|---|---|---|
| 44 | VCMGND4 | gnd | VCM power ground |
| 45 | VCMN1 | O12 | VCM negative output |
| 46 | VCMN2 | O12 | VCM negative output |
| 47 | RSEN1 | O12 | Spindle power sensing resitor |
| 48 | RSEN2 | O12 | Spindle power sensing resitor |
| 49 | Rsense | I5 | Spindle sensing resistor input |
| 50 | OUTW1 | O12 | Spindle phase C output |
| 51 | OUTW2 | O12 | Spindle phase C output |
| 52 | VM1 | IO12 | Vmotor |
| 53 | VM2 | IO12 | Vmotor |
| 54 | VCV4 | S12 | 12V power supply |
| 55 | VCV3 | S12 | 12V power supply |
| 56 | OUTV1 | O12 | Spindle phase B output |
| 57 | OUTV2 | O12 | Spindle phase B output |
| 58 | RSEN3 | O12 | Spindle power sensing resitor |
| 59 | RSEN4 | O12 | Spindle power sensing resitor |
| 60 | OUTU1 | O12 | Spindle phase A output |
| 61 | OUTU2 | O12 | Spindle phase A output |
| 62 | CT | I12 | Spindle central tap |
| 63 | CPOSCH | IO20 | Charge pump diodes connection |
| 64 | VBOOST | IO20 | Charge Pump voltage |

(*) used also to set the IC power supply application. If this pin is pull-up externally the L7250 became a 5V application

S = Supply ; IO = Input/Output ; I = Input ; O = Output ; gnd = Ground.

## ELECTRICAL CHARACTERISTCS

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| | VCV1,VCV2,VCV3,VCV4 | 14 | V |
| | VCC5 maximum voltage | 6 | V |
| | OUTU1,OUTU2,OUTV1,OUTV2,OUTW1,OUTW2<br>VCMP1,VCMP2,VCMN1,VCMN2<br>VM1,VM2 | -1V to 16 | V |
| | Digital Input Voltage | -0.3 to VCC5 | V |
| | Operating free-air temperature | 0 to 70 | °C |
| | Storage Temperature | -55 to 150 | °C |

## ELECTRICAL CHARACTERISTCS

POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **POWER MONITOR, SUPPLY CURRENTS, ETC.** | | | | | | |
| Icc5 | VCC5 Operating current | Spindle and VCM enabled, no load | | 9 | | mA |
| Ivcv | VCV + VRET Operating current | Spindle and VCM enabled, no load | | 44 | | mA |
| CHARGE PUMP VOLTAGE BOOSTER | | | | | | |
| VBOOST | Charge pump output voltage | VCV = 12V<br>Iload = 5mA | | 18.5 | | V |
| VBOOSTfreq | Switching frequency | | | 1 | | MHz |
| **POWER MONITOR** | | | | | | |
| vt5 | VCC5 threshold | | 4.0 | 4.175 | 4.35 | V |
| vt12 | VCC12 threshold | | 9 | 9.5 | 10 | V |
| hv5 | VCC5 hysteresis | | 40 | 100 | 160 | mV |
| hv12 | VCC12 hysteresis | | 100 | 200 | 300 | mV |
| vt33 | V33 Threshold | | 2.7 | 2.8 | 2.9 | V |
| hv33 | V33 Hysteresis | | 20 | 40 | 60 | mV |
| vt18 | V18 Threshold (at pin 25_FEED) | | 1.07 | 1.12 | 1.17 | V |
| hv18 | V18Hysteresis | | 25 | 50 | 75 | mV |
| $NPOR_{low}$ | NPOR low level output voltage | VCV > 4.5V Iol = 5mA | | 0.75 | | V |

**ELECTRICAL CHARACTERISTCS** (continued)
POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $NPOR_{pull}$ | NPOR internal pull_up resistor to V33 | | | 6 | | Kohm |
| $CPOR_{Ic}$ | CPOR charging current | Vout = 0V | | 5 | | uA |
| $CPOR_{low}$ | CPOR low level output voltage | VCV > 4.5V Iol = 1mA | | 50 | | mV |
| Vref25 | 2.5V reference voltage | | -5% | 2.5 | +5% | V |
| **THERMAL WARNING AND THERMAL SHUTDOWN** | | | | | | |
| $T_{warn}$ | Thermal warming temperature | Characterized, tested by correlation. | 130 | 140 | 150 | °C |
| Tsoff | Thermal Shutdown temperature | Characterized, tested by correlation | 150 | 165 | 180 | °C |
| Thys | Thermal Hysteresis | valid for both temperature thresholds | 20 | 25 | 30 | °C |
| **VM ISOLATION FET** | | | | | | |
| IsoR | Rds ON | @ 125°C , I=2.5A | | | 0.1 | Ohm |
| Isol | Continuous current | | | | 2.5 | A |

**SPINDLE DRIVER SECTION**

| | | | | | | |
|---|---|---|---|---|---|---|
| **POWER STAGE** | | | | | | |
| Rds(on) | Total output ON resistance (Source + Sink) | @ 125°C, I=2.5A | | | 0.9 | Ω |
| Idsx | Output leakage current | | | -200 | -500 | µA |
| CTlkg | Centarl tap leakage | | | | 1 | µA |
| DiodeFw | Clamp diode forward voltage | If = 2.5A | 0.6 | | 1.2 | V |
| Slew | Output slew rate | OUTx 10% to 90%<br>Reg04H ‘b7b6b5’ = 011 | | 40 | | V/µS |
| **BACK EMF COMPARATOR** | | | | | | |
| Vie | Common mode input voltage range. | Guaranteed by design | 0 | | VM | V |
| Vr | Input voltage range where output shall not invert. | Guaranteed by design | -1 | | VM+1 | V |
| BEMFoff | BEMF input offset | CT = 6V | -15 | | +15 | mV |
| BEMFhy | BEMF hysteresys | CT = 6V | | 50 | | mV |
| **SPINDLE CURRENT LIMITING** | | | | | | |
| Iin | RSENSE Input bias current. | 0 < Vin < 3.3V | | | 1 | µA |
| CUROff | Comparator offset | | -15 | | +15 | mV |

**ELECTRICAL CHARACTERISTCS** (continued)
POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CURdacr | DAC resolution | | | 3 | | bit |
| $CUR_{dac\_L}$ | DAC output | Reg04H 'b4b3b2' = 000 | | 250 | | mV |
| $CUR_{dac\_H}$ | DAC output | Reg04H 'b4b3b2' = 111 | | 600 | | mV |
| $CUR_{lin}$ | DAC linearity | | -10 | | +10 | mV |
| Cbrake | | | | | | |
| Icbrake | VCbrake leakage | VCbrake=5V | | | 1 | µA |

**VCM SECTION**

| | | | | | | |
|---|---|---|---|---|---|---|
| **CURRENT SENSE AMPLIFIER** | | | | | | |
| Vts | Common mode input voltage range. | GBD - not tested | -0.6 | | VM+1 | V |
| Sns _voff | Input offset voltage | | -12 | | 12 | mV |
| Sns_gain0 | Differential Voltage GAIN0 | Reg09H 'b7' = 0 | -5% | 4.5 | +5% | |
| Sns _gain1 | Differential Voltage GAIN1 | Reg09H 'b7' = 1 | -5% | 16 | +5% | |
| Sns_low<br>Sns_high | VSENSE output saturation voltage | Iload=+/-1mA<br>Vin_diff=+/- 500mV | <br>4.75 | | 250 | mV<br>V |
| sns_slew | Output slew rate | Cload=50pF | 1 | | | V/µs |
| Sns_band | -3dB Bandwidth | Guaranteed by design | 200 | 400 | | kHz |
| sns _cmrr | Common mode rejection ratio | f < 10 KHz, tested at DC only<br>CMRR=$A_{V\ DIFF/AV\ CM}$ | 70 | | | dB |
| sns _svrr | supply voltage rejection ratio VCV | f < 10 KHz, tested at DC only | 60 | | | dB |
| **ERROR SUMMING AMPLIFIER** | | | | | | |
| err _gain | Voltage gain | no load | 60 | | | dB |
| err _band | Unity gain bandwidth | Guaranteed by design | | 4 | | MHz |
| err _slew | Output Slew Rate | Cload=50pF | 1.5 | | | V/µS |
| err _ibias | Input bias current | | | | 1 | µA |
| err _off | Input offset voltage | | -10 | 0 | 10 | mV |
| err_svrr | supply voltage rejection ratio | f < 10 KHz, tested at DC only | 60 | | | dB |
| err _clamp low | Low output (clamp) voltage | Isink = 1 mA, referred to Vref25 | | | TBD | V |

**ELECTRICAL CHARACTERISTCS** (continued)
POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| err _clamp high | High output (clamp) voltage | Isource = 1mA, referred to Vref25 | TBD | | | V |
| **VCM OUTPUT DRIVERS** | | | | | | |
| PWR_Gain | Power amplifier differential gain. | $I_o$ = ±1A, Rload = 8Ω | 14 | 15 | 16 | V/V |
| Rds(on) | Total output ON resistance (Source + Sink) | @ 125°C, I=2A | | | .9 | Ω |
| PWR_Lkg | Output leakage current | | | | 600 | uA |
| DiodeFw | Clamp diode forward voltage | If = 2A | 0.6 | | 1.2 | V |
| THD | Total Harmonic Distortion | characterized no tested | | 1 | | % |
| PWR_Slew | VCMN or VCMP slew rate | $R_L$ = 8 ohms | 1 | | | V/us |
| PWR_Band | Power Amp -3dB Bandwidth | Driving ERROUT = VDACREF, Guaranteed by design | 250 | 500 | | kHz |
| Icross | Static Shoot-through current | Guaranteed by design | | 0 | | mA |
| **VCM CURRENT CONTROL LOOP STATIC AND DYNAMIC CHARACTERISTICS** | | | | | | |
| IVCMoff | Total offset current | Rs=0.2 | -75 | | 75 | mA |
| DIVCMoff | Total offset current drift temperature coefficient | Guaranteed by design | | | .2 | mA/°C |
| Gm_psrr | Gm loop VSRR of VCV | | -1 | | 1 | mA/V |
| **VCM LINEAR DAC** | | | | | | |
| DAC_res | Resolution | | | 15 | | bit |
| DAC_out | Full Scale Output Voltage | wrt VDACREF | 0.96 | 1 | 1.04 | V |
| DAC_off | Mid-Scale Error | wrt VDACREF | -12 | | 12 | mV |
| DAC_DNL | Differential Non linearity | Guaranteed Monotonicity | | | ±1 | LSB |
| DAC_INL | Integral Non Linearity | | | | ±64 | LSB |
| DAC_ConvT | Conversion time | 90% from 3FFFh to 0020h | | | 3 | µs |

**VCM LOAD/UNLOAD**

| | | | | | | |
|---|---|---|---|---|---|---|
| **ADC** | | | | | | |
| ADC_res | resolution | | | 10 | | bit |
| ADC_DNL | Differential Non Linearity | | | | 1 | LSB |
| ADC_INL | Integral Non Linearity | | | | 3 | LSB |
| ADC_ConvT | Conversion time | | | 40 | | ADC Clock cycles |

**ELECTRICAL CHARACTERISTCS** (continued)
POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC AUXILIARY INPUT** | | | | | | |
| AUX_range0 | Input range 0 | Reg06H 'b3' = 0<br>Referred to Vref25 | | ±1 | | V |
| AUX_range1 | Input range 1 | Reg06H 'b3' = 1<br>Referred to Vref25 | | ±2.25 | | V |
| AUX_Ibias | Input bias | | -100 | | 100 | µA |
| **VCM VOLTAGE AMPLIFIER** | | | | | | |
| Volt_gain | Voltage gain | | | 0.165 | | V/V |
| Volt_off | Input offset | | -15 | | +15 | mV |
| Volt_cmrr | Common mode rejection ratio | f < 10 KHz, tested at DC only<br>CMRR=$A_{V\ DIFF/AV\ CM}$ | 46 | | | dB |
| Volt_svrr | supply voltage rejection ratio | f < 10 KHz, tested at DC only | 60 | | | dB |
| **BEMF processor amplifier** | | | | | | |
| CalCoarseIn | Calcoarse voltage input range | | 0.5 | | 2 | V |
| Gain1 | First stage gain | Vcontrol = 1.25 V | | 1.91 | | V/V |
| Gain2 | Second stage gain | | | 16 | | V/V |
| Offset | Residual input offset after calibration | Vcontrol = 1.25V<br>(Measured between VCMN and SNS_P pins) | -3 | | +3 | mV |
| Rout | BEMF amp output resistance (pin 31) | | | 500 | | ohm |
| **ULOAD @ POR** | | | | | | |
| Timer1_V | Timer1 Charging Voltage | | | 2.5 | | V |
| Timer1_I | Timer1 Discharging Current | | | 2 | | µA |
| Timer1_T | Timer1 Low threshold | | | 0.2 | | V |

**VOLTAGE REGULATORS**

| | | | | | | |
|---|---|---|---|---|---|---|
| **1.8 AND 3.3 LINEAR REGULATOR** | | | | | | |
| V18 feed | 1.8V feedback Voltage | | -5% | 1.25 | +5% | V |
| V33 OUT | 3.3V Output Voltage | | -5% | 3.3 | +5% | V |

**ELECTRICAL CHARACTERISTCS** (continued)
POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| V18 IDRIVE V33 IDRIVE | Output base current drive | | | | 15 | mA |
| **NEGATIVE REGULATOR** | | | | | | |
| FREQ0 | Oscillator frequency | Default configuration | | 500 | | KHz |
| FREQ1 | Oscillator frequency | TestRegister = '00001001' or = '00101001' | | 1 | | MHz |
| VoutH | High level output voltage | | TBD | | | V |
| VoutL | Low level output voltage | | | | TBD | V |
| VNEerr OFFS | Feedback input offset | | -10 | | 10 | mV |
| VNEGerr BIAS | Feedback input bias | | | 0 | 1 | µA |
| Vneg_err _cmrr | Common mode rejection ratio | f < 10 KHz, tested at DC only CMRR=$A_{V\ DIFF/AV\ CM}$ | 46 | | | dB |
| Vneg_err _svrr | supply voltage rejection ratio VCV | f < 10 KHz, tested at DC only | 60 | | | dB |

**SHOCK SENSOR**

| | | | | | | |
|---|---|---|---|---|---|---|
| SkIgain0 | Input OPAMP gain0 | Reg02H 'b7' = 0 | | 10 | | V/V |
| SkIgain1 | Input OPAMP gain1 | Reg02H 'b7' = 1 | | 80 | | dB |
| SkIoff | Input OPAMP offset | | -15 | | +15 | mV |
| SkIinput | Input OPAMP input impedance | Reg02H 'b7' = 0 | | 10 | | Mohm |
| SkFgain | Filter OPAMP open loop gain | | | 80 | | DB |
| SkFband | Filter OPAMP unity gain bandwidth | Guaranteed by design | | 5 | | Mhz |
| SkFoff | Filter OPAMP offset voltage | | -10 | | +10 | MV |
| SkOThH0 | Output window comparator VthHigh | Referred to Vref25 ; Reg02H 'b6' = 0 | | 200 | | mV |
| SkOThH1 | Output window comparator VthHigh | Referred to Vref25 ; Reg02H 'b6' = 1 | | 500 | | mV |
| SkOThL0 | Output window comparator VthLow | Referred to Vref25; Reg02H 'b6' = 0 | | 200 | | mV |
| SkOThL1 | Output window comparator VthLow | Referred to Vref25; Reg02H 'b6' = 1 | | 500 | | mV |

**ELECTRICAL CHARACTERISTCS** (continued)
POWER SUPPLY [VCC5 & VCV] VCC5 = 5V ±10%, VCV = 12V ±10%. $T_{amb}$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SERIAL PORT** | | | | | | |
| Voh | Logic Output voltage high | Ioh=1mA | 2.7 | | | V |
| Vol | Logic Output voltage low | Iol=1mA | | | 0.5 | V |
| Vih | Logic input high | Iih=1uA | 2.2 | | | V |
| Vil | Logic input low | Iil=-1uA | | | 0.5 | V |
| Iih | Logic high input current | Internal Pulldown Resistor Vin = 3.3V | | 33 | | µA |
| Iil | Logic low input current | | | | -1.00 | µA |

## 1 SERIAL PORT

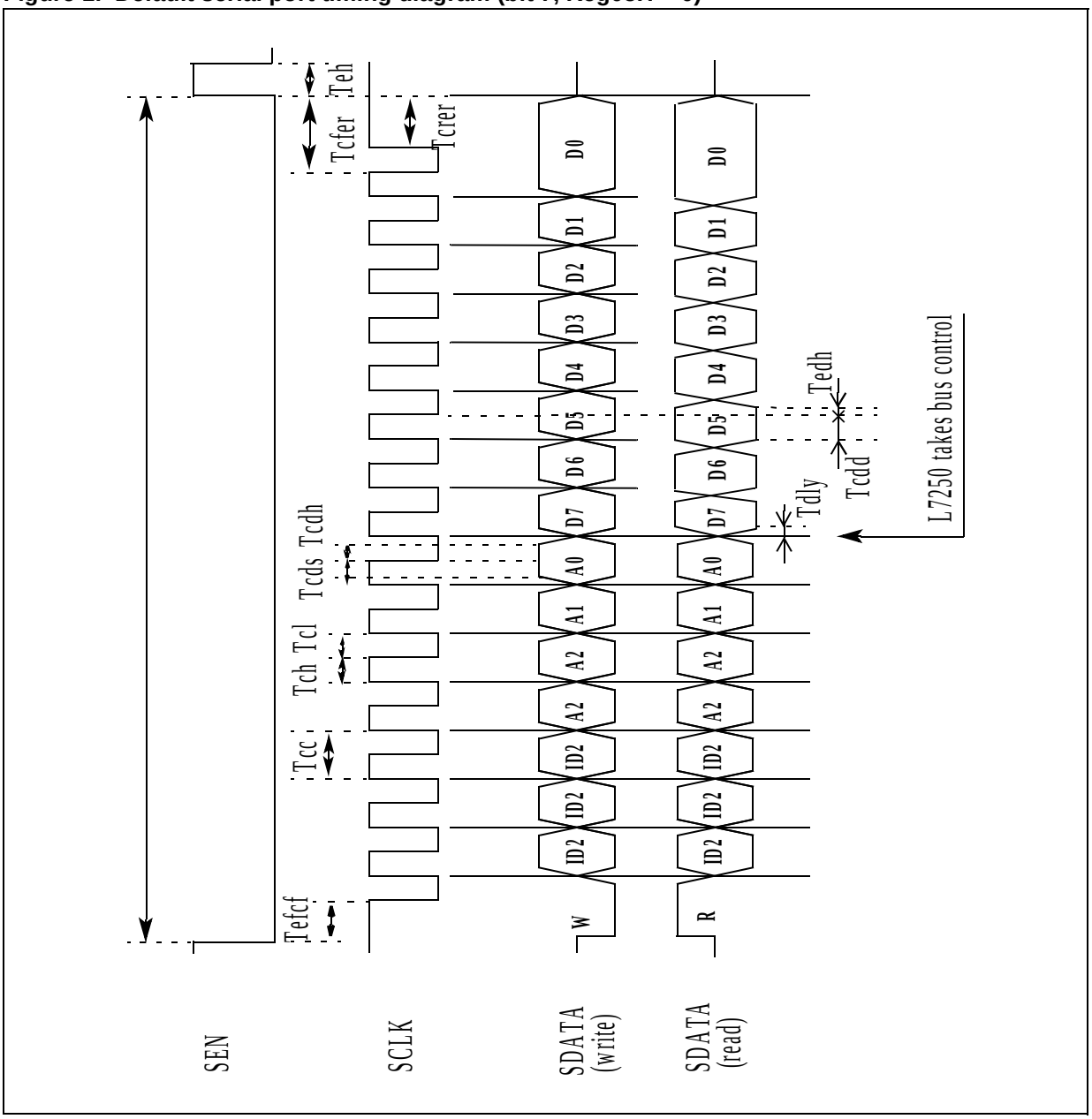
The serial port is a bidirectional three pin interface, using SDATA, SCLK and SEN to address and communicate with sixteen 8 bit registers in the L7250. These registers include the status register, Spindle control registers, VCM control registers, sinewave drive registers, and test mode register. These registers are cleared to zero at power up.

### 1.1 Default comunication modes setting (bit 7, Reg05H ) = 0

After the SEN falling edge, the internal state machine is waiting for the first SCLK falling edge. This means that if the SCLK line starts from an high level the first falling edge, respecting the setup time Tefcf, is considered, and is used to read the R/W bit. During a writing process the internal state machine must see 16 SCLK falling edges to validate the operation. The write mode is started if the R/W bit is low on the first falling edge of SCLK. The read mode is started if the R/W bit is high on the first falling edge of SCLK. The ID, Address, and Data are all then subsequently read by the L7250 on the falling edges of SCLK. (See Figure 1)

The microcontroller has to read the data on the falling edge of the SCLK signal. After the hold time (Tedh) the data line switches to the next data without a tri-state phase.During a read mode the last address bit is read by L7250 on the eighth falling edge of SCLK. The internal state machine then turns the SDATA bit around for the L7250 to assume control at the next SCLK rising edge (the first rising edge after the 8th SCLK falling edge).

**Figure 1. Default serial port timing diagram (bit 7, Reg05H = 0)**




Note1: During writing process L7250 latches the data on the SCLK falling edge (the ASIC is writing on the SCLK rising edge)

Note2: During reading process L7250 takes the bus control on the next SCLK rising edge after the 8th SCLK falling edge

The L7250 write the data on the SCLK falling edge respecting the data hold time (Tedh)

Note3: The ID number for the L7250 is ID1=ID2=ID3=1

### 1.2 Default serial port timing Table

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Tcc | Serial clock period | 30 | | ns |
| Tch | Serial clock high time | 13 | | ns |
| Tcl | Serial clock low time | 13 | | ns |
| Tcds | Serial data setup time to clock falling edge (write mode) | 5 | | ns |
| Tcdh | Serial clock falling edge to serial data hold time (write mode) | 4 | | ns |
| Tedh | Serial clock falling edge to serial data hold time (read mode) | 5 | | ns |
| Tcdd | Serial data setup time to clock falling edge (read mode) | 5 | | ns |
| Tel | Serial Enable low time | 490 | | ns |
| Teh | Serial Enable high time | 30 | | ns |
| Tefcf | Serial Enable falling edge to serial clock falling edge | 17 | | ns |
| Tcfer | Serial clock falling edge to Serial enable rising edge | 17 | | ns |
| Tdly | SDATA turn around delay time | 0 | | ns |

Note 1: All specifications with respect to 50% of signal switching thresholds
Note 2: Reading mode tested at Max 20Mhz

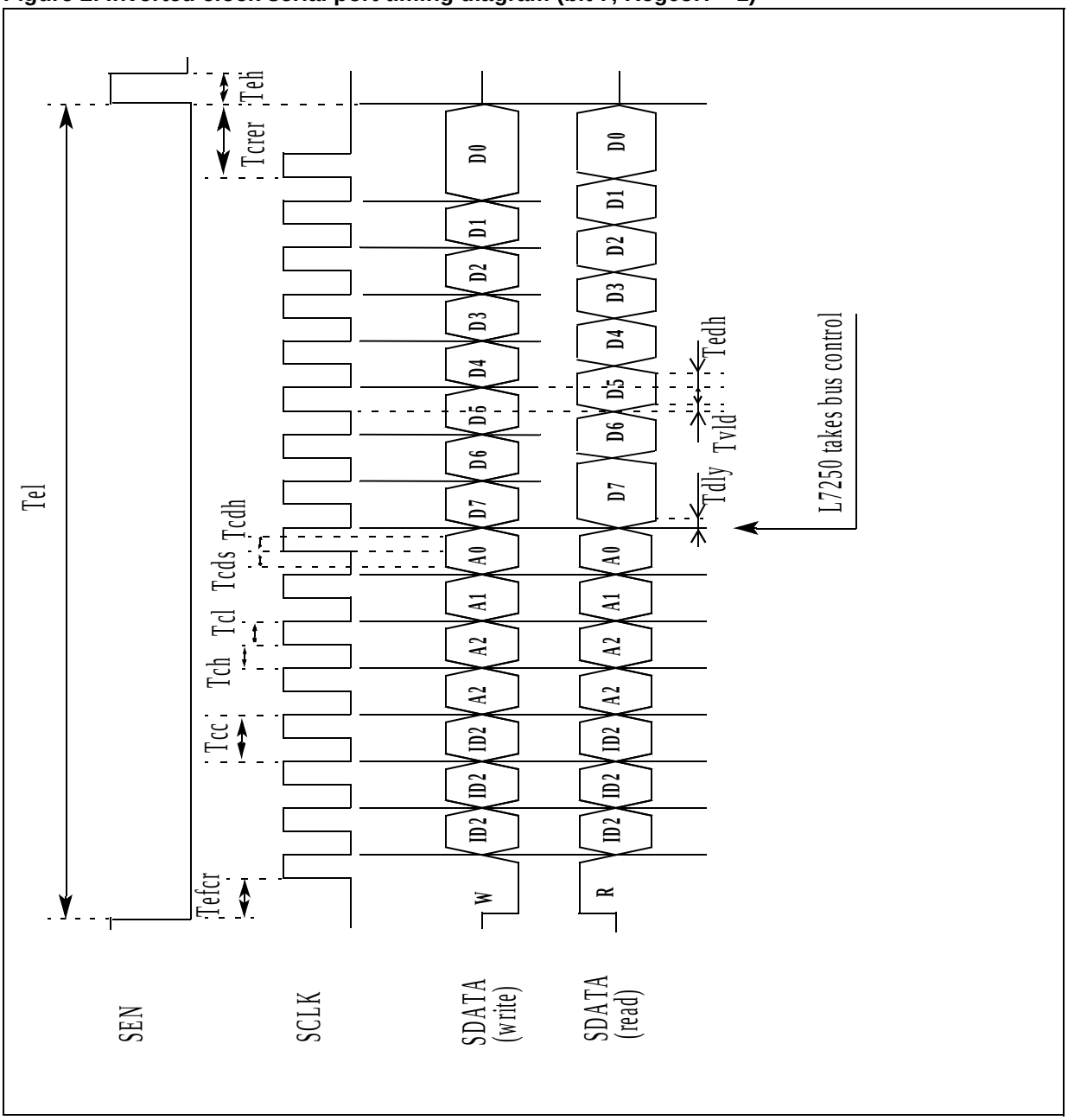
### 1.3 Inverted clock comunication modes (bit 7, Reg05H) = 1

To set the bit7, Reg05H to 1, entering this different comunication mode, a writing process using the default comunication protocol (see the above paragraph) must be used.

After the SEN falling edge, the internal state machine is waiting for the first SCLK rising edge. This means that if the SCLK line starts from a low level the first rising edge, respecting the setup time Tefcr, is considered, and is used to read the R/W bit. The internal state machine must see 16 SCLK rising edges to validate the write operation. The write mode is started if the R/W bit is low on the first rising edge of SCLK. The read mode is started if the R/W bit is high on the first rising edge of SCLK. The ID, Address, and Data are all then subsequently read by the L7250 on the rising edges of SCLK (See Figure 2).

The microcontroller has to read (latch) the data on the falling edge of the SCLK signal. L7250 presents the data on the SCLK rising edge. During a read mode the last address bit is latched by the L7250 on the eighth rising edge of SCLK. The internal state machine then turns the SDATA bit around for the L7250 to assume control at the next SCLK falling edge (the first falling edge after the 8th SCLK rising edge).

**Figure 2. Inverted clock serial port timing diagram (bit 7, Reg05H = 1)**




Note1: During writing process L7250 latches the data on the SCLK rising edge (the ASIC is writing on the SCLK falling edge)

Note2: During reading process L7250 takes the bus control on the next SCLK falling edge after the 8th SCLKrising edge

The L7250 write the data on the SCLK rising edge and it is expecting the ASIC to latches the data on the SCLK falling edge

Note3: The ID number for the L7250 is ID1=ID2=ID3=1

### 1.4 Inverted clock serial port timing Table

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Tcc | Serial clock period | 30 | | ns |
| Tch | Serial clock high time | 13 | | ns |
| Tcl | Serial clock low time | 13 | | ns |
| Tcds | Serial data setup time to clock falling edge (write mode) | 5 | | ns |
| Tcdh | Serial clock falling edge to serial data hold time (write mode) | 4 | | ns |
| Tedh | Serial clock falling edge to serial data hold time (read mode) | 5 | | ns |
| Tvld | Serial clock rising edge to SDATA stable time (read mode)<br>Cload=5pF (see Note2)<br>Cload=50pF (see Note2) | | <br>11<br>15 | <br>ns<br>ns |
| Tel | Serial Enable low time | 490 | | ns |
| Teh | Serial Enable high time | 30 | | ns |
| Tefcr | Serial Enable falling edge to serial clock rising edge | 17 | | ns |
| Tcrer | Serial clock rising edge to Serial enable rising edge | 17 | | ns |
| Tdly | SDATA turn around delay time | 0 | | ns |

Note 1: All specifications with respect to 50% of signal switching thresholds
Note 2: In reading mode the clock frequency is limited by this parameter;
in fact the min 'serial clock high time' is defined by (Tvld+Tasu)
where Tasu = min ASIC setup time

## Table 1. Register Map

| addr | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | name | mnemonic | attributes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00H | SPNCurrSign | VCMcalOut | ZCBad | ThShutdown | ThWarn | rev2 | rev1 | rev0 | SR | status | readonly |
| 01H | RLvoltage1[1] | RLvoltage1[0] | RLvoltage2[1] | RLvoltage2[0] | Rltimer[2] | Rltimer[1] | Rltimer[0] | NoBrake | VCM1 | VCM RLreg | read/write |
| 02H | ShockConf | ShockTh[0] | RLToffBrake[1] | RLToffBrake[0] | Rlcalib[3] | Rlcalib[2] | Rlcalib[1] | Rlcalib[0] | VCM2 | VCMRL reg | read/write |
| 03H | BemfOffCal | VCMState2 | VCMState1 | VCMState0 | SPstate3 | SPstate2 | SPstate1 | SPstate0 | CTR1 | SP&VCMstate | read/write |
| 04H | SPslew2 | SPslew1 | SPslew0 | Curdac2 | Curdac1 | Curdac0 | PWMmask1 | PWMmask0 | CTR2 | control | read/write |
| 05H | SPlprot | m3 | m2 | m1 | m0 | TSDen | VnegEn | Sken | CTR3 | control | read/write |
| 06H | w4 | w3 | w2 | w1 | w0 | PREADC(1) | PREADC(0) | PREsmo | CTR4 | control | read/write |
| 07H | LoadCP | Advance | FFWEn | TO4 | TO3 | TO2 | TO1 | TO0 | CTR5 | control | read/write |
| 08H | Kv7 | Kv6 | Kv5 | Kv4 | Kv3 | Kv2 | Kv1 | Kv0 | KVR | Kval | read/write |
| 09H | GainSwitch | dac14 | dac13 | dac12 | dac11 | dac10 | dac9 | dac8 | DAR1 | DAC reg 1 | read/write |
| 0AH | dac7 | dac6 | dac5 | dac4 | dac3 | dac2 | dac1 | dac0 | DAR2 | DAC reg 2 | read/write |
| 0BH | ADC_DATA(9) | ADC_DATA(8) | ADC_DATA(7) | ADC_DATA(6) | ADC_DATA(5) | ADC_DATA(4) | ADC_DATA(3) | ADC_DATA(2) | ADR | ADC reg | readonly |
| 0CH | ADC_DATA(1) | ADC_DATA(0) | ADC_RES_ADDR(1) | ADC_RES_ADDR(0) | ADCRange | ADC_CH_ADDR(1) | ADC_CH_ADDR(0) | ADC_START | ADR | ADC reg | read/write |
| 0DH | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved | | | read/write |
| 0EH | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved | | | read/write |
| 0FH | test7 | test6 | test5 | test4 | test3 | test2 | test1 | test0 | TEST | test | read/write |

**Table 2. Register map content description** (continued)

| Bit | SPI field name | Content |
|---|---|---|
| **REGISTER SR, ADDRESS: 00H** | | |
| [2:0] | Rev[2:0] | Revision number of the device, set internally |
| [3] | ThWarn | Thermal warning |
| [4] | ThShutdown | Thermal shutdown |
| [5] | ZCbad | Signals a problem with spindle speed loop synchronism |
| [6] | VCMcalOut | VCM error output in calibration mode |
| [7] | SPNCurrSign | Spindle current sign to implement adaptive torque optimizer control |
| **REGISTER VCM1, ADDRESS: 01H** | | |
| [0] | NoBrake | 0=VCM active brake phase enabled<br>1= VCM active brake phase disabled |
| [3:1] | Rltimer[2:0] | 000 = only Unload1 is enabled<br>001 = threshold set to 0.4V<br>010 = threshold set to 0.8V<br>011 = threshold set to 1.2V<br>100 = threshold set to 1.6V<br>101 = threshold set to 2V<br>110 = threshold set to 2.4V<br>111 = only Unload2 is enabled |
| [5:4] | Rlvoltage2[1:0] | Selects between 4 values of unload voltage in Unload2 phase:<br>00 = 1V<br>01 = 1.125V<br>10 = 1.250V<br>11 = 1.375V |
| [7:6] | Rlvoltage1[1:0] | Selects between 4 values of unload voltage in Unload1 phase:<br>00 = 0.375V<br>01 = 0.5V<br>10 = 0.625V<br>11 = 0.75V |
| **REGISTER VCM2, ADDRESS: 02H** | | |
| [3:0] | Rlcalib[3:0] | 0111 = 29.4%<br>0110 = 25.2%<br>0101 = 21%<br>0100 = 16.8%<br>0011 = 12.6%<br>0010 = 8.4%<br>0001 = 4.2%<br>0000 = 0%<br>1111 = -4.2%<br>1110 = -8.4%<br>1101 = -12.6%<br>1100 = -16.8%<br>1011 = -21%<br>1010 = -25.2%<br>1001 = -29.4%<br>1000 = -33.6% |

**Table 2. Register map content description** (continued)

| Bit | SPI field name | Content |
|---|---|---|
| [5:4] | RLToffBrake[1:0] | Selects the duration of Toff (Ton) active brake phase:<br>00 = 300usec<br>01 = 400usec<br>10 = 500usec<br>11 = 600usec |
| [7] | SkockConf | Selects the Shock Sensor application<br>0 = piezo element<br>1 = charging element |
| [6] | SkockTh[0] | Selects the Shock Sensor threshold<br>0 = Vref +/- 200mV<br>1 = Vref +/- 500mV |
| **REGISTER CTR1, ADDRESS: 03H** | | |
| [3:0] | Spstate[3:0] | 0000 = CLCOAST<br>0001 = OLCOAST<br>0010 = OLSIX<br>0011 = OLSIN<br>0100 = OLBRAKE<br>0101 = INDSENSE<br>0110 = CLSIX<br>0111 = CLSIN<br>1000 = CLBRAKE |
| [6:4] | VCMstate[2:0] | Possible states for the VCM:<br>000 = Unload/Retract<br>001 = tri-state<br>010 = brake<br>011 = enable current mode<br>100 = enable voltage mode<br>101 = offset calibration<br>110 = confirm the previous state<br>111 = confirm the previous state |
| [7] | BemfOffCal | VCM BEMF processor offset calibration |
| **REGISTER CTR2, ADDRESS: 04H** | | |
| [1:0] | PWMmask[1:0] | Selects the length of the mask over PWM rising edge:<br>00 = 2 us<br>01 = 4 us<br>10 = 6 us<br>11 = 8 us |
| [4:2] | Currdac[2:0] | Selects the voltage threshold for the spindle current limiter:<br>000 = 250mV<br>001 = 300mV<br>010 = 350mV<br>011 = 400mV<br>100 = 450mV<br>101 = 500mV<br>110 = 550mV<br>111 = 600mV |

**Table 2. Register map content description** (continued)

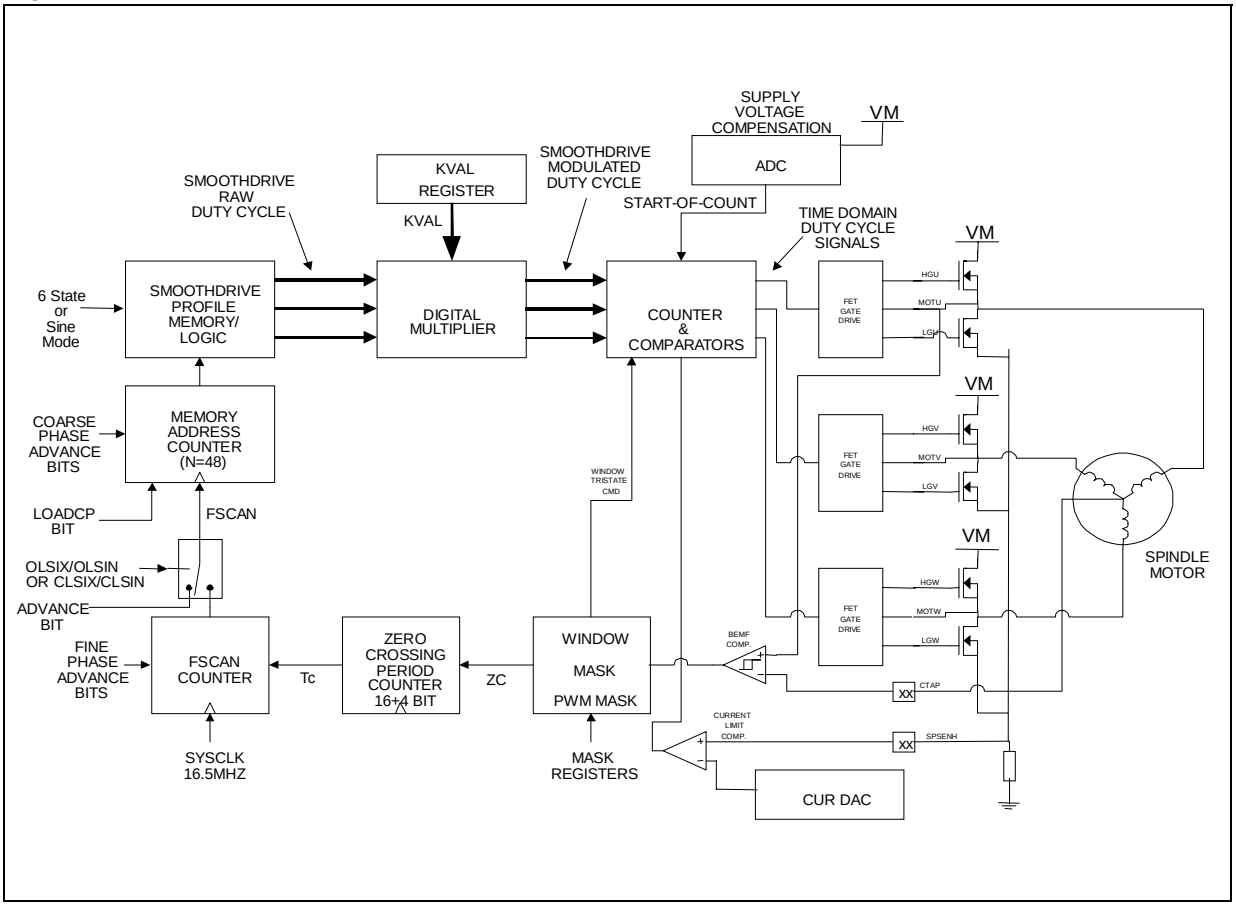
| Bit | SPI field name | Content |
|---|---|---|
| [7:5] | Spslew[2:0] | 000 = 10 V/us<br>001 = 20 V/us<br>010 = 30 V/us<br>011 = 40 V/us<br>100 = 50 V/us<br>101 = 60 V/us<br>110 = 70 V/us<br>111 = 80 V/us |
| **REGISTER CTR3, ADDRESS: 05H** | | |
| [0] | Sken | 0 = shock sensor output no latched<br>1 = shock sensor output latched (to clear the latched information a transition 1 -> 0 -> 1 is necessary) |
| [1] | Vnegen | 0 = negative regulator disabled<br>1 = negative regulator enabled |
| [2] | TSDen | 0 = thermal shutdown disabled<br>1 = thermal shutdown enabled |
| [6:3] | M[3:0] | masking while sensing ZC, expressed in terms of half samples after window opening<br>In terms of electrical degrees the single mask step is 3.75. |
| [7] | SPIprot | 0 = default protocol<br>1 = inverted SCLK protocol |
| **REGISTER CTR4, ADDRESS: 06H** | | |
| [0] | PREsmo | 0 = spindle clock is system clock divided by two (FFWDADC clock is system clock divided by 8)<br>1 = spindle clock is system clock (FFWDADC clock is system clock divided by 4) |
| [2:1] | PREADC[1:0] | 00 = sleep mode<br>01 = ADC clock is system clock divide by 4<br>10 = ADC clock is system clock divide by 2<br>11 = ADC clock is system clock |
| [7:3] | W[4:0] | Windowing while sensing ZC, expressed in terms of half samples before TO value<br>In terms of electrical degrees the single window step is 3.75. |
| **REGISTER CTR5, ADDRESS: 07H** | | |
| [4:0] | TO[4:0] | Coarse and fine section of phase shift, applied for torque optimization.<br>In terms of electrical degrees the Torque Optimizer single step is 0.937 electrical degrees. |
| [5] | FFWEn | 0 = power supply compensation for spindle disabled<br>1 = power supply compensation for spindle enabled |
| [6] | Advance | 0->1 increments by one the current sample position |
| [7] | LoadCP | 0->1 enables load of TO value as the current sample position |
| **REGISTER KVR, ADDRESS: 08H** | | |
| [7:0] | Kv[7:0] | KVAL factor for speed loop control |

**Table 2. Register map content description** (continued)

| Bit | SPI field name | Content |
|---|---|---|
| **REGISTER DAR1, ADDRESS: 09H** | | |
| [6:0] | Dac[14:8] | 7 MSB for VCM dac |
| [7] | GainSwitch | 0 = gain voltage of the VCM sense amplifier equal to 4.5 V/V<br>1 = gain voltage of the VCM sense amplifier equal to 16 V/V |
| **REGISTER DAR2, ADDRESS: 0AH** | | |
| [7:0] | Dac[7:0] | 8 LSB for VCM dac |
| **REGISTER ADR, ADDRESS: 0BH** | | |
| [7:0] | ADC_DATA[9:2] | 8 MSB output data from ADC conversion |
| **REGISTER ADR, ADDRESS: 0CH** | | |
| [0] | ADCSTART | 0-> 1 starts a new ADC conversion |
| [2:1] | ADC_CH_ADDR[1:0] | Channel whose conversion is required<br>00 = VCM current sense amplifier output<br>01 = VCM voltage amplifier output<br>10 = VCM BEMF<br>11 = Auxiliary Channel (external pin) |
| [3] | ADCrange | 0 = the 4 signals enter directly (maintaining the proper dynamic range) the ADC block<br>1 = the 4 signals are scaled down to the ADC dynamic range |
| [5:4] | ADC_RES_ADDR[1:0] | Channel whose result conversion is currently present in ADC_DATA |
| **REGISTER ADR, ADDRESS: 0DH** | | |
| 0DH [7:0] | reserved | |
| **REGISTER ADR, ADDRESS: 0EH** | | |
| 0EH [7:0] | reserved | |
| **REGISTER ADR, ADDRESS: 0FH** | | |
| 0FH [7:0] | Test[7:0] | Test register |

## 2 SPINDLE MOTOR CONTROLLER

**Figure 3.**




### 2.1 Spindle Smoothdrive Functionality

L7250 utilizes ST's proprietary Smoothdrive commutation algorithm. Smoothdrive is a voltage mode pseudo-sinusoidal spindle drive scheme where the duty cycles of the three windings are modulated to form sinusoidal voltages across each winding. The system determines the shape and amplitude of the driving voltages in a completely digital manner.

### 2.2 SYSCLK

The Smoothdrive system clock comes through the SYSCLK pin.

The system expects either 33MHz or 16.5MHz on this pin, and needs 16.5MHz internally. A SYSCLK divide by two can be enabled by a SPI register bit PRESMO to accomodate a 33MHz external clock.

### 2.3 Smoothdrive Wave shape

The basic Smooth drive wave shape is stored in digital memory. A voltage profile designed to reduce switching losses and increase the voltage headroom has been implemented. Essentially, two phases are PWM'ed, while the low side driver of the third phase is on at 100% duty cycle. The PWM duty cycles are modulated in such a way as to result in sinusoidal currents on all 3 motor phases. Driving in this manner, as opposed to driving true sinusoids on all three phases, results in improved headroom and efficiency, approaching that of conventional 6 state commutation.

The system is phase locked to the motor by sensing one BEMF zero crossing on one winding, once per electrical

cycle. A window is opened up in that winding, and it is tri-stated to allow sensing of the zero crossing. The width of the window opening is programmable, and can be made very small in steady state. A frequency locked loop keeps the wave shape in sync with the motor speed. The system is entirely digital, requiring no external components.

The Smoothdrive wave shape is sync with the motor. It divides the electrical period, from one zero crossing to the next, into 48 evenly spaced sample periods. For each sample period, the driving duty cycle is defined for each motor phase by a table in the Smoothdrive logic. The Memory Address Counter sequences the samples through the cycle, and is clocked N times per cycle. The following describes how the frequency locked loop system works:

There are N sine wave samples per electrical rev. N=48 for this design.

Each electrical period (from one ZC to the next) is measured by a timer with an effective frequency of Fsysclk/48, resulting in a measured zero crossing period Tc. The timer does not actually run at Fsysclk/48 - the resolution is more like Fsysclk/3.

The FSCAN Counter is a down counter preloaded with Tc, and running at Fsysclk. The FSCAN Counter puts out a pulse each time it hits zero, then it resets to Tc and counts down again. This cycle occurs N (48) times per electrical cycle. Thus, the FSCAN Counter divides the electrical cycle into N evenly spaced samples based on the previous Tc. The pulse signal out of this block, that occurs 48 times per electrical period, is called FSCAN.

The Memory Address Counter counts FSCAN pulses, and tells the Profile Logic which full scale duty cycle values to use for each Smoothdrive sample period.

### 2.4 PWM rate

The PWM rate is unrelated to the Smoothdrive sample rate. The minimum PWM rate is 32.2kHz with 16.5MHz spindle system clock, defined by (Fsys/512). The spin system clock is SYSCLK or SYSCLK/2, chosen via serial port (SYSCLK/2 is the default at power up). 9 bits of resolution define the duty cycle at each sample period. The PWM counter is reset at the beginning of each electrical cycle (at the ZC).

The PWM duty cycle is defined for each of the two chopping phases by comparing the appropriate duty cycle values to the counter. The duty cycle values are the result of multiplying values in the Smoothdrive waveform table by the amplitude value KVAL coming from SPI.

### 2.5 Supply Voltage Compensation via ADC

The Smoothdrive system is a voltage mode drive scheme. Without compensation, the spindle drive amplitude would be a proportion of the motor supply voltage. L7250 implements a supply voltage compensation scheme whereby the drive amplitude is indipendent on motor supply voltage.

An internal 6 bit ADC reads the motor supply voltage variation (+/-10%), and the applied duty cycle is modified to keep the applied voltage constant. A side effect is that the PWM frequency will be changed as well as the duty cycle.

The ADC runs on a 4MHz clock derived from the SYSCLK (it is divided by 8 if the PRESMO bit is set to zero else it is divided by 4). The conversion results affects the PWM counter once per PWM cycle, nominally 32 kHz.

### 2.6 BEMF comparator Hysteresis

Since only one polarity ZC is detected, the BEMF comparator hysteresis no longer needs to contribute a time offset. The hysteresis is zero on the significant edge, and is engaged on the other edge. Thus, larger values of hysteresis can be used to provide noise immunity at low speed while coasting, without affecting ZC timing.

Hysteresis of 50mV provides adeguate sensitivity for detecting motion startup, while improving noise immunity when the motor is moving very slow or is stationary.

### 2.7 Startup Algorithm Description

L7250's spindle motor startup is controlled by firmware, and consists of four distinct phases: Inductive Position

Sense, to determine rotor position, Open Loop Commutation, which accelerates the motor to build up BEMF, Synchronization , to measure motor speed and position, initializing the Smoothdrive system, and Closed Loop Smoothdrive Commutation, the normal synchronous commutation mode to accelerate and run at speed.

### 2.7.1 Inductive Position Sense

Inductive position sensing is achieved through a firmware routine that measures the current rise time in each of the six possible states (six steps profile), and uses this information to determine the rotor position.

The six steps profile still comes from the Profile Memory that contains 48 samples, but in this case there are only six different configuration, each of them repeated eight times; the linear scansion of the memory one sample at a time gives a new six step configuration every eight increments.

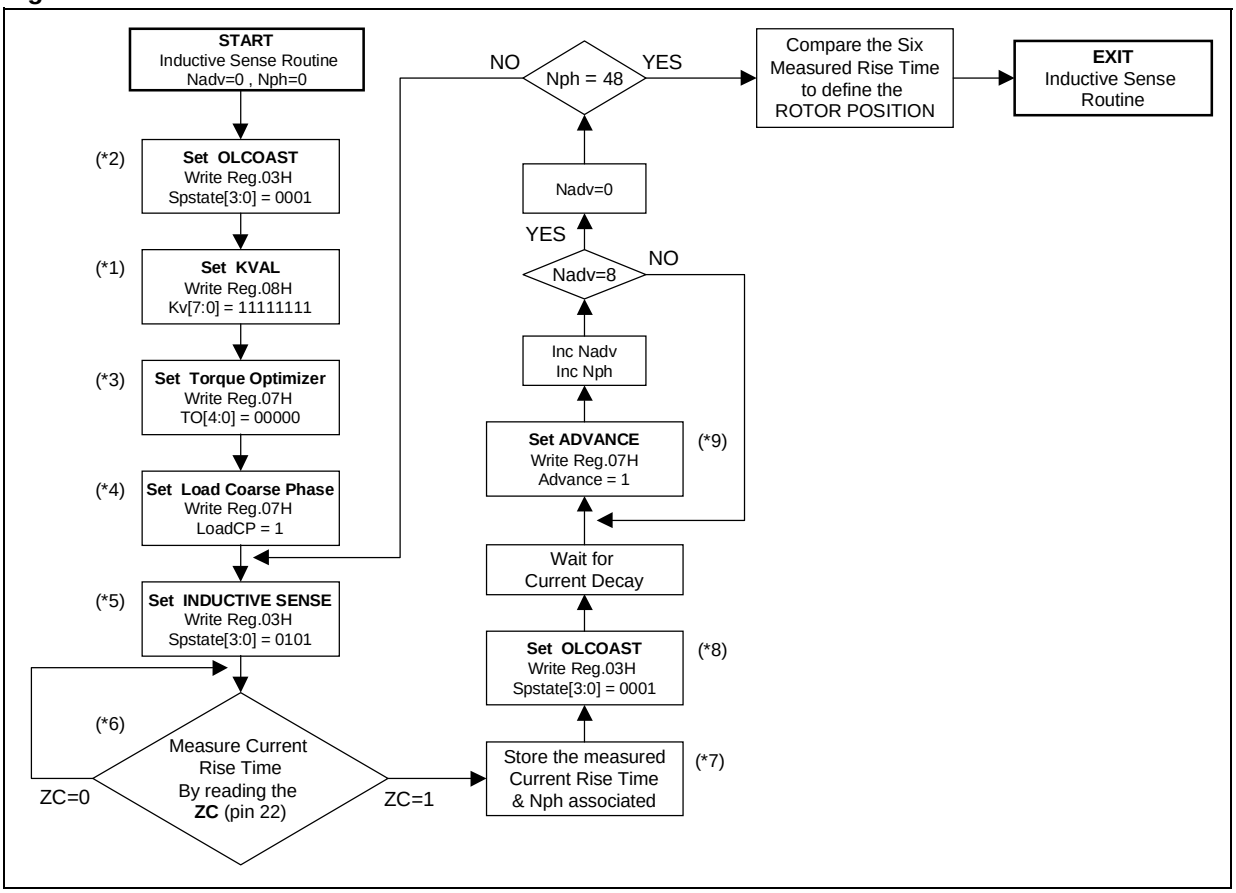
Before any operation can be done, the firmware routine must set the KVAL value present in SPI to the maximum value (*1) , to saturate the PWM signals given to the motor, and put the Memory Address Counter in a known position (*3); this is done keeping the motor in OLCOAST (*2) state and asserting a LoadCP command (*4) to load the content of the torque optimizer related SPI register into the Memory Address Counter.

At this point, the present six steps configuration can be energized through the INDSENSE state (*5) , waiting for the current to reach the threshold programmable via SPI (*6); the current limiting comparator will be triggered by this condition, and it's output will be visible at ZC pad. The current rise time will be measured and stored from the ASIC (*7) .

The device automatically limits the PWM signals for the three phases to limit the current, but the currents in the windings must be recirculated from firmware putting the motor in OLCOAST (*8) state.

A burst of eight ADVANCE signals (*9) must be asserted from SPI to reach the next configuration in the profile memory, then the procedure can be repeated. Each winding can be excited more than one time, to average the measurements, and at the end of the sensing sequence the ASIC decides the rotor position.

**Figure 4. Inductive Sense Routine**

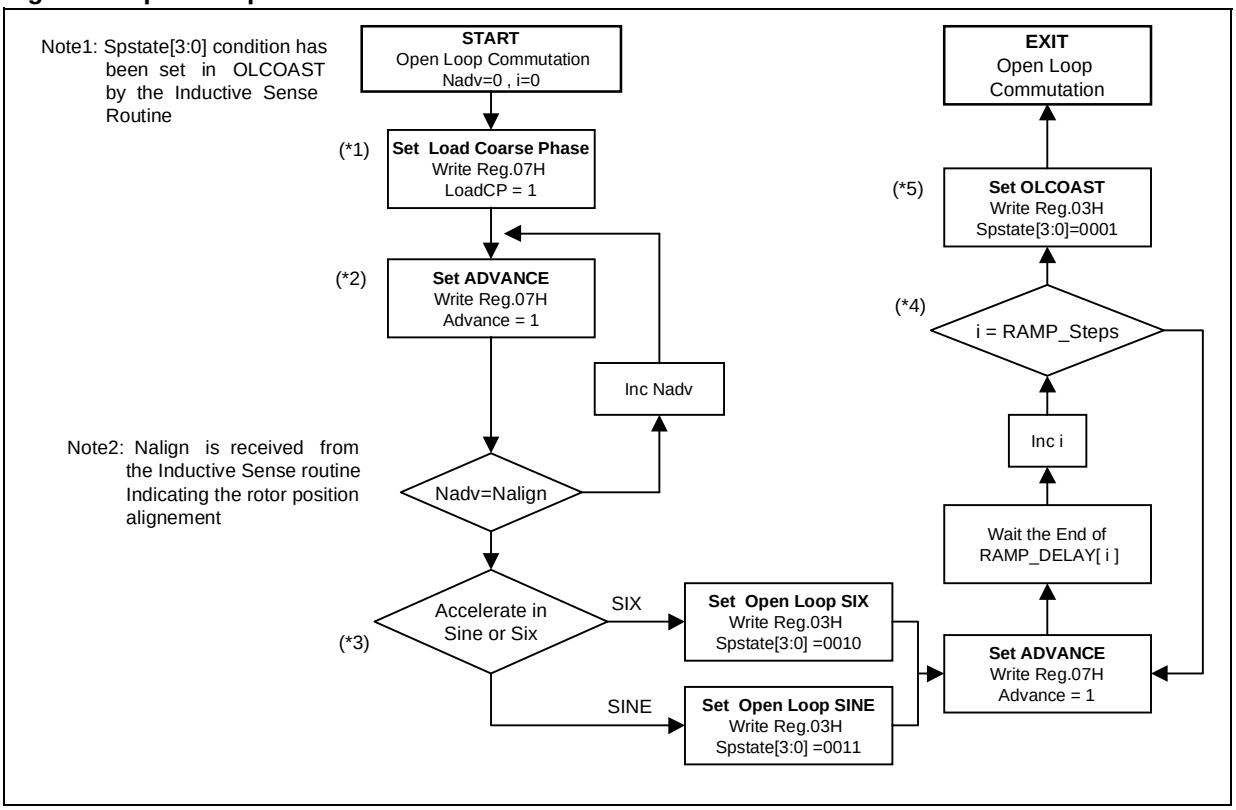


### 2.7.2 Open Loop Commutation

After position sense is complete, the microcontroller commutates the motor following a constant acceleration profile until sufficient BEMF is developed to reliably measure it.

The starting position of the open loop commutation, determined by the position sense routine, is set up by first initializing the Memory Address Counter using LOADCP (*1), then clocking ADVANCE (*2) the appropriate number of times (8 pulses per 6 state position). The spindle state will be OLCOAST while setting the initial state. Then, drivers are enabled in either OL_SIX or OL_SIN modes (*3) , depending on whether 6 state or sine mode open loop commutation is desired. Once the motor is accelerated up to an appropriate speed (*4) , the motor is tri-stated by transitioning to the OLCOAST (*5) and then CLCOAST states, as described below, to synchronize the Smoothdrive system to the motor.

**Figure 5. Open Loop Commutation**




### 2.7.3 Synchronization to Smoothdrive Commutation

When the open loop commutation is complete, the drivers are put in OLCOAST mode, and after a delay for setting the Bemf sampling period, CLCOAST is asserted, so that a ZC Period (Tc, the time between two BEMF zero crossings) can be detected and measured.

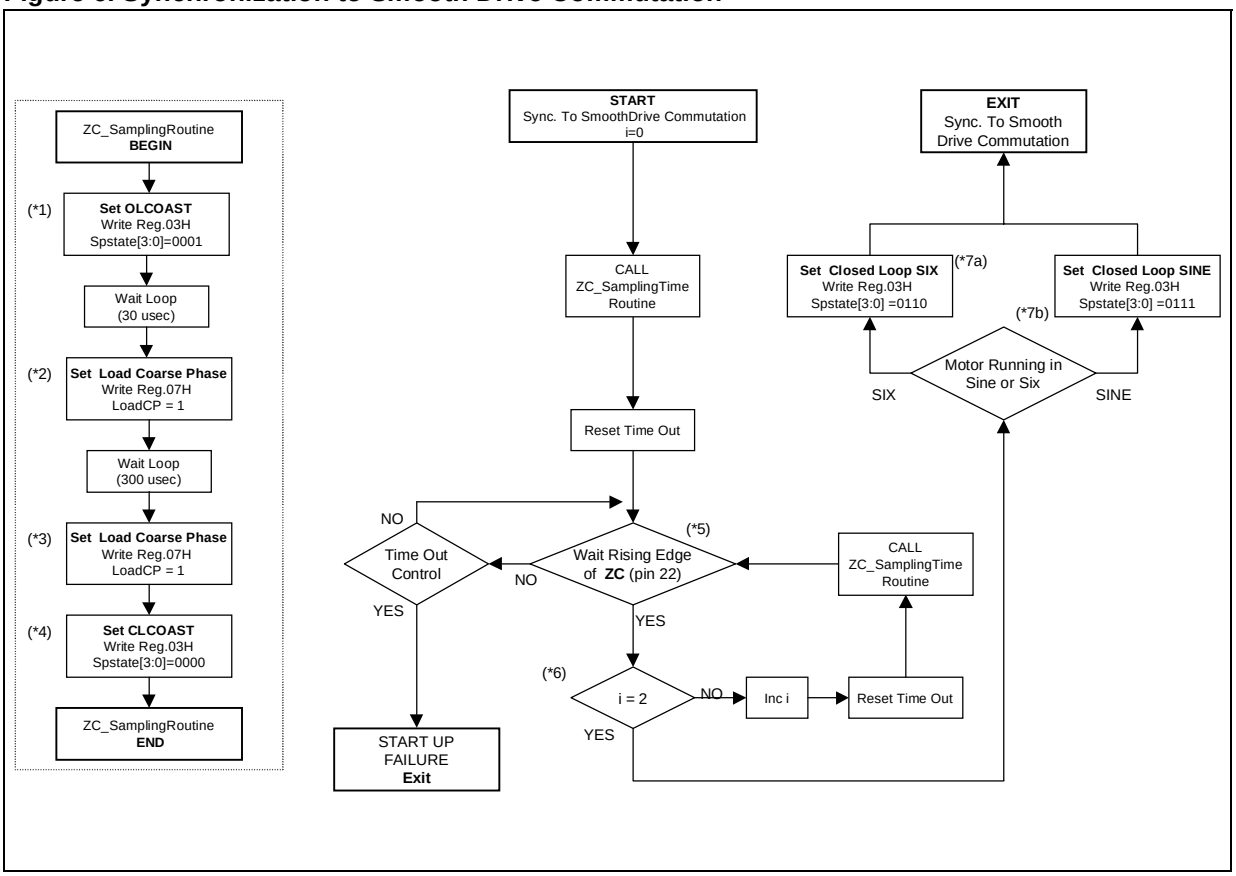
The BEMF sampling period is set in OLCOAST (*1) and after a delay (30 usec ) a Load CP (*2) is asserted. After a delay of time Tc0 (300usec suggested) another Load CP is asserted (*3); this initializes the electrical period for BEMF sampling. Once pregrammed the transition to CLCOAST (*4) , the BEMF is sampled at the rate of Tc0 to look for two consecutive LOW readings (in anticipation of the LOW->HI zero crossing transition (*5) ).

After the first ZC rising edge, the BEMF sampling period is refreshed to Tc0 value.

If two consecutive ZC edges are detected (*6), then after the last rising edge the Smoothdrive commutation is synchronized with the motor rotor position and it is ready to be programmed in closed loop commutation .

At least two ZCs must be observed before transitioning to closed loop spinup (CLSIX or CLSIN) (*7a or *7b) . This ensures that the Smoothdrive circuitry is synchronized to the spindle motor.

**Figure 6. Synchronization to Smooth Drive Commutation**




### 2.7.4 Closed Loop Commutation

During closed loop commutation, the motor is driven following the smooth driver wave shape (or the traditional six step profile). To keep sync, each electrical cycle a winding of the spindle motor (phase U) is tri-stated, for a programmable (via SPI) window (W), to sense for the ZC occurrence; to mask the current flyback time a masking time is applied starting from the opened window for a certain number M of samples (settable via SPI). Due to the fact that the motor winding is driven in voltage mode a control of the phase shift between the applied voltage and the Bemf is required in order to optimize the system efficiency (the loss in efficiency is related to the cosine of the angle between Bemf and current). Via the SPI it is possible to set an appropriate Torque Optimizer (TO) value based on the application characteristics (Rm, Lm, Speed).

When a ZC is detected the circuit starts scanning the stored smooth drive wave shape (or the traditional six step profile) from the number of sample pointed by the TO register; the tri-stated window is opened a certain number of samples before.

In the following table the relation between the TO register contents and the window and masking time position and duration:

| | start | stop |
|---|---|---|
| window | TO-W | At ZC detection |
| mask | TO-W | TO-W+M |

### 2.8 Spindle PWM Current Limiting

Peak motor current is limited with a fixed frequency PWM scheme that works in conjunction with the Smoothdrive PWM rate. When the current limit threshold is reached the motor is put in brake condition, and it is re-enabled at the beginning of the next PWM cycle if the current limiting condition is false.

Spindle current is sensed via an external resistor connected from the low side driver sources to ground. This sense voltage is compared to an internal programmable voltage reference (Reg04H Currdac[2:0]).

There is a built in digital filter, generating a SYSCLK derived delay (20 * SYSCLK period) from the over current event. This delay appears on both edges of the current limiting comparator.

### 2.9 Slew Rate Control

Closed loop Voltage Slew rate control is provided on both edges for the high and low side drivers. The slew rate value can be set with three bits in the serial port (Reg04H Spslew[2:0]). Slew rates up to 80V/us and down to 10V/us will be controllable.

### 2.10 Synchronous rectification

The appropriate low-side driver is enabled during the off-time phase to conduct recirculation current with a lower voltage drop than the low side driver body diode, reducing power losses. Crossover current protection is provided to prevent shoot-through currents.

### 2.11 Open loop and closed loop brake

Spindle braking may be done while keeping the Smoothdrive system in sync with the motor, or not.

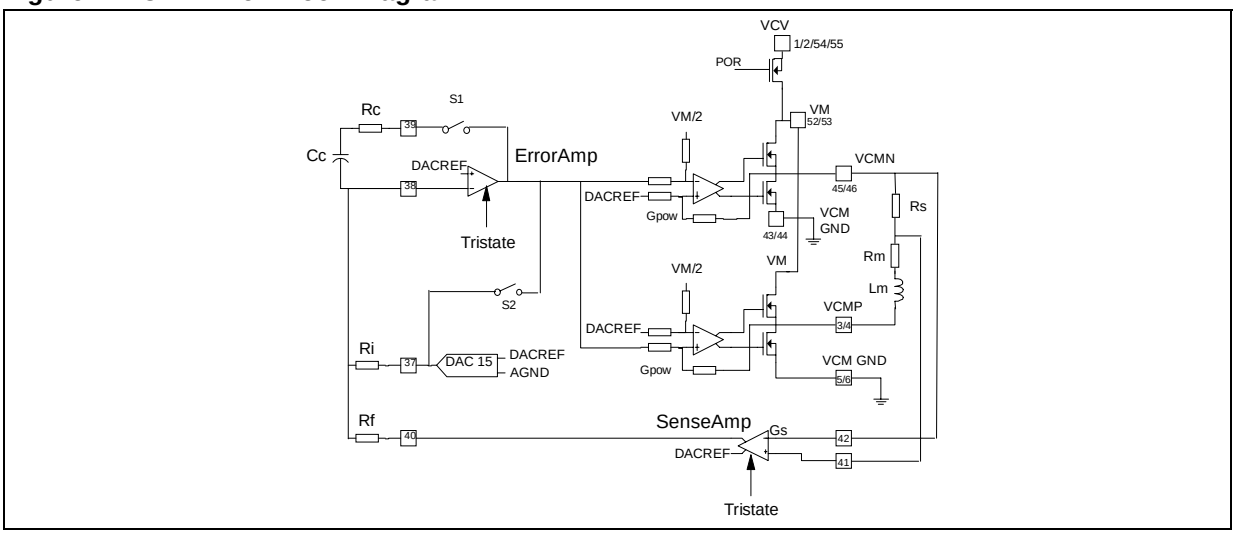
Closed Loop Braking means ZC's are still being detected in the same way as when normally commutating. So, all 3 motor phases are driven low, but when the window is normally opened to look for a ZC, MOTU is tri-stated. When the ZC occurs, MOTU is driven low as the other motor phases, until the next window comes up. A motionless motor will wait for a ZC, keeping MOTU tri-stated and the other two phases low. Open loop braking means that all 3 motor phases are driven low, and ZC's are not detected. Braking caused by a power fault is always open loop braking.

CBRK provides control voltage for brake circuitry after power fails. An external cap on this pin is charged to 5V, so that the cap stays charged after a power failure.

## 3 VOICE COIL MOTOR DRIVER

The VCM driver is configured as a transconductance amp, with an n-channel DMOS H-bridge power output, current sense amp, error amp, and 15 bit linear DAC for command input. The power stage is a class AB voltage amp. The error amp closes the transconductance loop around the power amp, using feedback from the current sense amp. The VCM block is shown below.

**Figure 7. VCM Driver Block Diagram**




The current flowing into the voice coil is equal to:

$$I_{coil} = -\frac{R_f}{R_i} \cdot \frac{1}{R_s \cdot G_s} \cdot V_{in}$$

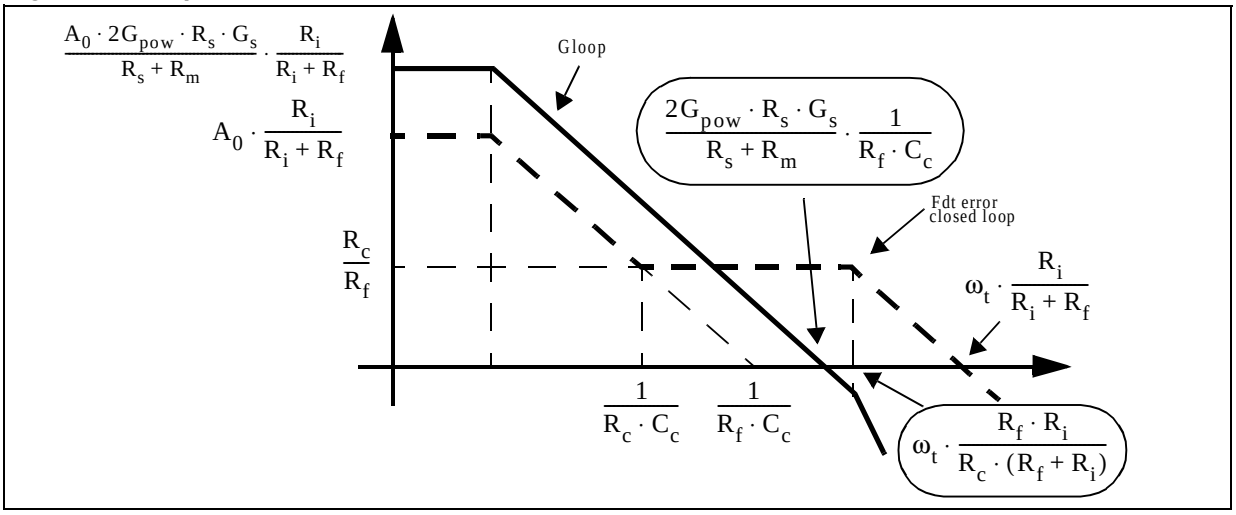
Where $G_S$ is the sensing opamp gain (programmable via serial port

Considering a typical application where Rf = 5.6k, Ri = 2.5k, Rs = 0.25Ω and Gs = 4.5V/V we obtain a maximum current equal to about 2A for 1V DAC output (Vin). The sense amplifier input range is about 0.55V. The power stages assure this current requirement and they have a differential gain of 16.

The loop is compensated through the RC network Rc and Cc that cancels out the motor pole Lm/Rm.

This graphic shows the theoretic Gloop Bode diagram and put in evidence the second pole of the loop that is strictly related to the error amplifier bandwidth.

**Figure 8. Gloop**



Considering a typical application with Rs = 0.25Ω, Lm = 0.75mH, Rm = 7.5Ω, Gs = 4.5 Gpow = 8, Rf = 5.6K, Cc = 3.3nF, Rc = 33k we will obtain a bandwidth about 20kHz. To increase the bandwidth a different values of the external components could be calculated following the above relation and taking in account the limitation introduced by the second pole due to the error amplifier bandwidth (ωt). This one has a typical value about 4MHz.

### 3.1 VCM Operating Modes and Control

At power-on-reset the VCM register is cleared and the VCM is in Unload/Retract mode.
Via serial port is possible to command the following modes: Unload/Retract, Tri-state (disable), Brake, Enable Current Mode, Enable Voltage Mode, Offset Calibration

### 3.2 VCM Power Driver H-Bridge

The VCM driver is capable of high performance linear, class-AB, H-bridge operation with all power devices internal. The power amp stage is configured as a voltage amp with gain of 16. The H-bridge consists of 4 N-channel DMOS power transistors. Power is supplied to the H-bridge through the internal ISO-FET ( at pins VM 52,53), and ground returned via four VCMGND pins (5,6,43,44). Boosted gate drive for the high side drivers is provided by the charge pump circuitry, with the boosted voltage at the VCP pin.

### 3.3 VCM Current Command 15 bit DAC

The VCM current command is defined by an internal linear, 2's complement, 15 bit DAC. The mid scale reference for the DAC, VREF25, is defined by an on-chip reference at 2.5V. VREF25 is the reference for the sense amp and error amp in the VCM loop. Level shifting from VREF25 to VM/2 will be done in the power stage.

0x3FFF Max current flowing from VCMN to VCMP (current mode operation)
0x----
0x0001
0x0000 zero current
0xFFFF
0x----
0x4000 Max current flowing from VCMP to VCMN (current mode operation)

To write the 15 bit DAC the two register REG09H [14:8] and REG0AH [7:0] have to be referred.
At any time the MSB register is entered, to apply the modification also the LSB register must be write. Instead writing only the LSB register its content will be immediatly visible on the DAC structure.
Then a double write sequence its necessary if the [14:8] bit have to be modified while it is possible to move the DAC in a fine way (write of the [7:0] bit) with only one write sequence.

### 3.4 VCM Current Sense Amp

VCM current is sensed by a diff amp that amplifies and level shifts the voltage drop across an external resistor in series with the VCM coil. The sense amp has a nominal differential voltage gain programmable through the serial port bit Reg09H bit 7, and the output, VSENSE, is relative to VREF25 (pin 21). The amp has been design to have high common mode rejection (over 70dB at DC), Power supply rejection over 60dB, and as low an input offset as possible.

### 3.5 VCM Current Loop Error Amplifier

The VCM error amp gains up the difference between the current command voltage DAC_OUT and the current sense voltage VSENSE. VCM current loop compensation is implemented externally with an RC network connected across ERR_IN and ERR_OUT. The error amp output is referred to VREF25.

### 3.6 Error Amp Output Clamp

The error amp output swing is clamped in both directions (Vref25+/-3Vbe) to prevent wind-up of the integrating compensation components around the error amp in the event of saturation.

### 3.6.1 Voltage Mode

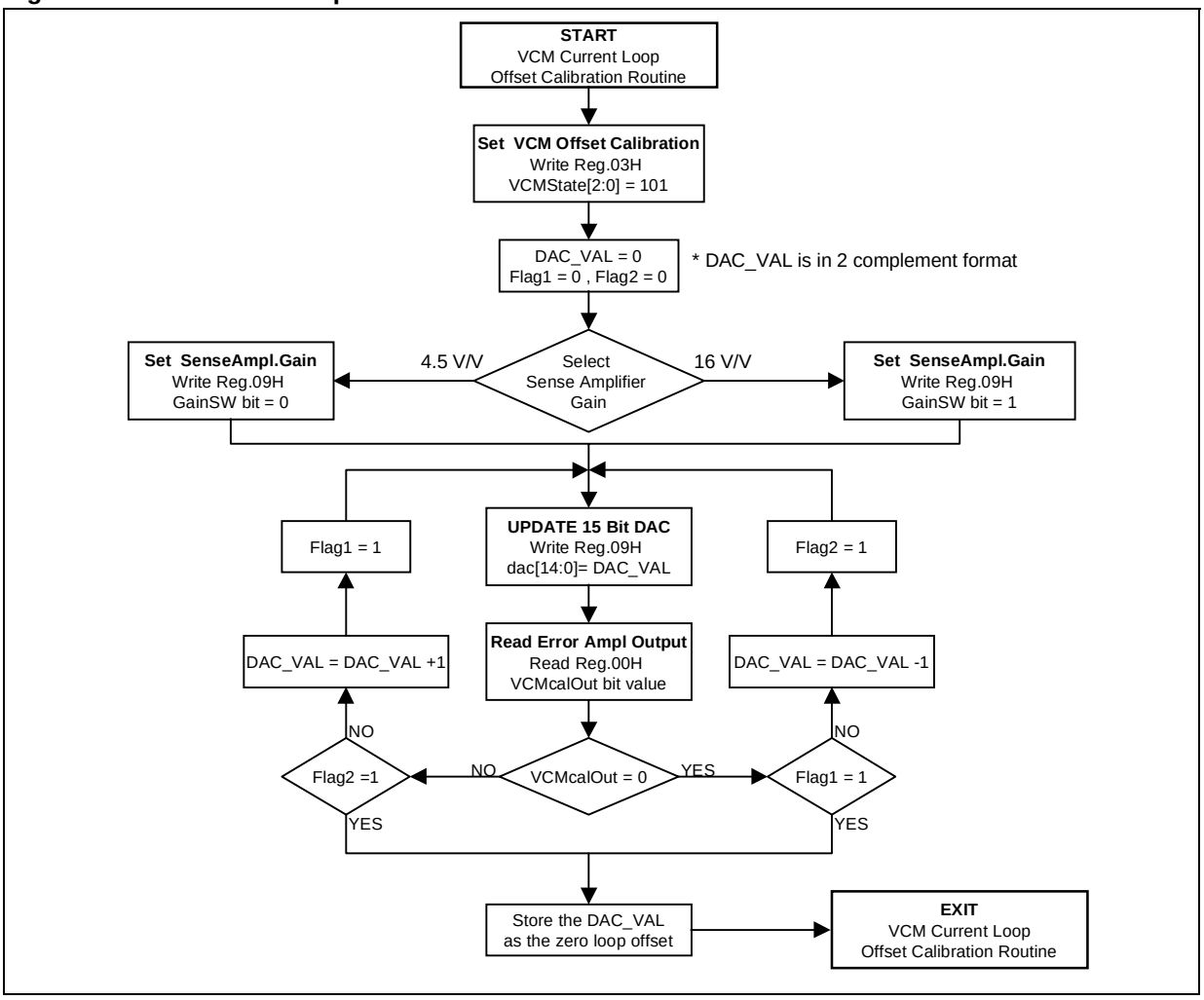
In Voltage Mode, the VCM power outputs will apply a voltage to the VCM motor commanded by the VCM DAC. This is implemented by tristating the sense amp and error amp outputs, and connecting DAC_OUT to ERR_OUT with an internal switch (switch S2). Skipping the err_out amplifier the DAC command will enter the power section without any inversion, then the DAC codification must be considered in opposite direction respect to the current mode operation.

## 3.7 VCM Loop Offset Calibration Mode

The VCM Loop Calibration mode can be implemented following two different approach:

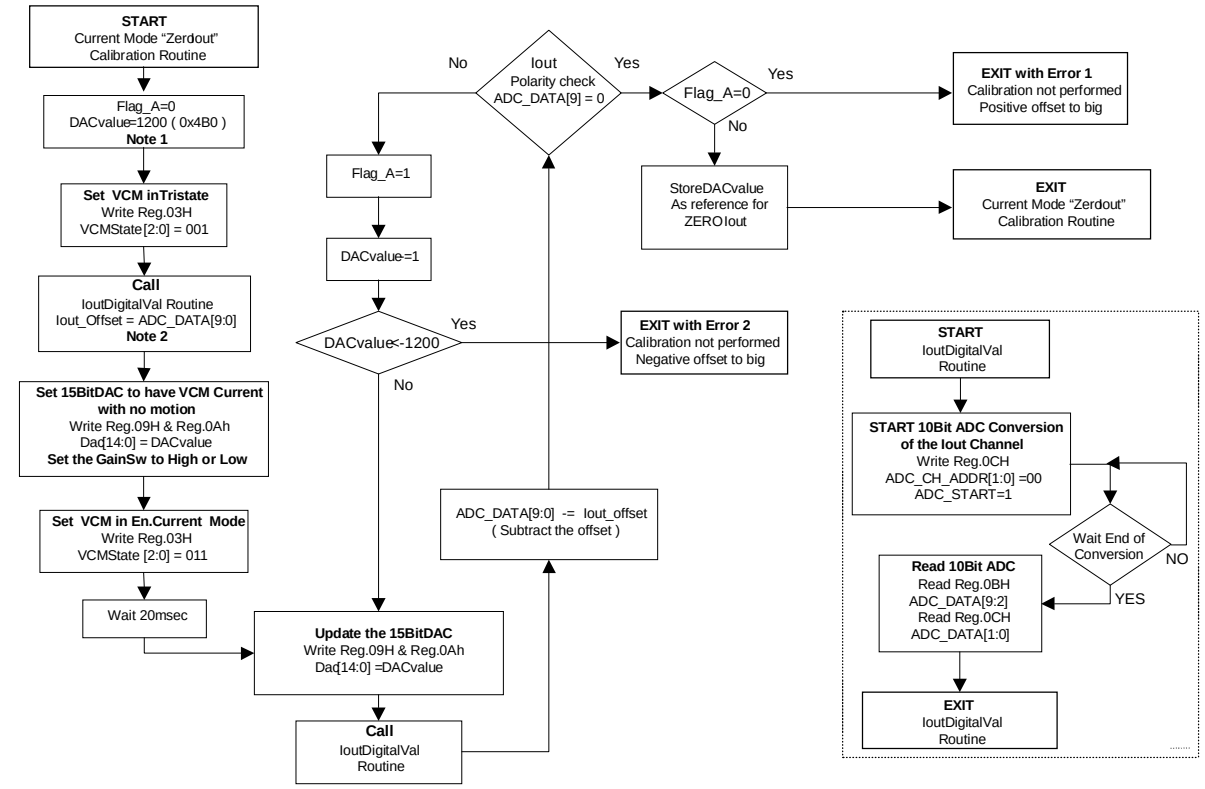
**1)** The VCM loop is enabled (sense amp, error amp, DAC), but the VCM power stage is tri-stated. Thus, the sense amp is guaranteed to be monitoring a zero current condition.
To implement offset calibration, the current command is swept through zero by the controller ASIC. Since the Gm loop is open, the error amp output will be saturated in one direction or the other depending on the current command (to configurate the error opamp as a comparator the external compensation network will be disconnected opening the switch S1). As the command sweeps through the zero current command point, the error amp output will swing to the other extreme. The comparator senses the output swing of the error amp, and through the serial port (Reg. 00H -> b6) interrupts the ASIC. The appropriate DAC value corresponding to the trip point interrupt is the loop zero current offset.

**Figure 9. VCM Current Loop Offset Calibration 1**



**2)** A second approach is considering to have the VCM in stop position; to enable it in current mode configuration driving current in the right direction in order to be sure to mantain the stop position; to decrement the 15bit DAC value to reach the zero current condition using the 10bit ADC to measure the current value.
In the following diagram a detailed flow chart is presented.

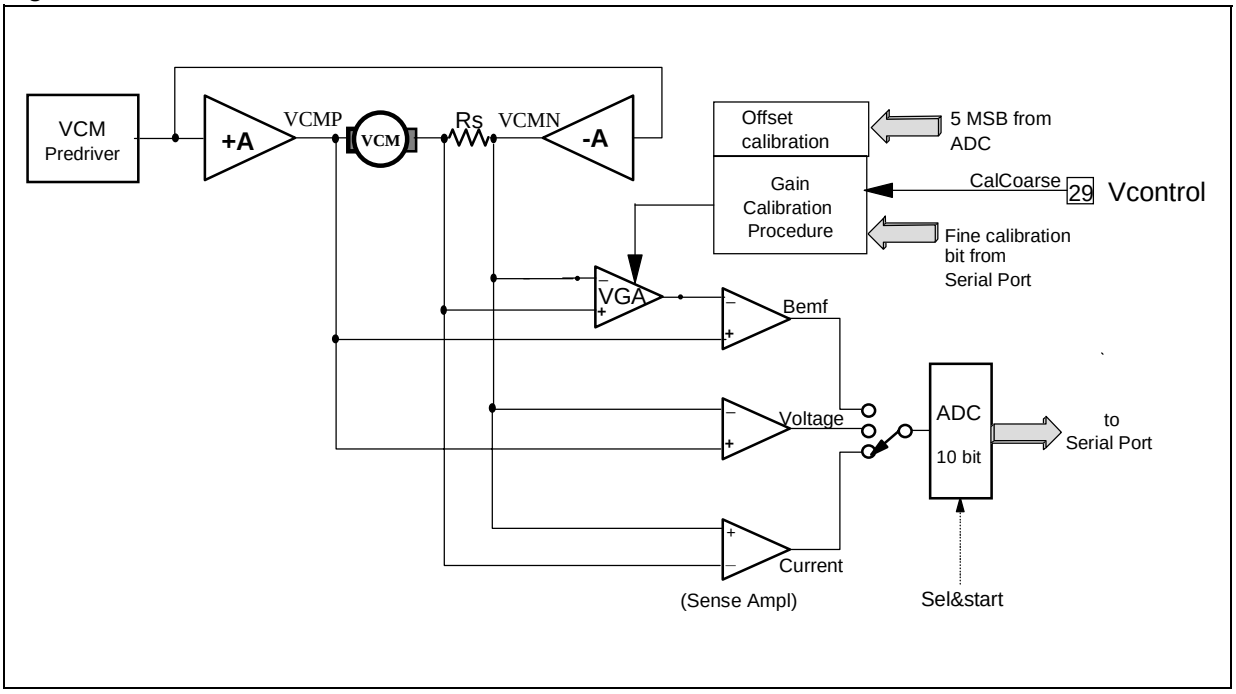
**Figure 10. VCM Current Loop Offset Calibration 2**




Note 1 : once the VCM will be enabled in current mode with the DAC value at 1200 the current will keep the motor against the crash stop position
Note 2 : with the VCM in tristate, the result of the digital conversion of the Iout Channel has to be used as ZERO current offset value

### 3.8 VCM Ramp Load / Unload System

**Figure 11.**




The Ramp Load system is designed to allow a microcontrolled assisted constant velocity for ramp loading and unloading.

VCM Current-Voltage-Bemf monitor circuitry is integrated for the loading or unloading operation. VCM Current-Voltage-Bemf are converted in digital by a 10 bit AD converter and can be read through the serial port.

#### 3.8.1 Load/Unload operation at power good

When both the 12V and 5V are present, the Load/Unload operation can be assisted by the microcontroller. The power stage can be driven in both current and voltage mode and the velocity of the Load/Unload operation is controlled by reading the internal registers that give information regarding the VCM current, voltage and the Bemf generated by the VCM motion.

The VCM current measurements is done by sending to the AD converter the output of the VCM Current Sense Ampl.

The VCM voltage is measured by connecting an operational amplifier, with a scaling factor, to the VCMP and VCMN of the power stage.

The VCM Bemf detection is done using a first amplifier, having a controlled gain, followed by a second operational amplifier implementing the transfer function necessary to BEMF reconstruction. The programmable gain of the first operational amplifier it is necessary to consider various coil resistance values related to different application.

The BEMF information is carry out on pin VCMBEMF (31) for filtering pourpose (the output impedance is typically set to 500ohm).

The conversion in digital of these parameters is used by the microcontroller as a feedback to close the velocity control loop during the ramp loading or unloading operation, and to perform calibrations.

All these signals can enter directly the ADC block (ADCrange bit = 0) or can be scaled to adjust the dynamic range to the ADC one (ADCRange bit = 1).

The scaling factor is set equal to 2.25 for the ‘Current’, ‘Voltage’, ‘Auxiliary’ input channels, while is set to 1.25 for the ‘Bemf’ input channel.

### 3.8.2 Gain Calibration Procedure

The Bemf detector circuitry must be calibrated right before the beginning of any Load/Unload operation.

Because the coil resistance can vary up to 30% due to thermal effects, it is necessary to calibrate the gain of the first stage depending on the ratio between the operating coil resistance value and the sense resistance value.

The output of the Bemf detector circuiry is:

Bemf = OutP - OutM - Rs*Ivcm ( 1+ Rm/Rs)

where: Rm = motor resistance
Rs = sensing resistance

If the Gain of the first stage is matching the ratio between the coil resistance at operating temperature and the sense resistor, the Bemf measured is right the value generated by the VCM motion.

The gain trimming is done with the VCM in a stop position (no Bemf must be generated) with a certain amount of current flowing into the coil; in this condition the gain must be adjusted in order to have zero voltage from the Bemf circuitry.

The gain adjusting is splitted in two phases. A coarse calibration is obtained setting the external resistor divider at the CalCoarse pin (29) following the relation:

Vcontrol = [0.21 + (Rm/Rs) / 28.8]

Vcontrol max. range = Vbg ±0.75V

Where: Vbg = bandgap voltage (typ = 1.25)

A fine calibration is obtained by writing the internal register 02H -> b[3:0]. The fine calibration is used to compensate the variation of the VCM coil resistance according with operating temperature condition.

The calibration is implemented moving the Vcontrol voltage by a percentage indicated on the RLcal table at pag.17.

### 3.8.3 VCM Bemf offset trimming

Due to the high gain necessary to implement the BEMF reconstruction, the inpact of the offset on the output value is very high. For this reason dedicated circuitry, using the 5 MSB of the AD converter, has been integrated in order to compensate this offset.

The flow chart below reported are describing the method to implement the offset calibration.

**Figure 12. VCM Bemf Offset Calibration CLEAR Routine**

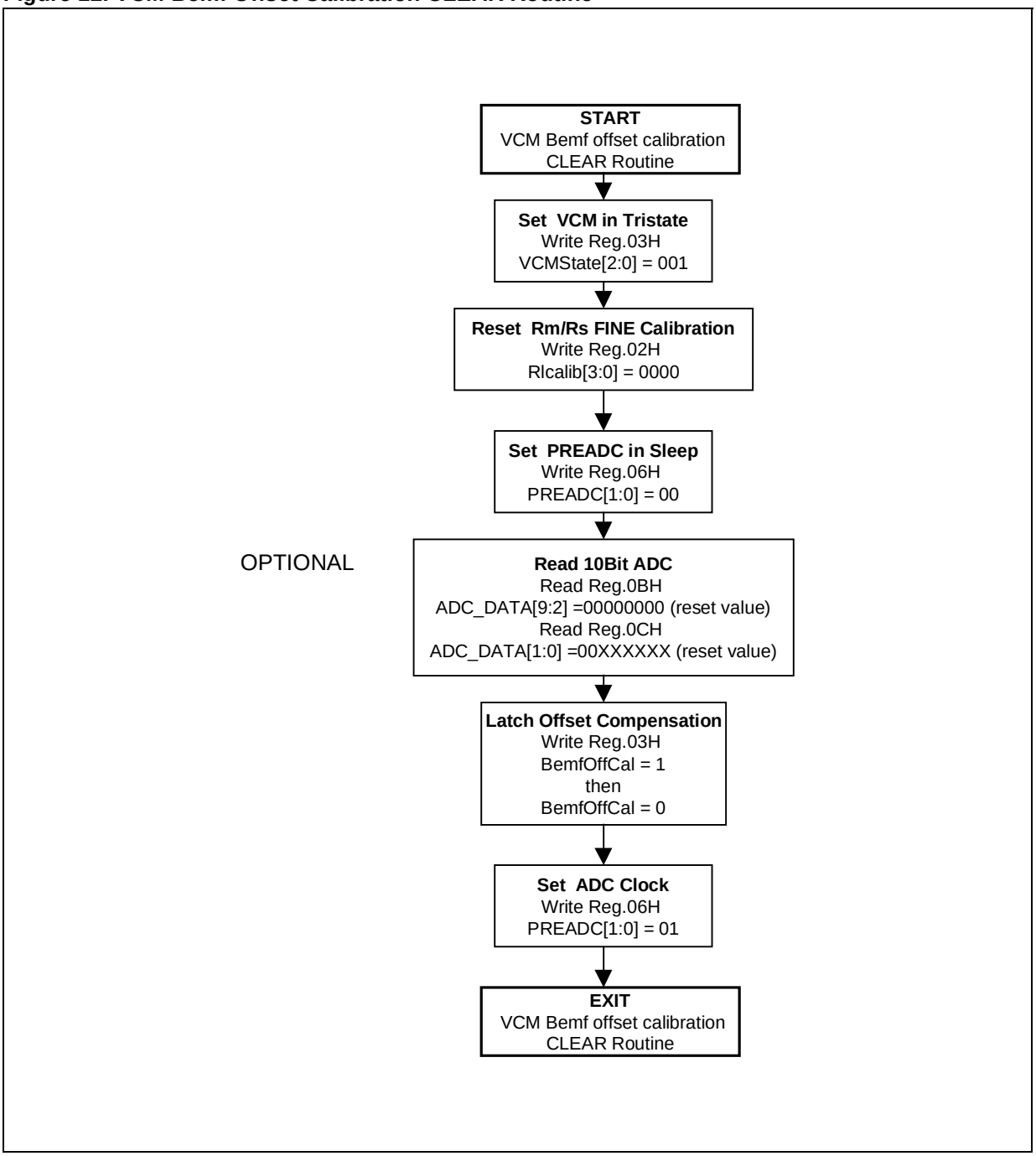
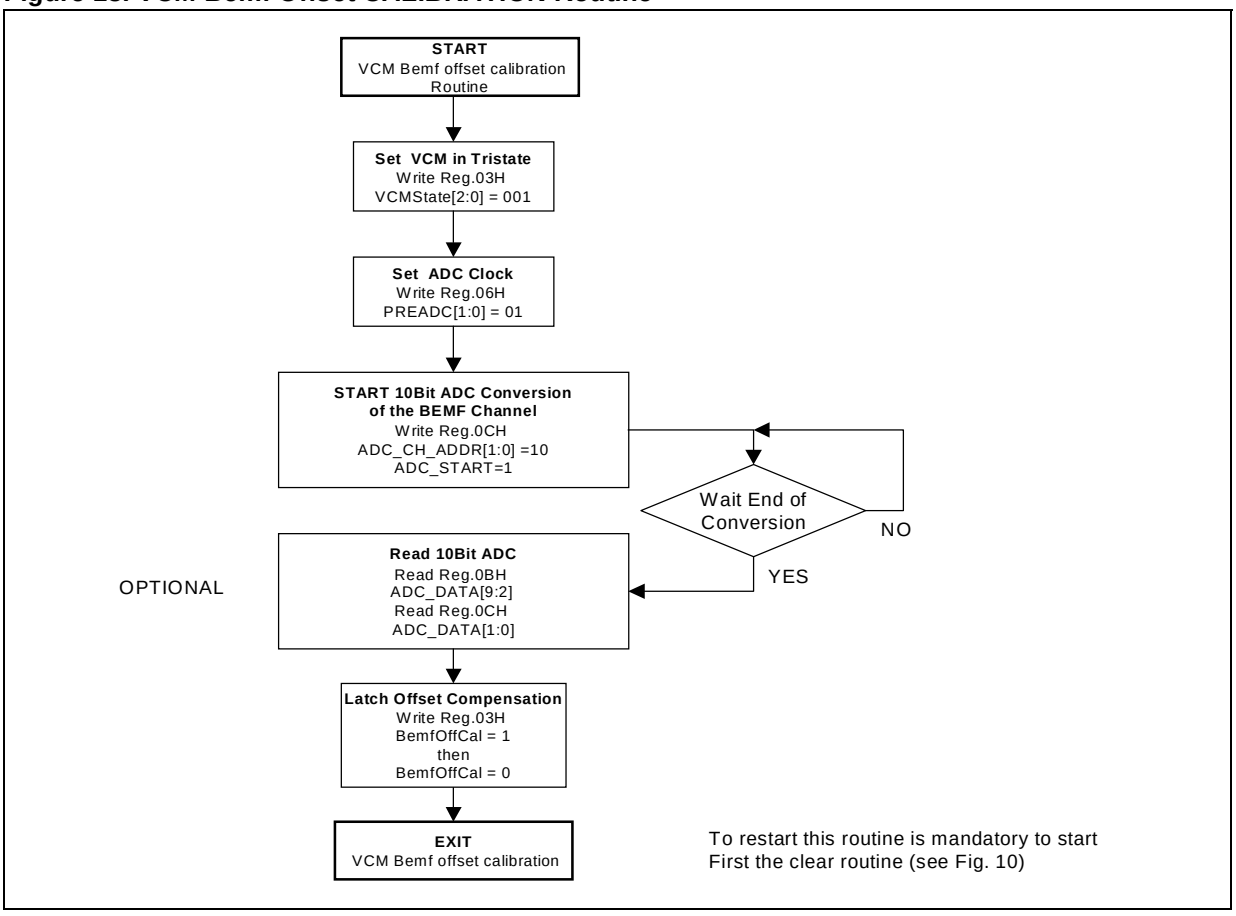


**Figure 13. VCM Bemf Offset CALIBRATION Routine**




At the end of the calibration routine the analog value measured at pin 31 is rapresenting the VCM BEMF value at the zero motion (BEMF zero value). With the ADC it is possible to operate a new convertion in order to memorize this value and to take in account of it during the load/unload procedure.

### 3.8.4 Power Off Unload - Active brake and constant voltage unload operation

In case of power shut down, an unload procedure start automatically in order to take the heads over the ramp in the parking position (the same procedure can be also enabled, when the power is on, via serial port programming the unload/retract status of the VCM -> reg. 03H. In this case at the end of the unload phase the spindle motor is driven in tri-state condition).

The unload procedure doesn't start at power off if the VCM status bit are set to 000 because the system is considering the heads already in park position. No entering the unload procedure also the spindle brake is not activated.

The unload procedure is done in two step:

- active brake

- constant voltage unload operation

The unload procedure take place only if the VCM status bit have moved from the 000 configuration. Otherwise the unload procedure doesn't start and in case of power shut down the spindle motor enter the brake condition.

Active Brake : it is used to have a fast recovery of the VCM velocity down to the unload programmed velocity.

If just before a power shut down a fast seek was commanded, it is necessary to recover the VCM velocity in

order to avoid to rise the ramp or to meet the ID crash stop at high speed.

The over velocity detector circuit consist in a window comparator; in case of power failure the VCM power stage is tri-stated (for a fixed time about 200µs) in order to detect the amplitude of the Bemf generated by the VCM motion.

If the VCM Bemf is out of the window of the over velocity detector (this means that the heads are travelling at high speed versus the inner or outer position), the active brake routine is invoked.

The voltage threshold ( = motor electrical constant * motor angular velocity), setting the over velocity detector window, is set internally to 1.1V (to 0.4V if 5V application is considered).

At the contrary, if the VCM speed is inside the window (the heads where on track or moving slowly) the active brake is skipped and the constant unload operation is commanded.

The active brake routine consist in a procedure that drive the VCM alternately with two steps:

- first activating the diagonal of the power stage in order to drive current in the right direction to slow down the speed of the VCM for a time (RLTonBrake) that is half of the programmed RLToffBrake.

- then activating both the low side drivers of the power stage putting the VCM in short brake condition for a programmable time (RLToffBrake).

With the VCM in short brake the current into the coil is forced by the Bemf generated by the motion of the motor and the sense amplifier output is sensed in order to detect indirectly the VCM speed.

The switch between the active brake routine and the constant voltage unload operation is done when the VCM current, measured at the sense amplifier output during the short brake condition, fall down to zero (VCM is stopped).

The RLToffBrake (and so the RLTonBrake) time can be programmed by writing the Reg. 02H.

The active brake procedure can enabled/disabled by writing the Reg. 01H. In case the active brake procedure is disabled, at power off the constant unload operation start immediately.

Constant Voltage Unload operation : a constant voltage (with a sink and source capability) is applied to the VCM in order to drive the heads over the ramp in the parking position.

According with the contents of the registers REG. 01H it is possible to perform the unload operation in one or two steps and for each steps to select the voltage level applied to the VCM.

The capacitor connected at the Timer1 (pin 28) define the total time of the unload operation ; during the unload operation this capacitor is discharged by un internal constant current generator.

Programming the bit ‘b3b2b1’ of the REG. 01H it is possible to select different unload procedures:

With these bit set to 000 the unload is done in one step with the voltage selected by the two bit RLvoltage1 of REG. 01H.

With these bit set to 111 the unload is done in one step with the voltage selected by the two bit RLvoltage2 of REG. 01H.

The spindle motor is tristated during the unload operation

The other combinations of the bit ‘b3b2b1’ defines different threshold for the comparison with the discharging voltage of the capacitor at pin 21 .

The timing for the first step is with the capacitor voltage greater then the programmed threshold, the timing for the second step start when the capacitor voltage is below the threshold and end when the capacitor is discharged under the 'end unload threshold' (0.2V typ) .

In all the cases, when the capacitor at pin 21 is discharged under the 'end unload threshold' the spindle motor is driven inbrake condition.

The typical value of the retract procedure timing can be extimated using the following expression:

$T = Tstep1 + Tstep2 = 1.15 * C_{ext}$

Where:

Cext = External capacitor at pin ‘Timer1’ (28) measured in uF

**Figure 14. Costant voltage retract operation at power down**

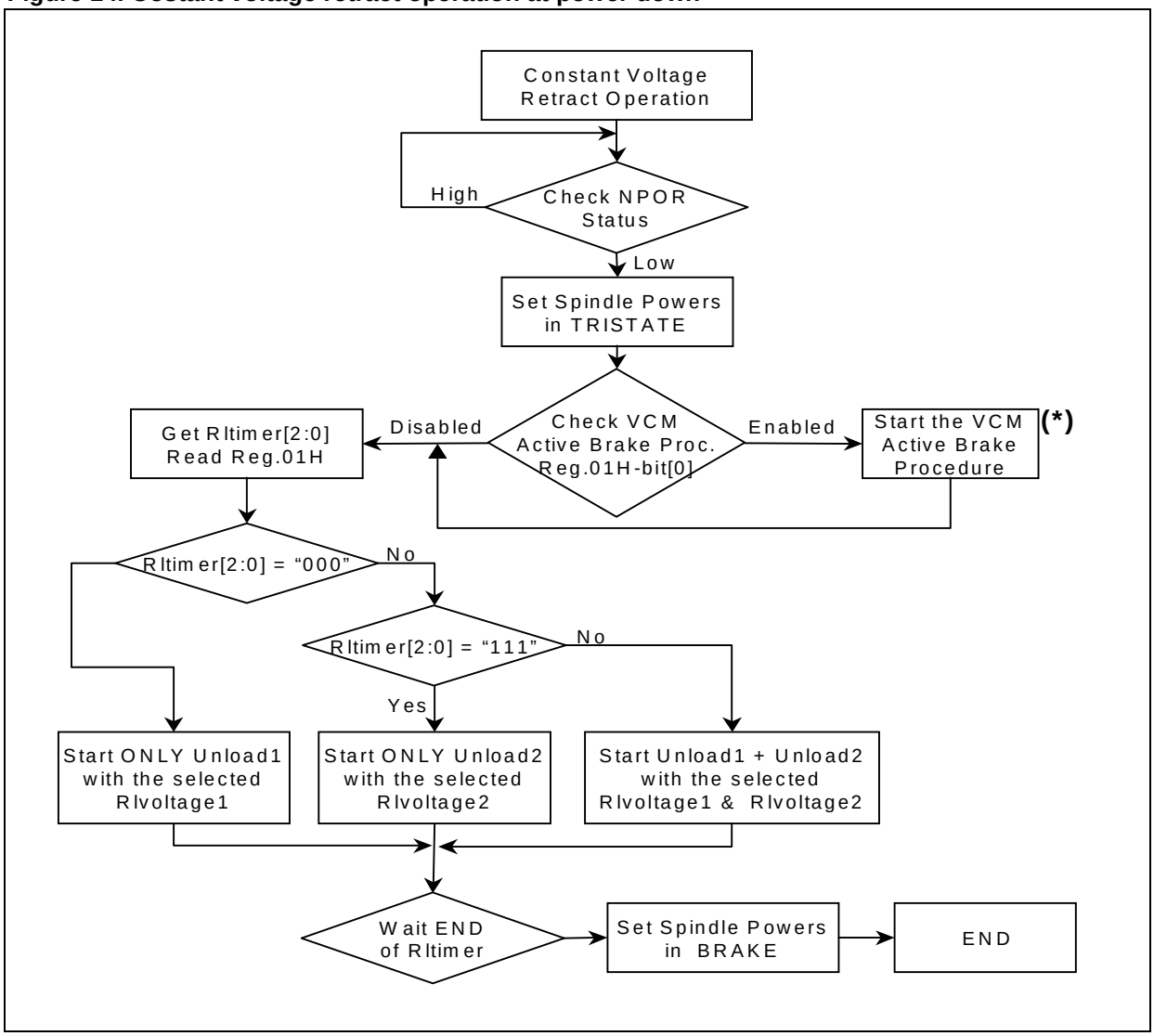
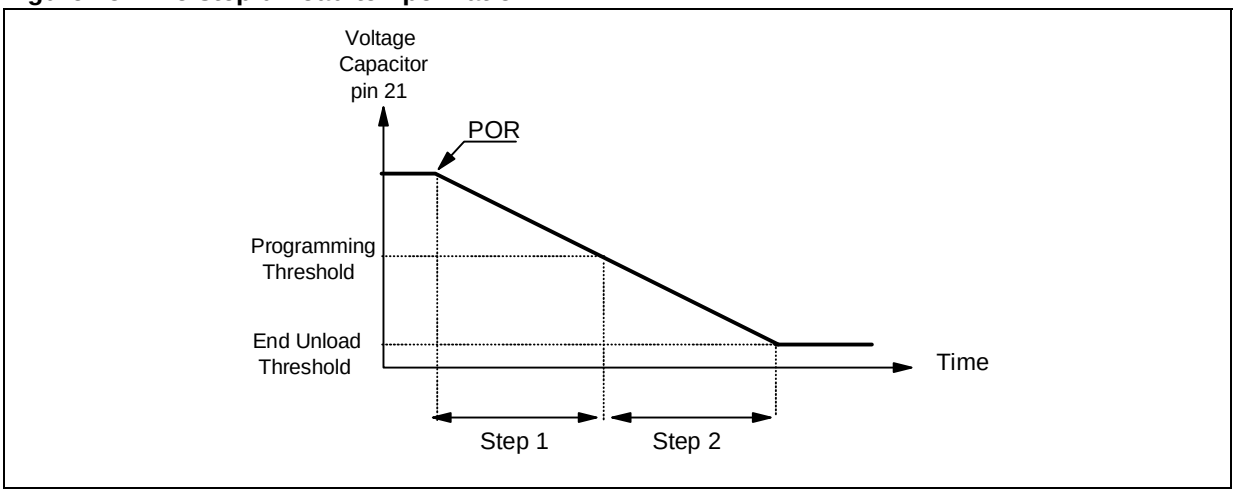



**Figure 15. Two step unload temporization**



### 3.8.5 Constant Voltage Unload operation at POWER ON

The same costant voltage retract operation can be activated via software (during a power on phase). In that case no actions are implemented to the spindle motor; the spindle motor will continue to mantain its running status.

Again in power on condition if the bit 'b3b2b1' of the REG. 01H are set to 000 or 111 only one step costant voltage retract is activated as in power off condition with the difference that when the 'End unload threshold' is reached the retract voltage is mantained applied to the motor until a different programmation is asserted via serial port by the microcontroller.

In all the others 'b3b2b1' combination as the timer1 is elapsed the VCM is put in tristate condition.

**NOTE: In case of Hard Disk application with CSS operation (no Ramp Loading), the polarity of the VCM connection must be reversed. In this way the active brake and the constant voltage unload operations will force the heads in the inner position of the disks.**

## 3.9 10 bit AD converter

The L7250 device includes a 10 bit analog to digital converter (hereafter ADC).

The ADC uses a two complement output code.

The ADC converts one of four different channels on demand, through SPI, and result of conversion can be read from SPI too. The uC tells the ADC which channel must be converted, gives a start signal, reads the conversion result; all this happens through the SPI.

The ADC convertion frequency, then its conversion time, could be changed using two bits into the serial port (Reg 06H -> b1,b2). Setting these two bit to the configuration 00 the ADC can be disabled entering a sleep mode status.

Hereafter is listed the recommended sequence of operations to obtain a conversion from ADC:

A) µC selects which channel must be converted, writing the ADC_CH_ADDR field in SPI (Reg 0CH -> b1,b2);

µC selects the ADC input range writing the ADCRange bit (Reg 0CH -> b3);

µC writes high the ADC_START bit (Reg 0CH ->b0) in SPI (end of required conversion automatically resets it);

B) now µC can read the conversion result from the SPI registers;

C) a new conversion can be required.

The µC isn't allowed to require a conversion start when the ADC is already running; the start bit can be written anyway, but ADC logic ignores it and continues the current conversion. If the uC avoids modifies over the ADC_START bit, it can be used as a flag to state the end of the conversion.

The result of conversion is ten bits wide, larger than the 8 bits SPI registers, so it has been spanned over two registers; if allowed by the precision required for the application, only the 8 msbits can be read with a single SPI read operation, saving some time.

A new conversion can be required after the end of the previous one but before the read-back of the result, i.e. swapping the order of (B) and (C) points listed before; working this way, it's possible to convert values closer in time than with the previous sequence.

SPI includes an additional read-only field (2bits) that contains the channel number related to the present conversion result.

## 4 POWER MONITOR, VOLTAGE REGULATORS AND SHOCK SENSOR

### 4.1 NPOR - Power ON Reset

The Power On Reset circuit monitors 12V and 5V power supplies as well as 3.3V and 2.5V regulators. If any monitored voltage falls below its under voltage threshold, NPOR is latched low after an internal glitch filter delay. When the positive regulators are in position, a delay time is added, the POR delay, before NPOR goes high and the reset condition is cleared. During this delay time, any power fault will reset the POR delay and start the process over again.

$T_{Delay} = 0.520 * C_{ext}$

Where :

$C_{ext}$ = External capacitor on pin CPOR measured in uF.

### 4.2 Linear Voltage Regulators:1.8V & 3.3V

The 3.3V linear use an external NPN transistor connected to the 5V power supply line, instead the 1.8V linear regulator use an external NPN transistor that could be connected to the 3.3V line or to the 5V power supply line.

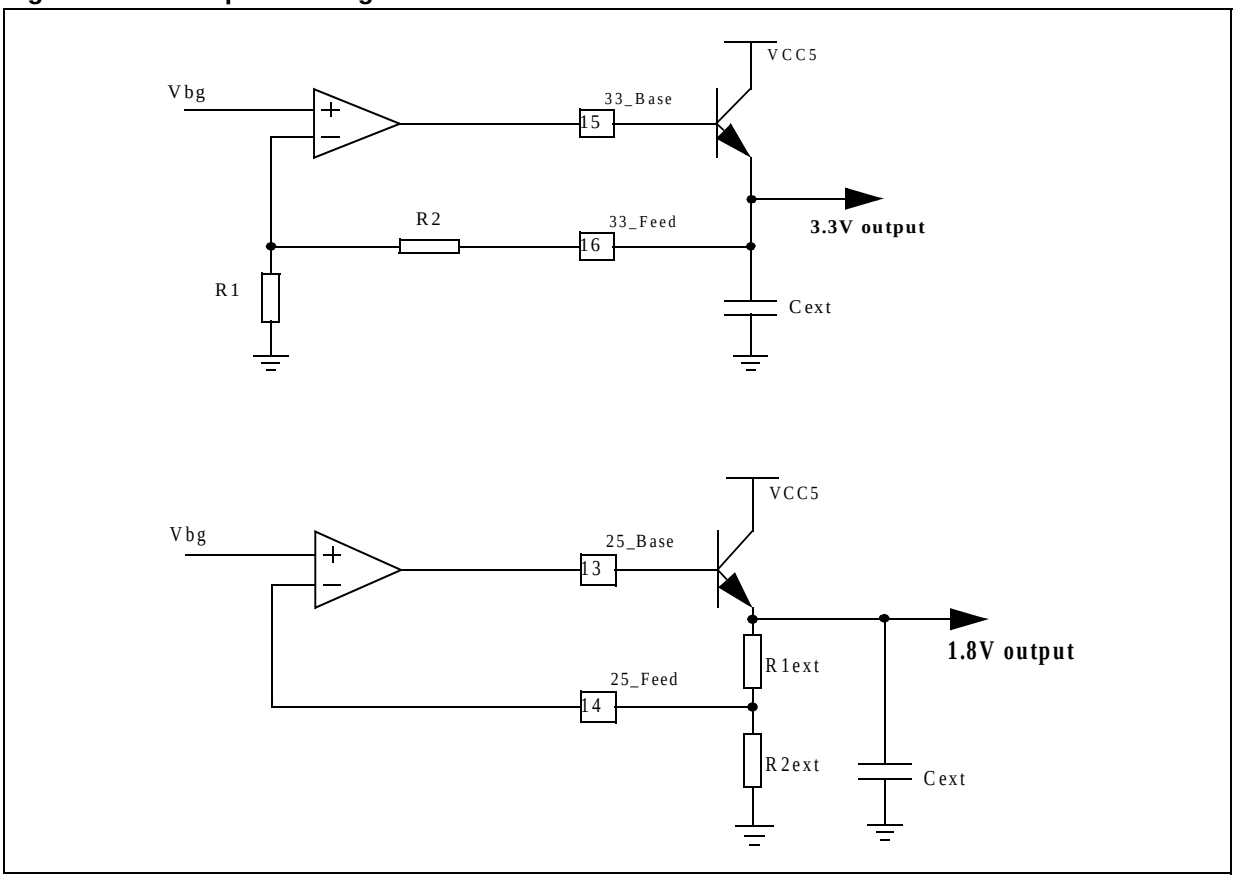
To fix the 1.8V regulator voltage output an external resistor divider as to be used.

The regulated voltage could be varied around the 1.8V value (from 1.3V to 2V) choosing the external divider appropriately.

The stability of the two regulators is guarantee by the external filter capacitor .

The internal Vbg reference is trimmed at the wafer level.

**Figure 16. Linear positive regulators**



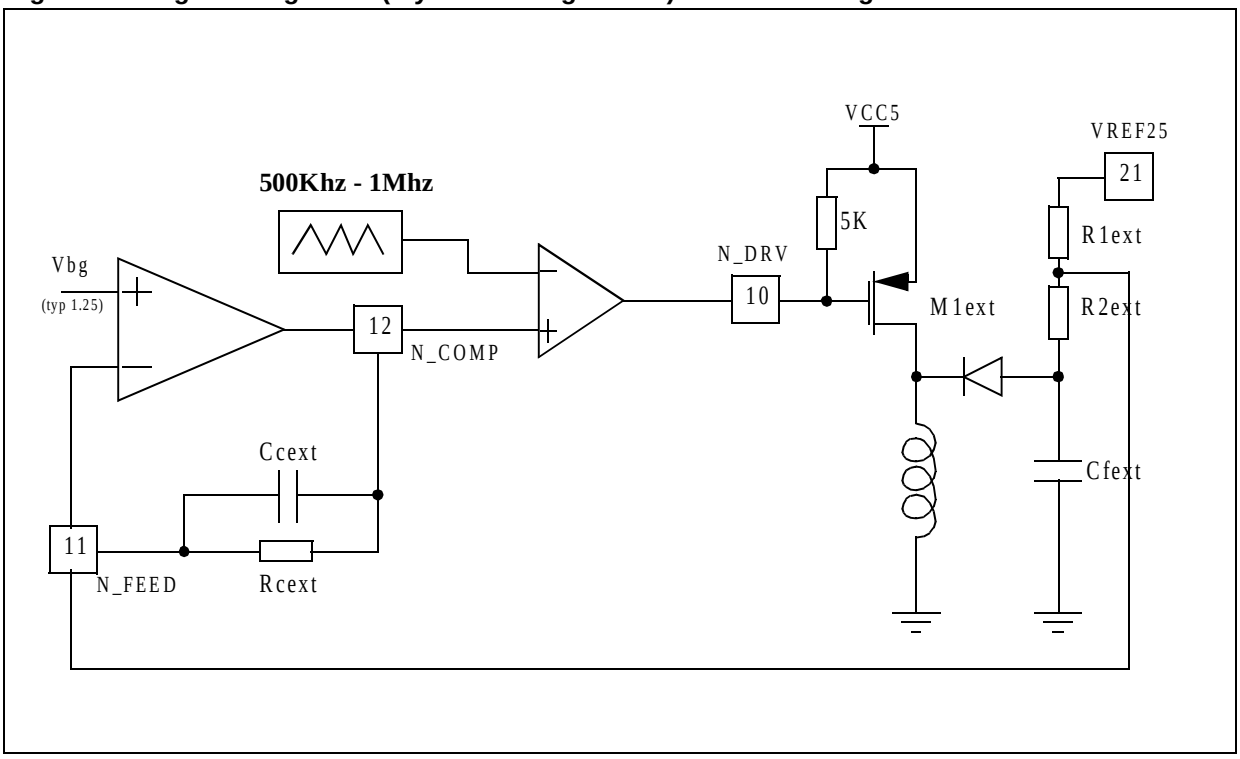
### 4.3 Negative Voltage Regulator (flyback configuration)

This is the default Negative Voltage Regulator configuration; programming the Test Register is possible to re-configurate this regulator following the indication present on the next paragraph.

The negative voltage regulator is a fixed frequency switcher intended to provide bias for the MR head preamp. The NVR consists of an internal triangular wave oscillator, an error amplifier, a comparator and a circuitry to soft start_up the regulator itself, in conjunction with an external PMOS power device, power diode, inductor, capacitor, feedback resistors and compensation network (refer to the block diagram of the negative voltage regulator including also the external components).

The error amp compares the external voltage feedback to the internal reference (Vbg = 1.25V). The voltage difference value is scaled by two external resistors. The ratio of these two resistors determines the nominal value of the regulated negative voltage (the internal reference is set to the bandgap voltage ~1.25V). The error amplifier input is available at N_FEED pin and the amplifier output is available at N_COMP pin. The voltage error gain and the loop compensation can be adjusted by the external components across these two pins. The output of the error amplifier is compared to an internal triangular wave oscillator to determine the duty cycle of the external PMOS power switch. A voltage clamp is placed on the error amplifier output to limit the maximum duty cycle. The nominal value of the triangular wave oscillator frequency is 500 kHz (programming the test register Reg 0FH to '00001001' it is possible to increment the switching frequency to the nominal value of 1Mhz). During the ON portion of the duty cycle, the PMOS charges an external inductor. During the OFF phase, the inductor charges a capacitor through an external diode, in a voltage inverter configuration. This architecture avoids any negative voltage on the L7250 IC pins. Under normal specified load conditions and correct scaling of the external components the regulator circuit should operates in a constant frequency variable duty cycle switch mode without any cycle slips. The NVR include also a digital soft start_up circuitry in order to limit the in rush current coming from the power supply when the regulator is turned-on. The NVR is controlled via serial port (using the Reg. 05H -> b1 the regulator could be turned on and off). During the power-up and power-down phases the regulator is always off being the serial port in reset status then the VnegEn bit equal to zero. During those phases the N_DRV output driver is in tri-state condition then an external pull-up to assure the Pch off condition must be considered.

**Figure 17. Negative regulator (Flyback configuration) - default configuration**



### 4.4 Negative Voltage Regulator (CUK configuration)

Programming the Test Register Reg 0FH to '00101001' it is possible to re-configurate the negative regulator loop inverting its polarity. All the others test register (Reg0FH) configurations are resetting to the default negative voltage regulator loop polarity (take care to avoid the test register bits modification if the 'CUK configuration' hardware is present and the negative regulator is enabled).

The functionality of the regulator is the same descripted on the previous paragraph with the difference that the loop polarity is reversed to permit to drive the external Nch component.

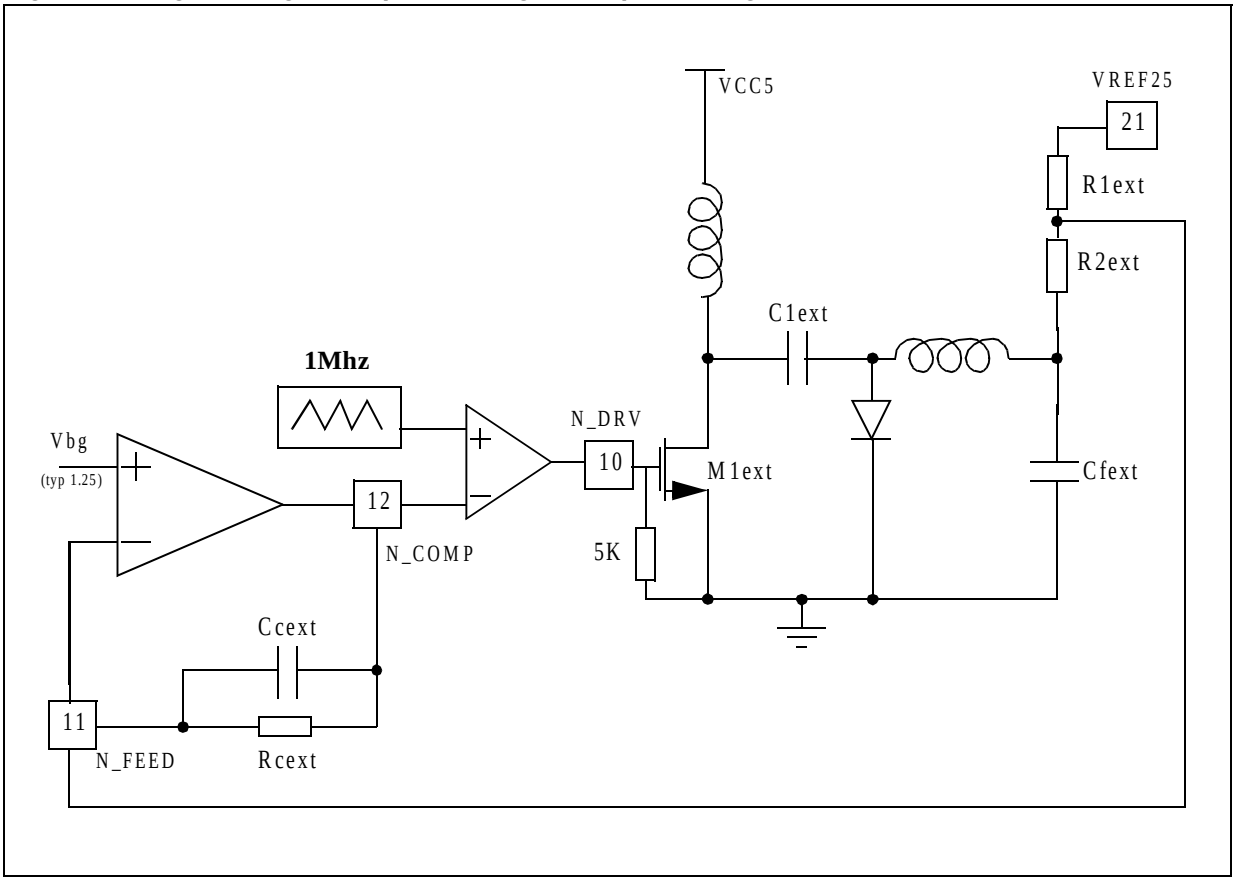
During this operation the nominal value of the triangular wave oscillator frequency is always fixed to 1 MHz.

The NVR is controlled via serial port (using the Reg. 05H -> b1 the regulator could be turned on and off).

Take care to program correctly the Test Register to enter the CUK configuration before to enable the NVR.

During the power-up and power-down phases the regulator is always off being the serial port in reset status then the VnegEn bit equal to zero. During those phases the N_DRV output driver is in tri-state condition then an external pull-down to assure the Nch off condition must be considered.

**Figure 18. Negative regulator (CUK configuration) - Test register => 00101001**



### 4.5 Shock Sensor

This block takes input from a piezoelectric or charging mode shock sensor element (selectable using the SPI bit ShockConf -> Reg02H, bit 7 ), and includes external filtering capability. A digital latched signal is available on SkDout pin if the Sken bit (from SPI) is set to 1 otherwise the SkDout pin is transparent to the shock signal.

If the output signal has been latched, a pulse to zero of the Sken bit it is necessary to clear it.

The shock sensor element will be connected to the Skin and VREF25.

**Figure 19. Piezoelectric Shock Sensor typical application block diagram (Reg02H->bit7=0)**

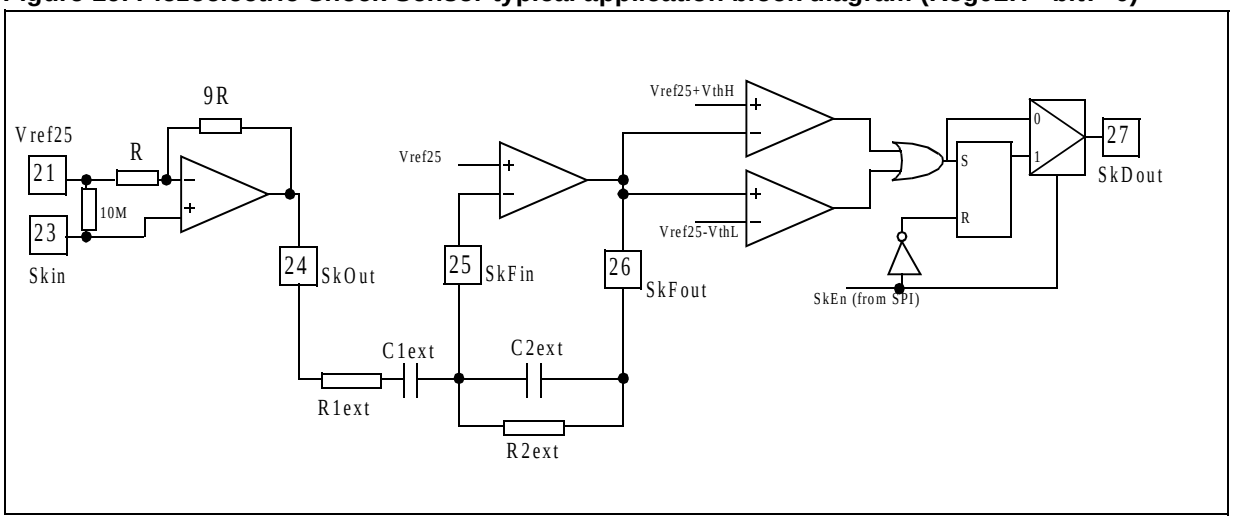
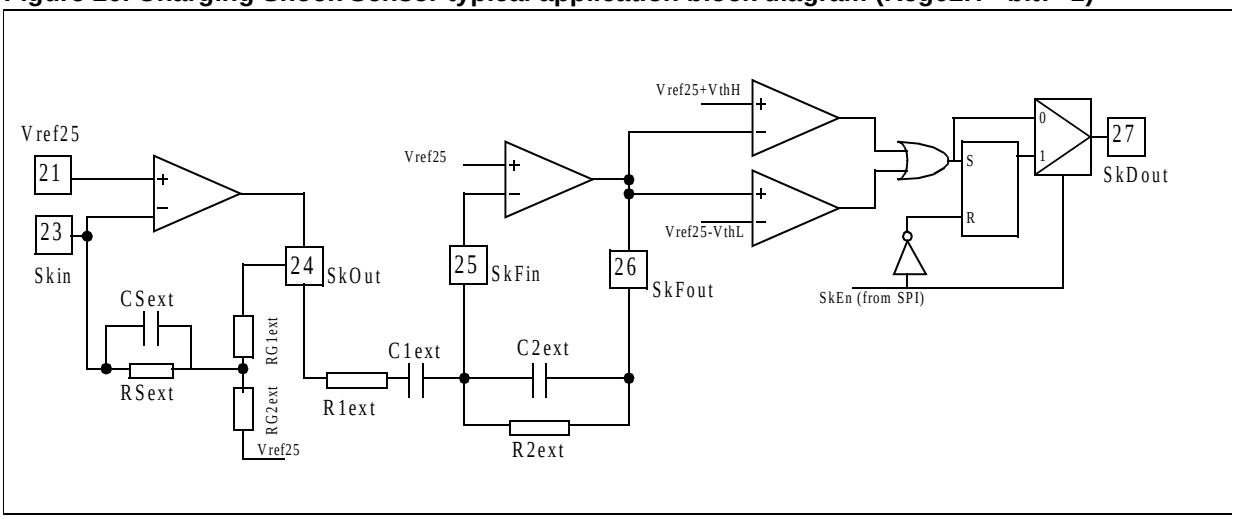



**Figure 20. Charging Shock Sensor typical application block diagram (Reg02H->bit7=1)**



### 4.6 Over Temperature Protection

L7250 has a temperature protection circuit consisting of a temperature sense circuit and two comparators. The temperature sense circuit generates a voltage proportional to the absolute die temperature. One comparator trips when the die temperature exceeds 140 deg C, asserting the temperature warning signal in the status register (ThWarn in the Reg 00H -> b3). The thermal warning comparator has nominally 20 deg C hysteresis.

The thermal Shutdown comparator trips when the die temperature exceeds 160 deg C, indicates an over temperature condition in the status register (ThShutdown in the Reg00H -> b4). The status register is transparent to the thermal shutdown information.

If the ThShutdown bit is equal to zero only the flag on the status register is activated, else the L7250 is driven into thermal shutdown mode, which initiates Unload of the Voice Coil Motor (no actions on the Spindle motor has been taken). Hysteresis of 25 deg C on this comparator allows the die temperature to stabilize before it is re-enabled.

Iif the ThShutdown bit is set to 1, the thermal Shutdown condition is latched, then to re-enable the function a reset cycle is needed (ThShutdown bit must be programmed to 0, then set again to 1).

**Figure 21. 12V Application diagram**

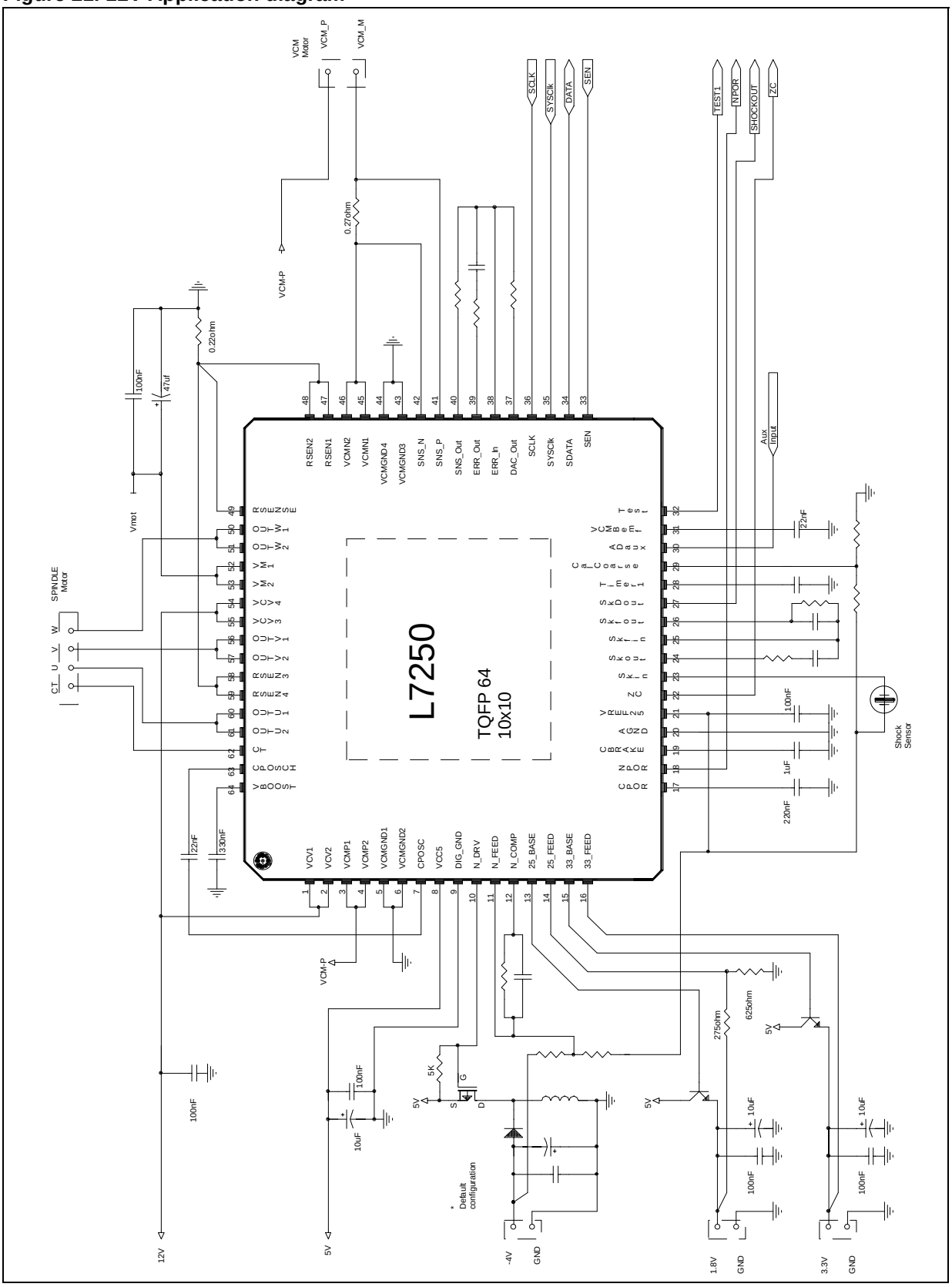
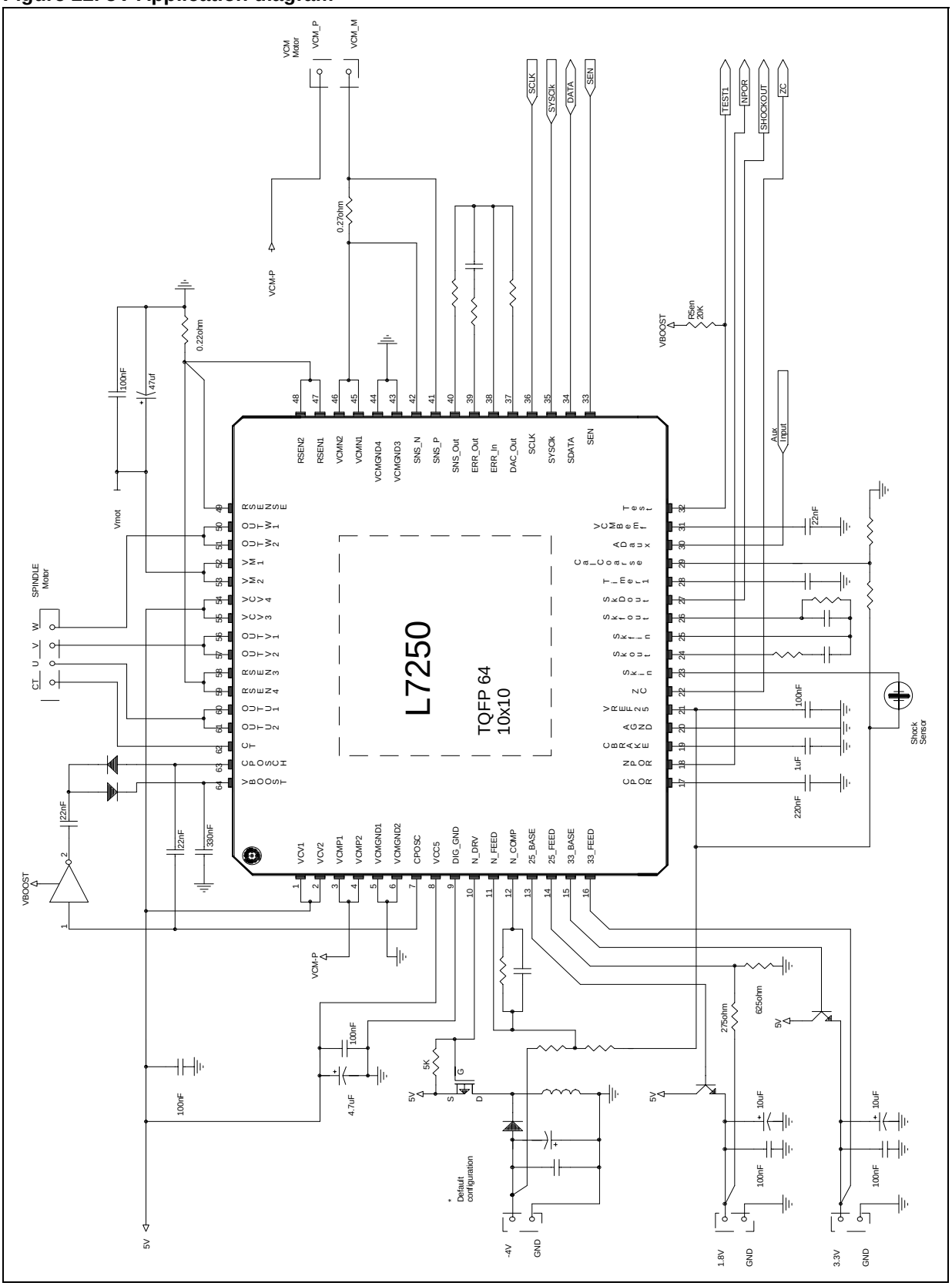
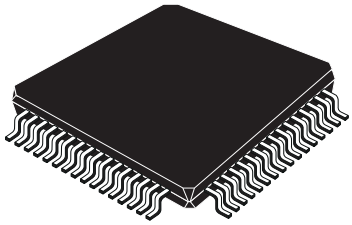


**Figure 22. 5V Application diagram**



| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B | 0.18 | 0.23 | 0.28 | 0.007 | 0.009 | 0.011 |
| C | 0.12 | 0.16 | 0.20 | 0.0047 | 0.0063 | 0.0079 |
| D | | 12.00 | | | 0.472 | |
| D1 | | 10.00 | | | 0.394 | |
| D3 | | 7.50 | | | 0.295 | |
| e | | 0.50 | | | 0.0197 | |
| E | | 12.00 | | | 0.472 | |
| E1 | | 10.00 | | | 0.394 | |
| E3 | | 7.50 | | | 0.295 | |
| L | 0.40 | 0.60 | 0.75 | 0.0157 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0393 | |
| K | 0°(min.), 7°(max.) | | | | | |

## OUTLINE AND MECHANICAL DATA



## TQFP64