

SERIAL ACCESS RTC WITH ALARMS

FEATURES SUMMARY

- 2.0 TO 5.5V CLOCK OPERATING VOLTAGE
- COUNTERS FOR TENTHS/HUNDREDTHS OF SECONDS, SECONDS, MINUTES, HOURS, DAY, DATE, MONTH, YEAR, and CENTURY
- SERIAL INTERFACE SUPPORTS I²C BUS (400KHz)
- PROGRAMMABLE ALARM and INTERRUPT FUNCTION
- LOW OPERATING CURRENT OF 200µA
- OPERATING TEMPERATURE OF -40 TO 85°C

Figure 2. 8-pin SOIC Package

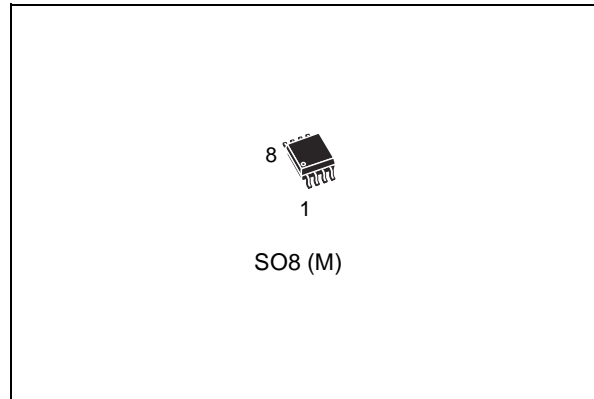


Figure 1. Logic Diagram

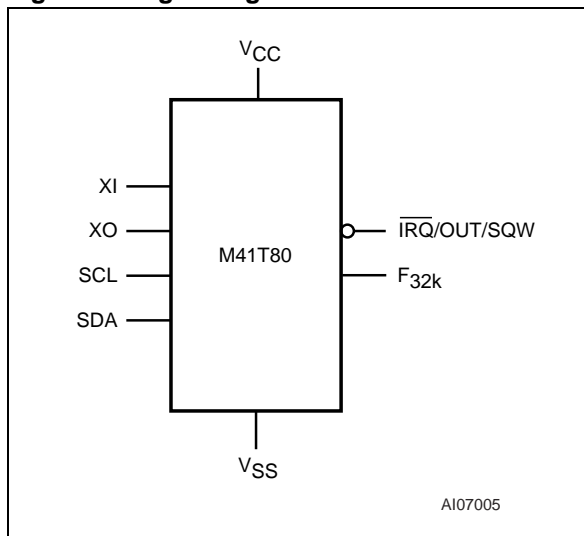


Table 1. Signal Names

| | |
|---|--|
| XI | Oscillator Input |
| XO | Oscillator Output |
| $\overline{\text{IRQ}}/\text{OUT}/\text{SQW}$ | Interrupt / Output Driver / Square Wave (Open Drain) |
| SDA | Serial Data Input/Output |
| SCL | Serial Clock Input |
| F _{32k} | 32kHz Square Wave Output (Open drain) |
| V _{CC} | Supply Voltage |
| V _{SS} | Ground |

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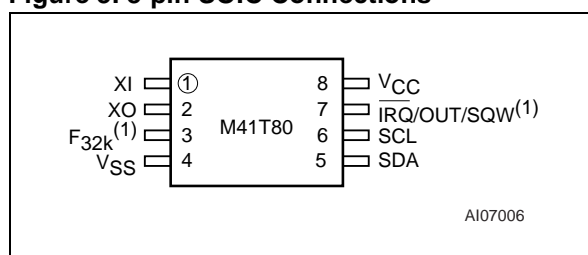
SUMMARY DESCRIPTION

The M41T80 Serial Access TIMEKEEPER® SRAM is a low power Serial RTC with a built-in 32.768 KHz oscillator (external crystal controlled). Eight registers (see Table 8, page 13) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 12 registers provide status/control of Alarm, 32kHz output, and Square Wave functions. Addresses and data are transferred serially via a two line, bi-directional I²C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

Functions available to the user include a time-of-day clock/calendar, Alarm interrupts, 32kHz output, and programmable Square Wave output. The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

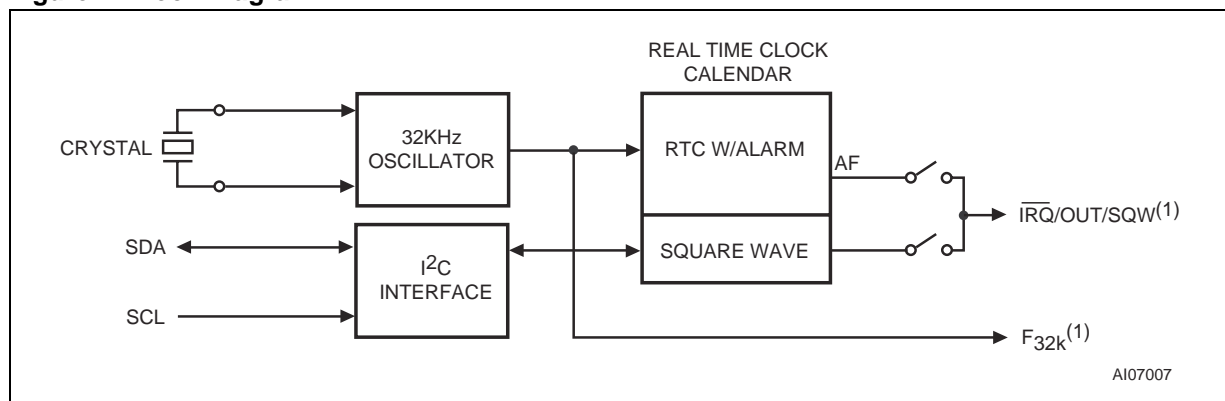
The M41T80 is supplied in an 8-pin SOIC.

Figure 3. 8-pin SOIC Connections



Note: 1. Open drain output.

Figure 4. Block Diagram



Note: 1. Open Drain output

MAXIMUM RATING

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

| Sym | Parameter | Value | Unit |
|---------------------------------|---|------------------------------|------|
| T _{STG} | Storage Temperature (V _{CC} Off, Oscillator Off) | -55 to 125 | °C |
| V _{CC} | Supply Voltage | -0.3 to 7 | V |
| T _{SLD} ⁽¹⁾ | Lead Solder Temperature for 10 Seconds | 260 | °C |
| V _{IO} | Input or Output Voltages | -0.3 to V _{CC} +0.3 | V |
| I _O | Output Current | 20 | mA |
| P _D | Power Dissipation | 1 | W |

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 to 120 seconds).

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

| Parameter | M41T80 |
|---|----------------------------|
| Supply Voltage (V_{CC}) | 2.0 to 5.5V |
| Ambient Operating Temperature (T_A) | -40 to 85°C |
| Load Capacitance (C_L) | 100pF |
| Input Rise and Fall Times | ≤ 50 ns |
| Input Pulse Voltages | $0.2V_{CC}$ to $0.8V_{CC}$ |
| Input and Output Timing Ref. Voltages | $0.3V_{CC}$ to $0.7V_{CC}$ |

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Measurement I/O Waveform

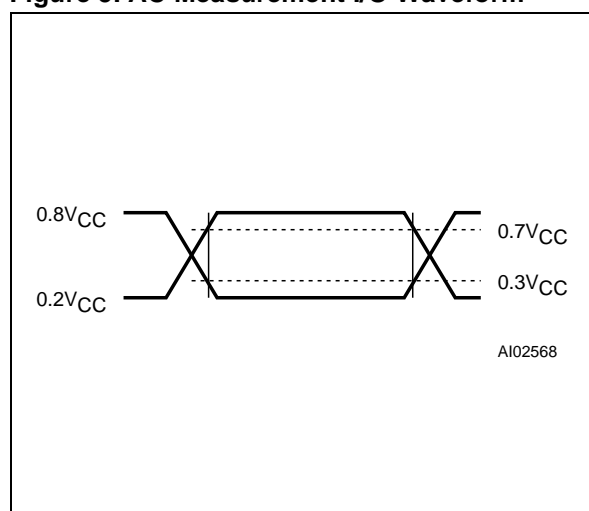


Table 4. Capacitance

| Symbol | Parameter ^(1,2) | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| C_{IN} | Input Capacitance | | 7 | pF |
| $C_{OUT}^{(3)}$ | Output Capacitance | | 10 | pF |
| t_{LP} | Low-pass filter input time constant (SDA and SCL) | | 50 | ns |

Note: 1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
 2. At 25°C, $f = 1$ MHz.
 3. Outputs deselected.

Table 5. DC Characteristics

| Symbol | Parameter | Test Condition ⁽¹⁾ | | Min | Typ | Max | Unit |
|---------------------------------|--|--|--------------------------|--------------------|-----|-----------------------|------|
| I _{LI} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | | | | ±1 | μA |
| I _{LO} | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{CC} | | | | ±1 | μA |
| I _{CC1} | Supply Current | Switch Freq (SCL) = 400kHz | | 3.0V | | 30 | μA |
| | | | | 5.5V | | 200 | μA |
| I _{CC2} ⁽²⁾ | Supply Current (standby) | All Inputs = V _{CC} - 0.2V Switch Freq (SCL) = 0Hz | 32KE = 1 or SQWE = 1 | 3.0V | 1.8 | 3.0 | μA |
| | | | | 5.5V | | 35 | μA |
| | | | 32KE = 0 and SQWE = 0 | 3.0V | 1.5 | 2.4 | μA |
| | | | | 5.5V | | 31 | μA |
| V _{IL} | Input Low Voltage | | | -0.3 | | 0.3V _{CC} | V |
| V _{IH} | Input High Voltage | | | 0.7V _{CC} | | V _{CC} + 0.3 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 3.0mA | | | | 0.4 | V |
| | Output Low Voltage (Open Drain) ⁽³⁾ | I _{OL} = 10mA | | | | 0.4 | V |

Note: 1. Valid for Ambient Operating Temperature: T_A = -40 to 85°C; V_{CC} = 2.0 to 5.5V (except where noted).

2. At 25°C.

3. For IRQ/FT/OUT, $\overline{\text{RST}}$, and 32kHz pins (Open Drain)

Table 6. Crystal Electrical Characteristics

| Sym | Parameter ^(1,2) | Min | Typ | Max | Units |
|----------------|----------------------------|-----|--------|-----|-------|
| f _O | Resonant Frequency | | 32.768 | | kHz |
| R _S | Series Resistance | | | 60 | kΩ |
| C _L | Load Capacitance | | 12.5 | | pF |

Note: 1. Externally supplied if using the SO8 package. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@kdsj.co.jp or <http://www.kdsj.co.jp> for further information on this crystal type.

2. Load capacitors are integrated within the M41T80. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

OPERATION

The M41T80 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 20 bytes contained in the device can then be accessed sequentially in the following order:

1. Tenths/Hundredths of a Second Register
2. Seconds Register
3. Minutes Register
4. Century/Hours Register
5. Day Register
6. Date Register
7. Month Register
8. Year Register
9. Control Register
10. 32kE Bit
- 11 - 16. Alarm Registers
- 17 - 19. Reserved
- 20 - Square Wave Register

2-Wire Bus Characteristics

The bus is intended for communication between different IC's. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High.
- Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from high to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data Valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called "transmitter," the receiving device that gets the message is called "receiver." The device that controls the message is called "master." The devices that are controlled by the master are called "slaves."

Acknowledge. Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 6. Serial Bus Data Transfer Sequence

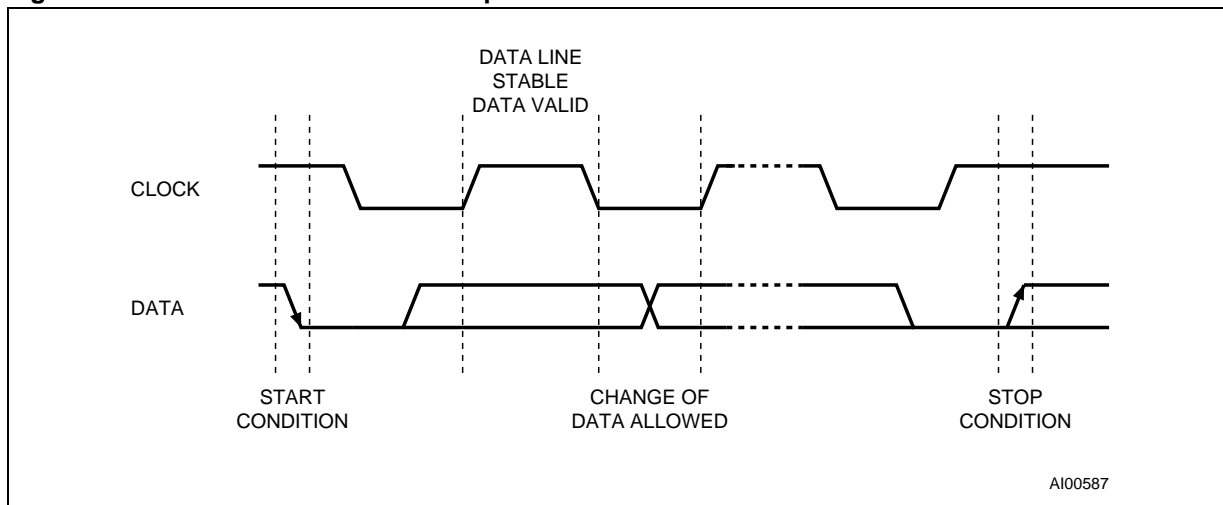


Figure 7. Acknowledgement Sequence

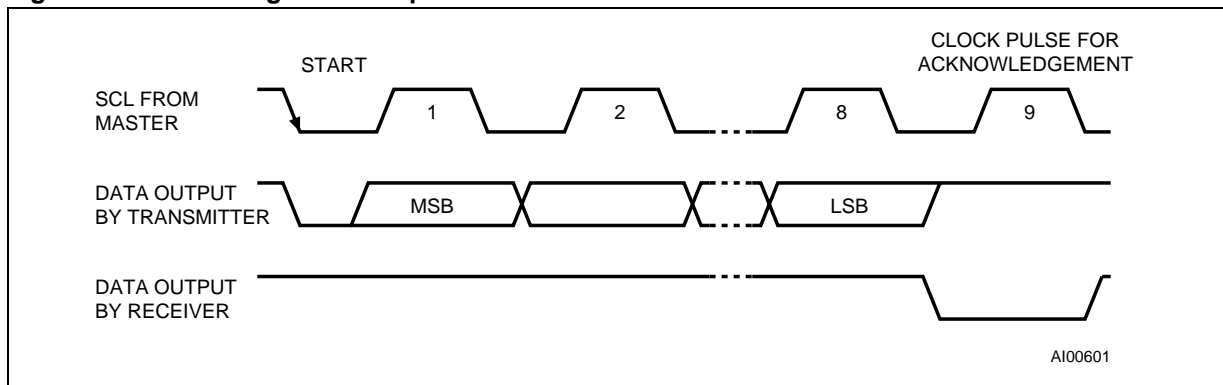


Figure 8. Bus Timing Requirements Sequence

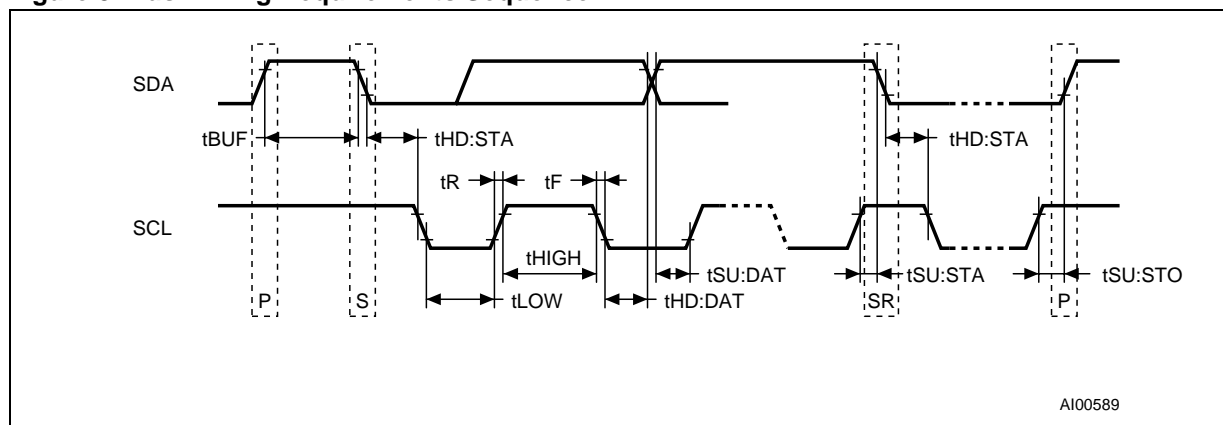


Table 7. AC Characteristics

| Sym | Parameter ⁽¹⁾ | Min | Typ | Max | Units |
|------------------------------------|---|-----|-----|-----|-------|
| f _{SCL} | SCL Clock Frequency | 0 | | 400 | kHz |
| t _{LOW} | Clock Low Period | 1.3 | | | μs |
| t _{HIGH} | Clock High Period | 600 | | | ns |
| t _R | SDA and SCL Rise Time | | | 300 | ns |
| t _F | SDA and SCL Fall Time | | | 300 | ns |
| t _{HD:STA} | START Condition Hold Time (after this period the first clock pulse is generated) | 600 | | | ns |
| t _{SU:STA} | START Condition Setup Time (only relevant for a repeated start condition) | 600 | | | ns |
| t _{SU:DAT} ⁽²⁾ | Data Setup Time | 100 | | | ns |
| t _{HD:DAT} | Data Hold Time | 0 | | | μs |
| t _{SU:STO} | STOP Condition Setup Time | 600 | | | ns |
| t _{BUF} | Time the bus must be free before a new transmission can start | 1.3 | | | μs |

Note: 1. Valid for Ambient Operating Temperature: T_A = -40 to 85°C; V_{CC} = 2.0 to 5.5V (except where noted).

2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.

READ Mode

In this mode the master reads the M41T80 slave after setting the slave address (see Figure 10, page 10). Following the WRITE Mode Control Bit (R/W=0) and the Acknowledge Bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ Mode Control Bit (R/W=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an Acknowledge Bit to the slave transmitter. The address pointer is only incremented on reception of an Acknowledge Clock. The M41T80 slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to "An+2."

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a Stop Condition or when the pointer increments to any non-clock address (08h-13h).

Note: This is true both in READ Mode and WRITE Mode.

An alternate READ Mode may also be implemented whereby the master reads the M41T80 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see Figure 11, page 11).

Figure 9. Slave Address Location

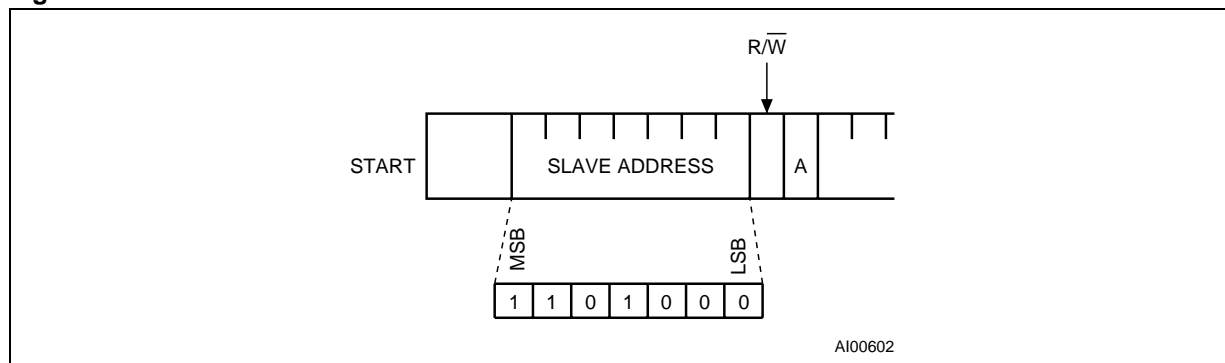


Figure 10. READ Mode Sequence

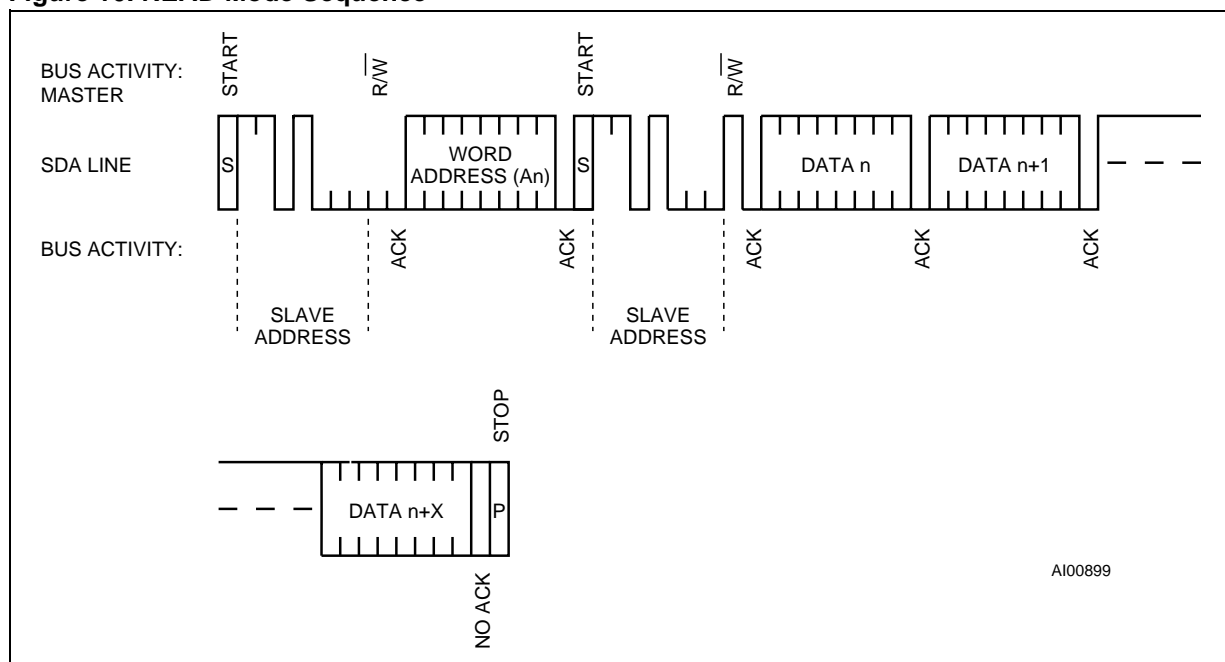
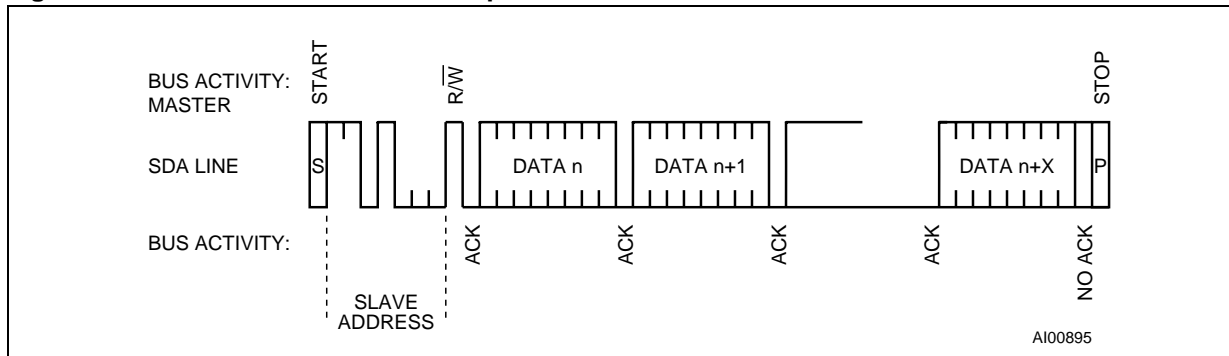


Figure 11. Alternative READ Mode Sequence

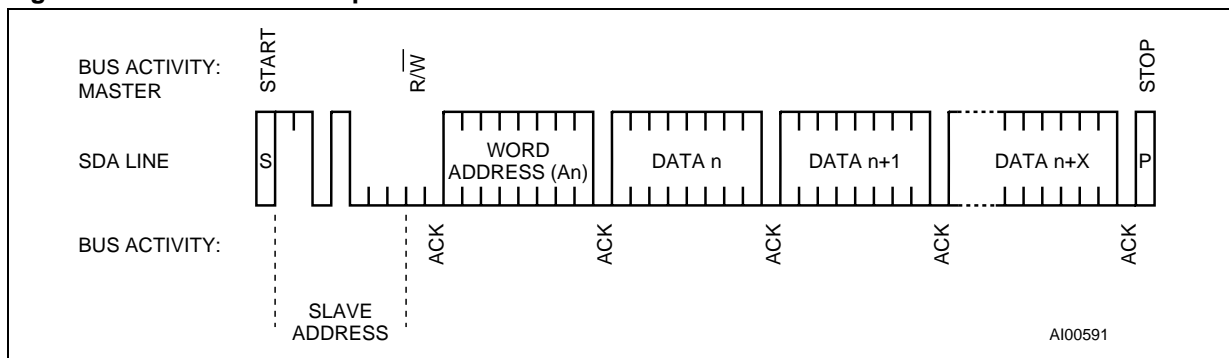


WRITE Mode

In this mode the master transmitter transmits to the M41T80 slave receiver. Bus protocol is shown in Figure 12, page 11. Following the START condition and slave address, a logic '0' (R/W=0) is placed on the bus and indicates to the addressed device that word address "An" will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next

and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T80 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see Figure 9, page 10 and again after it has received the word address and each data byte.

Figure 12. WRITE Mode Sequence



CLOCK OPERATION

The M41T80 is driven by a quartz-controlled oscillator with a nominal frequency of 32,768Hz. The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The 20-byte Register Map (see Table 8, page 13) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/Hundredths of Seconds, Seconds, Minutes, and Hours are contained within the first four registers.

Note: A WRITE to any clock register will result in the Tenths/Hundredths of Seconds being reset to "00," and Tenths/Hundredths of Seconds cannot be written to any value other than "00."

Bits D6 and D7 of Clock Register 03h (Century/Hours Register) contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of Register 04h contain the Day (day of week). Registers 05h, 06h, and 07h contain the Date (day of month), Month and Years. The ninth clock register is the Control Register. Bit D7 of Register 01h contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain.

When reset to a '0' the oscillator restarts within four seconds (typically one second).

The eight Clock Registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

TIMEKEEPER® Registers

The M41T80 offers 20 internal registers which contain Clock, Alarm, 32kHz, Flag, Square Wave, and Control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to any non-clock address (08h-13h).

TIMEKEEPER and Alarm Registers store data in BCD. Control, 32kHz, and Square Wave Registers store data in Binary Format.

Table 8. TIMEKEEPER® Register Map

| Addr | | | | | | | | | Function/Range BCD Format | |
|------|-------------|------------------|------------|--------|------------------------|-------------|----|----|---------------------------|-----------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 00h | 0.1 Seconds | | | | 0.01 Seconds | | | | 10s/100s of Seconds | 00-99 |
| 01h | ST | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 02h | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 03h | CEB | CB | 10 Hours | | Hours (24 Hour Format) | | | | Century/Hours | 0-1/00-23 |
| 04h | 0 | 0 | 0 | 0 | 0 | Day of Week | | | Day | 01-7 |
| 05h | 0 | 0 | 10 Date | | Date: Day of Month | | | | Date | 01-31 |
| 06h | 0 | 0 | 0 | 10M | Month | | | | Month | 01-12 |
| 07h | 10 Years | | | | Year | | | | Year | 00-99 |
| 08h | OUT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Control | |
| 09h | 32kE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 32kHz | |
| 0Ah | AFE | SQWE | 0 | AI 10M | Alarm Month | | | | AI Month | 01-12 |
| 0Bh | RPT4 | RPT5 | AI 10 Date | | Alarm Date | | | | AI Date | 01-31 |
| 0Ch | RPT3 | 0 | AI 10 Hour | | Alarm Hour | | | | AI Hour | 00-23 |
| 0Dh | RPT2 | Alarm 10 Minutes | | | Alarm Minutes | | | | AI Min | 00-59 |
| 0Eh | RPT1 | Alarm 10 Seconds | | | Alarm Seconds | | | | AI Sec | 00-59 |
| 0Fh | 0 | AF | 0 | 0 | 0 | 0 | 0 | 0 | Flags | |
| 10h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reserved | |
| 11h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reserved | |
| 12h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reserved | |
| 13h | RS3 | RS2 | RS1 | RS0 | 0 | 0 | 0 | 0 | SQW | |

Keys: ST = Stop Bit
0 = Must be set to '0'
32kE = 32kHz Enable Bit
CEB = Century Enable Bit
CB = Century Bit
OUT = Output level

AFE = Alarm Flag Enable Flag
RPT1-RPT5 = Alarm Repeat Mode Bits
AF = Alarm Flag (Read only)
SQWE = Square Wave Enable
RS0-RS3 = SQW Frequency

Setting Alarm Clock Registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every year, month, day, hour, minute, or second.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. Table 9, page 14 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set (and SQWE is '0.'),

the alarm condition activates the $\overline{\text{IRQ}}/\text{OUT}/\text{SQW}$ pin.

Note: If the address pointer is allowed to increment to the Flag Register address, an alarm condition will not cause the Interrupt/Flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "Alarm Seconds," the address pointer will increment to the Flag address, causing this situation to occur.

The $\overline{\text{IRQ}}/\text{OUT}/\text{SQW}$ output is cleared by a READ to the Flags Register as shown in Figure 13. A subsequent READ of the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'

Figure 13. Alarm Interrupt Reset Waveform

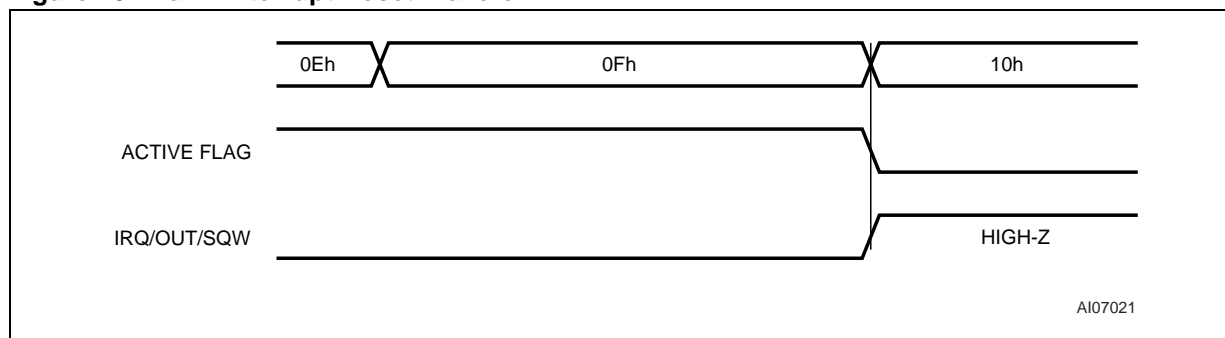


Table 9. Alarm Repeat Modes

| RPT5 | RPT4 | RPT3 | RPT2 | RPT1 | Alarm Setting |
|------|------|------|------|------|-----------------|
| 1 | 1 | 1 | 1 | 1 | Once per Second |
| 1 | 1 | 1 | 1 | 0 | Once per Minute |
| 1 | 1 | 1 | 0 | 0 | Once per Hour |
| 1 | 1 | 0 | 0 | 0 | Once per Day |
| 1 | 0 | 0 | 0 | 0 | Once per Month |
| 0 | 0 | 0 | 0 | 0 | Once per Year |

Table 10. Square Wave Output Frequency

| Square Wave Bits | | | | Square Wave | |
|------------------|-----|-----|-----|-------------|-------|
| RS3 | RS2 | RS1 | RS0 | Frequency | Units |
| 0 | 0 | 0 | 0 | None | - |
| 0 | 0 | 0 | 1 | 32.768 | kHz |
| 0 | 0 | 1 | 0 | 8.192 | kHz |
| 0 | 0 | 1 | 1 | 4.096 | kHz |
| 0 | 1 | 0 | 0 | 2.048 | kHz |
| 0 | 1 | 0 | 1 | 1.024 | kHz |
| 0 | 1 | 1 | 0 | 512 | Hz |
| 0 | 1 | 1 | 1 | 256 | Hz |
| 1 | 0 | 0 | 0 | 128 | Hz |
| 1 | 0 | 0 | 1 | 64 | Hz |
| 1 | 0 | 1 | 0 | 32 | Hz |
| 1 | 0 | 1 | 1 | 16 | Hz |
| 1 | 1 | 0 | 0 | 8 | Hz |
| 1 | 1 | 0 | 1 | 4 | Hz |
| 1 | 1 | 1 | 0 | 2 | Hz |
| 1 | 1 | 1 | 1 | 1 | Hz |

Full-time 32kHz Square Wave Output

The M41T80 offers the user a special 32kHz square wave function which defaults to output on the F_{32k} pin (Pin 3) as long as V_{CC} is valid, and the oscillator is running (ST Bit = '0'). This function is available within four seconds of initial power-up and can only be disabled by setting the 32kE Bit to

'0' or the ST Bit to '1.' If not used, the F_{32k} pin should be disconnected and allowed to float.

Note: The F_{32k} pin is an open drain which requires an external pull-up resistor.

Century Bit

Bits D7 and D6 of Clock Register 03h contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

Output Driver Pin

When the AFE Bit and SQWE Bit are not set, the $\overline{\text{IRQ/OUT/SQW}}$ pin becomes an output driver that reflects the contents of D7 of the Control Register. In other words, when D7 (OUT Bit) of address lo-

cation 08h is a '0,' then the $\overline{\text{IRQ/OUT/SQW}}$ pin will be driven low.

Note: The $\overline{\text{IRQ/OUT/SQW}}$ pin is an open drain which requires an external pull-up resistor.

Preferred Power-on Default

When powering the device up from ground (0V), the following register bits are set to a '0' state: ST; AFE; and SQWE. The following bits are set to a '1' state: OUT and 32kE (see Table 11, page 16).

Table 11. Preferred Power-on Default Values

| Condition | ST | Out | AFE | SQWE | 32kE |
|-------------------------|----|-----|-----|------|------|
| Power-up ⁽¹⁾ | 0 | 1 | 0 | 0 | 1 |

Note: 1. If V_{CC} falls to a voltage, $0V < V_{CC} < 2.0V$, these bits should be rewritten by the user.

PART NUMBERING

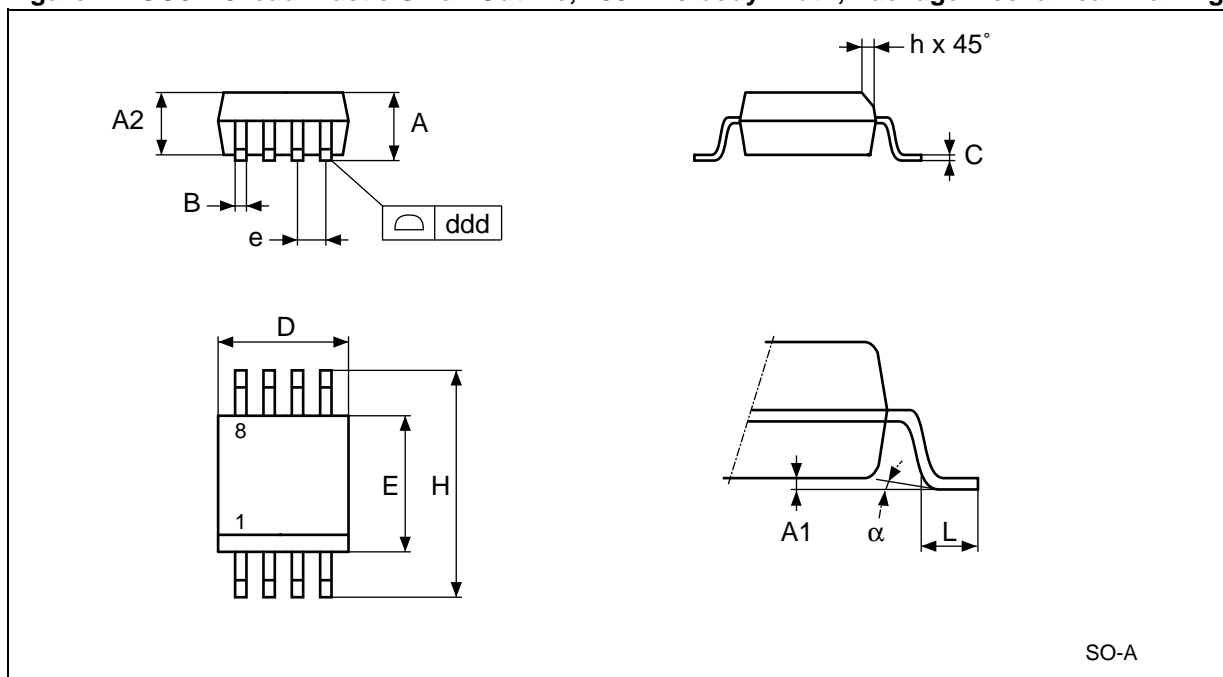
Table 12. Ordering Information Scheme

| Example: | M41T | 80 | M | 6 | TR |
|---|------|-------------------------------|---------|-------------------------------------|-----------------------------------|
| Device Type | M41T | | | | |
| Supply Voltage and Write Protect Voltage | | 80 = $V_{CC} = 2.0$ to $5.5V$ | | | |
| Package | | | M = SO8 | | |
| Temperature Range | | | | 6 = $-40^{\circ}C$ to $85^{\circ}C$ | |
| Shipping Method for SOIC | | | | | blank = Tubes TR = Tape & Reel |

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

PACKAGE MECHANICAL INFORMATION

Figure 14. SO8 – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Drawing



Note: Drawing is not to scale.

Table 13. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

| Symb | mm | | | inches | | |
|------|------|------|------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | – | 1.35 | 1.75 | – | 0.053 | 0.069 |
| A1 | – | 0.10 | 0.25 | – | 0.004 | 0.010 |
| B | – | 0.33 | 0.51 | – | 0.013 | 0.020 |
| C | – | 0.19 | 0.25 | – | 0.007 | 0.010 |
| D | – | 4.80 | 5.00 | – | 0.189 | 0.197 |
| ddd | – | – | 0.10 | – | – | 0.004 |
| E | – | 3.80 | 4.00 | – | 0.150 | 0.157 |
| e | 1.27 | – | – | 0.050 | – | – |
| H | – | 5.80 | 6.20 | – | 0.228 | 0.244 |
| h | – | 0.25 | 0.50 | – | 0.010 | 0.020 |
| L | – | 0.40 | 0.90 | – | 0.016 | 0.035 |
| α | – | 0° | 8° | – | 0° | 8° |
| N | 8 | | | 8 | | |

REVISION HISTORY

Table 14. Document Revision History

| Date | Rev. # | Revision Details |
|--------------|--------|------------------|
| October 2002 | 1.0 | First Issue |

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