ST10F168

16-Bit MCU With 256K Byte Flash and 8K Byte RAM Memories

ERRATA SHEET - REVISION BB

1 - DESCRIPTION

This Errata Sheet describes the functional and electrical problems known.

The revision number BB can be found in the second line printed on the ST10F168 package. It looks like: XBB-XXXXXXX where "BB" identifies the revision number.

2 - FUNCTIONAL PROBLEMS

The following malfunctions are known in this device:

2.1 - ST_PWRDN.1 - Execution of PWRDN Instruction

When instruction PWRDN is executed while pin NMI is at a high level (if PWRDCFG bit is clear in SYSCON register) or while at least one P2 pin used to exit from power-down mode (if PWRDCFG bit is set in SYSCON register) is at the active level, power down mode should not be entered, and the PWRDN instruction should be ignored.

However, under the conditions described below, the PWRDN instruction may not be ignored, and no further instructions are fetched from external memory, i.e. the CPU is in a quasi-idle state. This problem will only occur in the following situations:

a) the instructions following the PWRDN instruction are located in an external memory, and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MT-TCx=0) is used.

b) the instruction preceeding the PWRDN instruction **writes** to external memory or an XPeripheral (XRAM, CAN), and the instructions following the PWRDN instruction are located in external memory. In this case, the problem will occur for any bus configuration.

Note The on-chip peripherals are still working correctly, in particular the Watchdog Timer, if not disabled, will reset the device upon an overflow. Interrupts and PEC transfers, however, can not be processed. In case NMI is asserted low while the device is in this quasi-idle state, power-down mode is entered.

No problem will occur if the NMI pin is low (if PWRDCFG = 0) or if all P2 pins used to exit from power-down mode are at inactive level (if PWRDCFG = 1): the chip will normally enter powerdown mode.

Workaround:

Ensure that no instruction which writes to external memory or an XPeripheral preceeds the PWRDN instruction, otherwise insert e.g. a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate waitstate is used, the PWRDN instruction should be executed from internal RAM or XRAM.

Summary of Remaining Functional Problems Known on the ST10F168-BB

Name	Short Description
ST_PWRDN.1	Powerdown mode not ignored

3 - DEVIATIONS FROM DC/AC PRELIMINARY SPECIFICATION

DC parameters

After characterization, the DC parameter of ALE active current has been changed: I_{ALEH} change from 500µA to 600µA.

Note on on-chip oscillator

The XTAL2 output is not designed to provide a valid signal when XTAL1 is supplied by an external clock signal. It may happen, if the external clock signal is not perfectly symetrical and centered on V_{DD} / 2, that XTAL2 signal is not equal to XTAL1. This is due to the design of the oscillator, which has a auto-adaptation gain control dedicated to external crystal.

If an external clock signal is directly provided on XTAL1 pin, then leave XTAL2 pin disconnected to achieve the lowest consumption of the on-chip oscillator.

4 - ERRATA SHEET VERSION INFORMATION

This document was released on the 23rd of May 2000. It reflects the current silicon status of the ST10F168BB revision and is only valid for this.