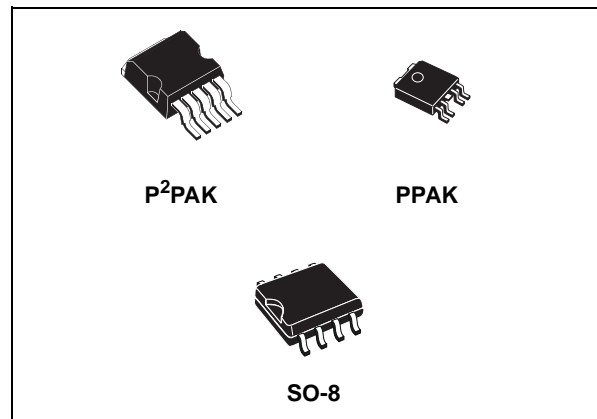


500mA SMART LDO

- GLITCH FREE TRANSITION BETWEEN INPUT SOURCES
- INTERNAL LOGIC SELECTS INPUT SOURCE
- GATE DRIVE FOR EXTERNAL PMOS BYPASS SWITCH
- 5V DETECTOR WITH HYSTERESIS
- 1% 3.3V REGULATED OUTPUT VOLTAGE
- 500mA GUARANTEED OUTPUT CURRENT
- OPERATING TEMPERATURE RANGE FROM 0°C TO 85°C
- AVAILABLE IN P²PAK PACKAGE
- PPAK AND SO-8 PACKAGES CAN BE AVAILABLE ON REQUEST



APPLICATIONS

- NETWORK INTERFACE CARDS
- PCMCIA/PCI INTERFACE CARDS
- DESKTOP COMPUTERS
- POWER SUPPLY WITH MULTIPLE INPUT SOURCES

DESCRIPTION

The ST1534A is intended for application such as power managed PCI and network interface cards (NICs), where operations from 3.3V VAUX supply

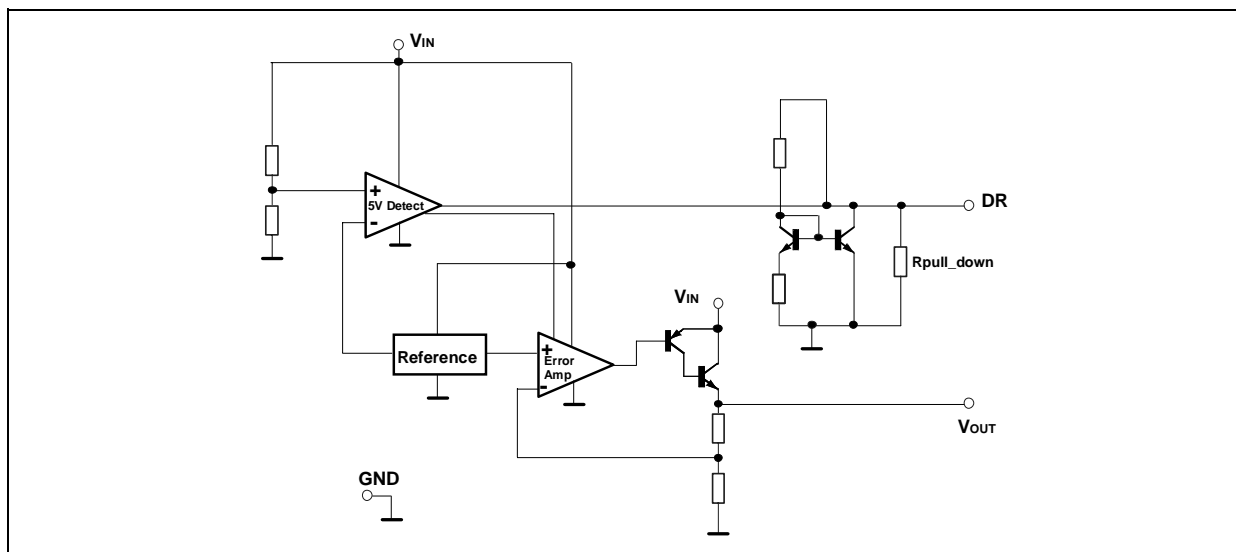
may be required when the 5V supply has been shut down.

During regular operation, 3.3V power for the PCI card is provided by the internal LDO regulator, generated from 5V supply. When the 5V V_{AUX} is available, the IC connects this supply directly to its output using an external P-Channel FET. This ensures an uninterrupted 3.3V out even if V_{IN} falls out of specification.

When both supplies are available simultaneously, the drive pin DR will be pulled high, turning off the PMOS switch.

The device is available in the popular 5 leads P²PAK and PPAK

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

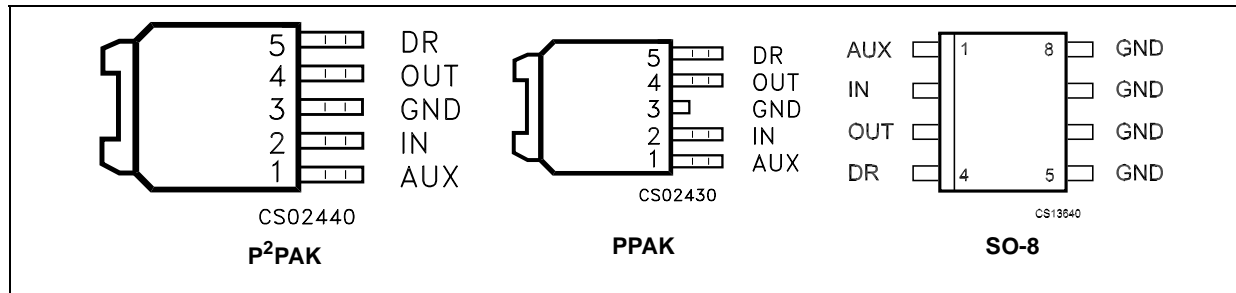
Symbol	Parameter ²	Value	Unit
V _I	DC Input Voltage	-0.3 to 7	V
V _{SHDN}	Shutdown Input Voltage	-0.3 to 7	V
I _O	Output Current	Internally limited	mA
T _{stg}	Storage Temperature Range	-40 to +125	°C
T _{op}	Operating Junction Temperature Range	0 to +85	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter	PPAK	P ² PAK	SO-8	Unit
R _{thj-case}	Thermal Resistance Junction-case	8	3	20	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	100	50	55	°C/W

CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

Pin PPAK/P ² PAK	Pin SO/8	Symbol	Name and Function
1	1	AUX	Auxiliary Input port typically 3.3V
2	2	IN	Input port typically 5V
3	5, 6, 7, 8	GND	Ground
4	3	OUT	LDO 3.3V Output Port
5	4	DR	Drive Output for external P-Channel MOSFET pass element

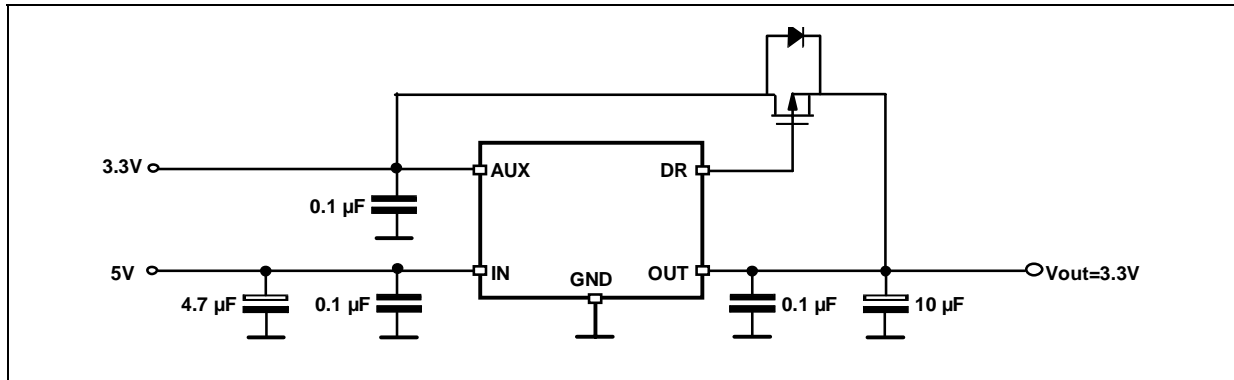
ORDERING INFORMATION

TYPE	PPAK (*)	P ² PAK (#)	SO-8 (*)
ST1534A	ST1534APT	ST1534AP2T	ST1534AD

(*) PPAK and SO-8 are available in Tape & Reel with the suffix "-TR".

(#) P²PAK is available in Tape & Reel with the suffix "-R".

TYPICAL APPLICATION CIRCUIT



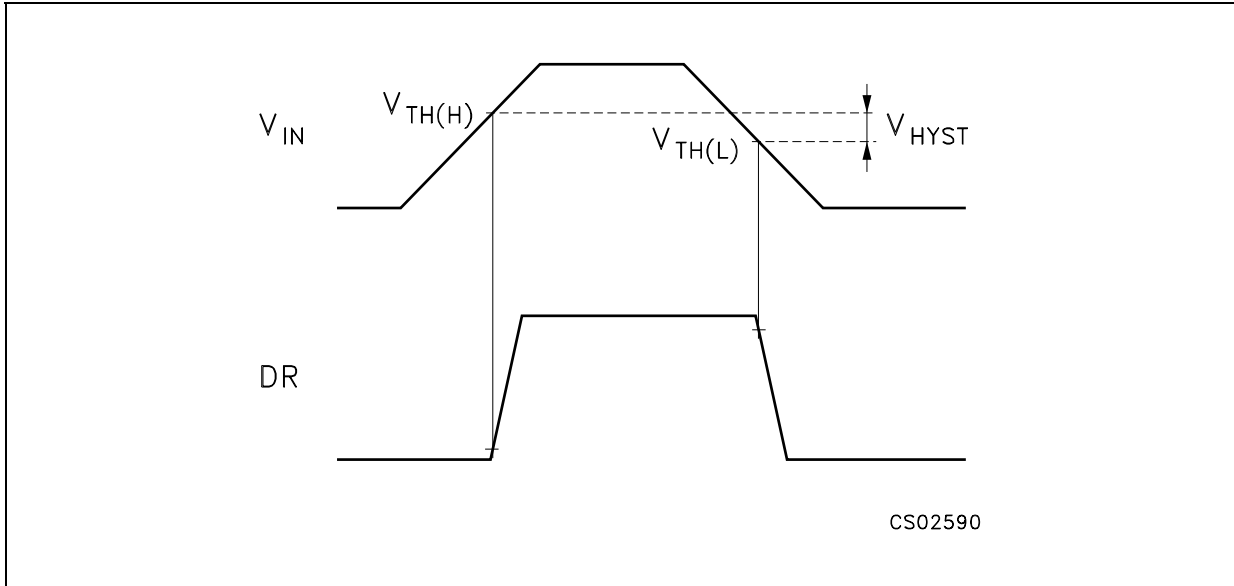
ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, $V_I = 5\text{V}$, $V_{\text{AUX}} = 3.3\text{V}$, $I_O = 10\text{mA}$, $C_O = 2.2\mu\text{F}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Input Voltage Range		4.5	5	5.5	V
I_{IN}	Input Supply Current	$V_I \geq 4.5\text{V}$ $I_O = 0\text{mA}$ $V_{\text{AUX}} = 0\text{V}$		11		mA
		$V_I \geq 4.5\text{V}$ $I_O = 0\text{mA}$ $V_{\text{AUX}} = 3.3\text{V}$		11		mA
		$V_I < 4.1\text{V}$ $I_O = 0\text{mA}$ $V_{\text{AUX}} = 0\text{V}$		2		mA
		$V_I < 4.1\text{V}$ $I_O = 0\text{mA}$ $V_{\text{AUX}} = 3.3\text{V}$		2		mA
I_{AUX}	Auxiliary Supply Current	$V_I = 0\text{V}$		2.2		mA
		$V_I = 5\text{V}$		200		μA
3.3V VOLTAGE REGULATOR BLOCK						
V_O	Output Voltage	$T_j = 0$ to 85°C	3.18	3.3	3.42	V
ΔV_O	Line Regulation	$V_I = 4.5$ to 5.5V		0.04	0.5	%
ΔV_O	Load Regulation	$I_O = 0$ to 500mA		0.1	1	%
V_d	Dropout Voltage	$I_O = 500\text{mA}$ $T_j = 0$ to 85°C			1.15	V
I_O	Output Current Limit	$T_j = 0$ to 85°C	550			mA
5V DETECT BLOCK						
V_{THL}	Low Threshold Voltage	V_I falling, $I_O = 500\text{mA}$ $T_j = 0$ to 85°C	4.15		4.3	V
V_{HYST}	Hysteresis		70		200	mV
DRIVE OUTPUT BLOCK						
V_{DR}	Drive Output Voltage	$V_I = 4.5$ to 5.5V $I_{\text{DR}} = 200\mu\text{A}$	3.6	$V_{\text{IN}} - 0.8$		V
		$V_I < 4.15\text{V}$ $I_{\text{DR}} = 200\mu\text{A}$		100	200	mV
I_{DR}	Drive Current	Sinking: $V_I = 4.15\text{V}$ $V_{\text{DR}} = 1\text{V}$	7	20		mA
		Sourcing: $V_I = 4.5\text{V}$ $V_I - V_{\text{DR}} = 2\text{V}$	7	25		mA
t_{DH}	Drive High Delay (Note 1 and 2)	$C_{\text{DR}} = 1.2\text{nF}$, V_{IN} ramping up, measured from $V_I = V_{\text{TH(H)}}$ to $V_{\text{DR}} = 3.3\text{V}$ $T_j = 0$ to 85°C		2	5	μs
t_{DL}	Drive Low Delay (Note 1 and 2)	$C_{\text{DR}} = 1.2\text{nF}$, V_{IN} ramping down, measured from $V_I = V_{\text{TH(L)}}$ to $V_{\text{DR}} = 200\text{mV}$ $T_j = 0$ to 85°C		3	6	μs

Note 1: Guaranteed by design

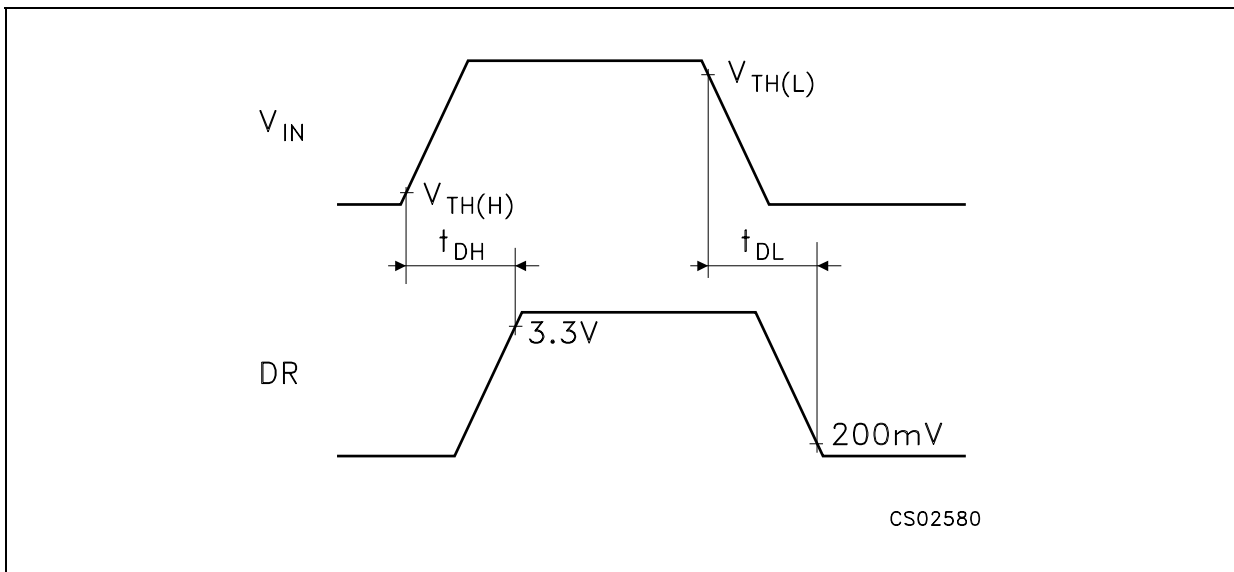
Note 2: See timing diagram

5V DETECT THRESHOLDS



V_{IN} rise and fall times (10% to 90%) to be $> 100\mu s$

TIMING DIAGRAM



V_{IN} rise and fall times (10% to 90%) to be $> 100\mu s$

TYPICAL CHARACTERISTICS (unless otherwise specified $T_j = 25^\circ\text{C}$)

Figure 1 : Supply Current vs Temperature

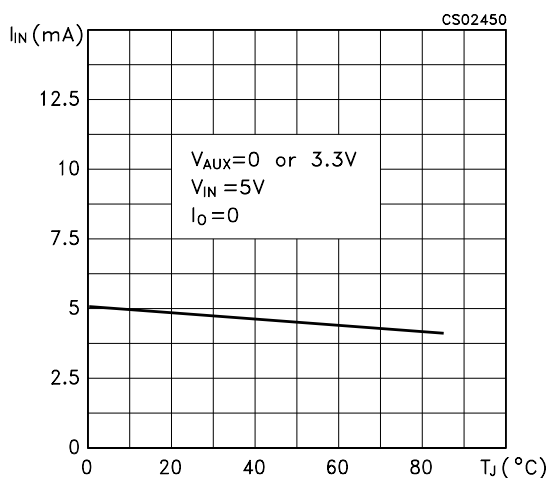


Figure 2 : Aux Current vs Temperature

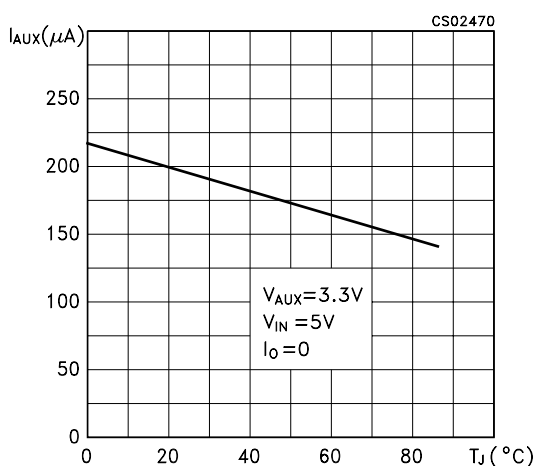


Figure 3 : Drive Current vs Temperature

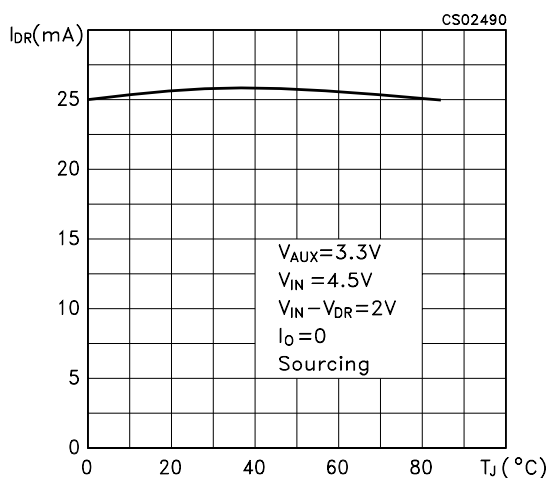


Figure 4 : Aux Current vs Temperature

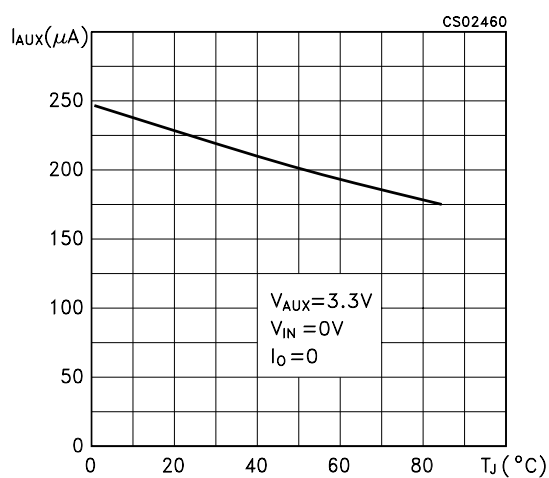


Figure 5 : Drive Output Voltage vs Temperature

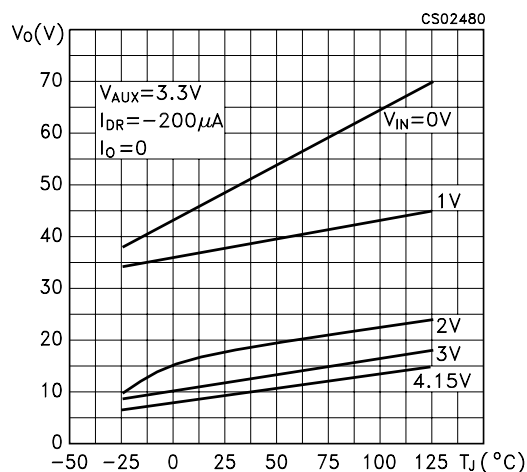


Figure 6 : Drive Current vs $V_{IN}-V_{DR}$

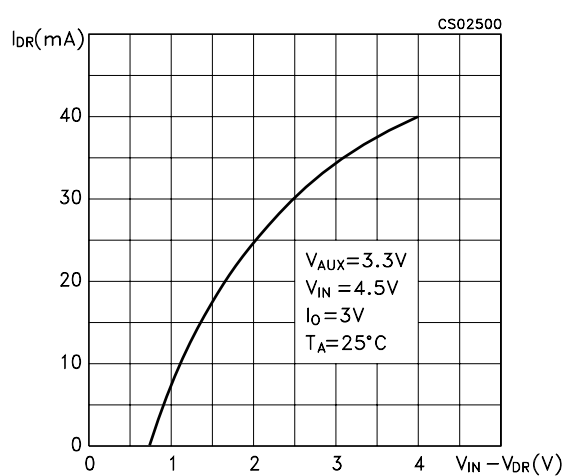


Figure 7 : Drive Current vs Temperature

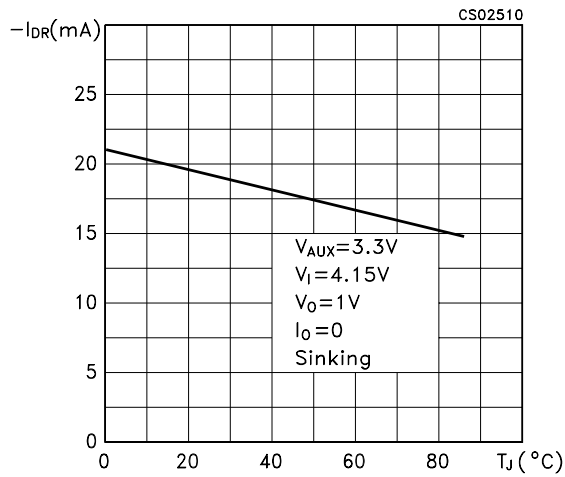


Figure 10 : Output Voltage vs Temperature

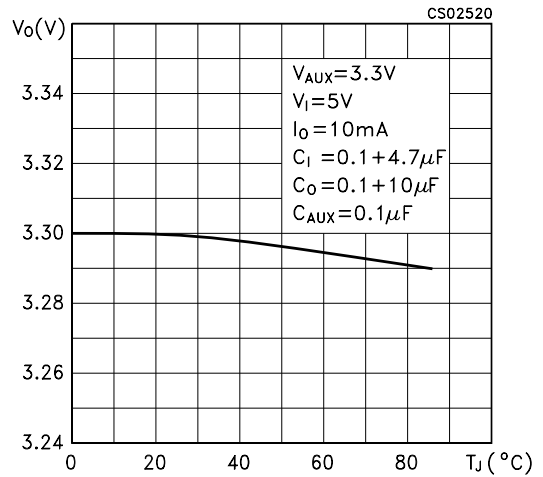


Figure 8 : Line Regulation vs Temperature

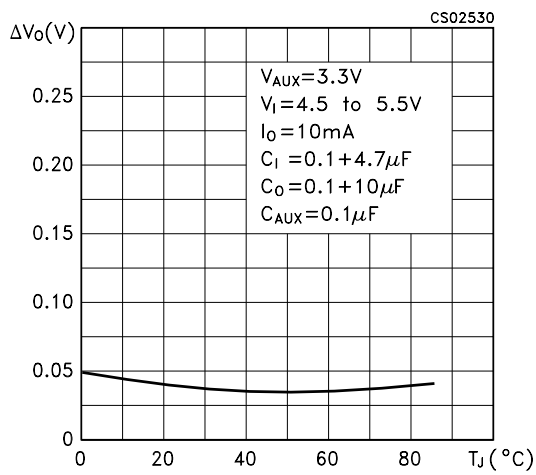


Figure 11 : Load Regulation vs Temperature

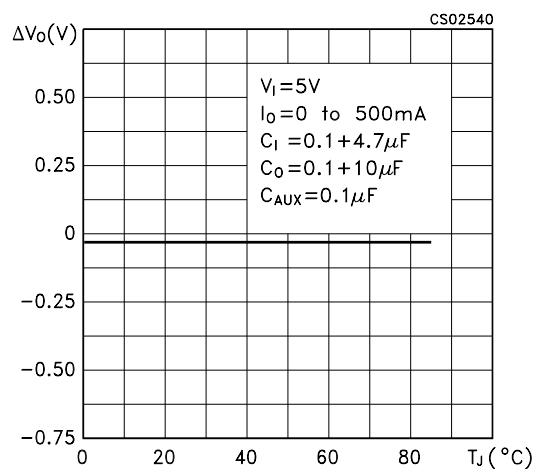


Figure 9 : Output Voltage vs Input Voltage

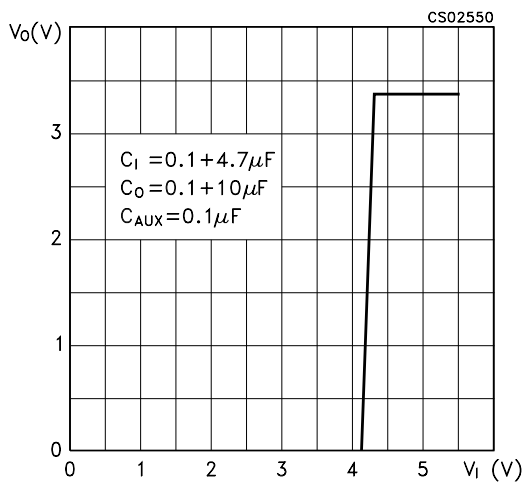


Figure 12 : Threshold Voltage vs Temperature

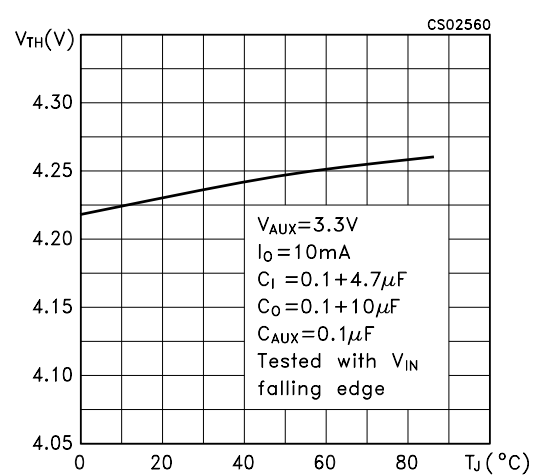


Figure 13 : Hysteresis vs Temperature

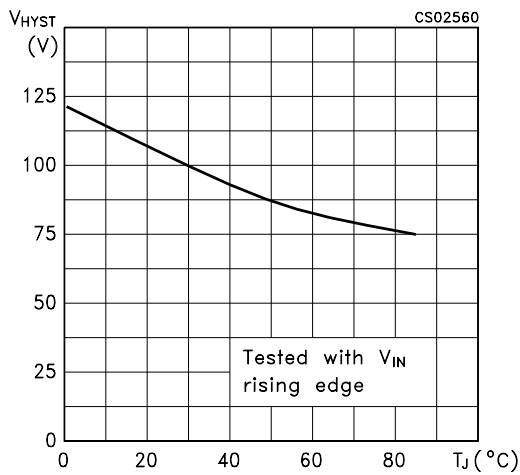
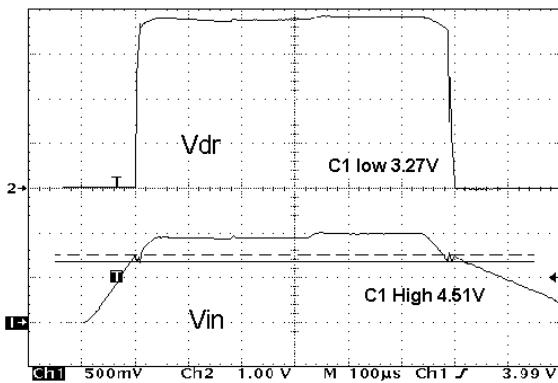
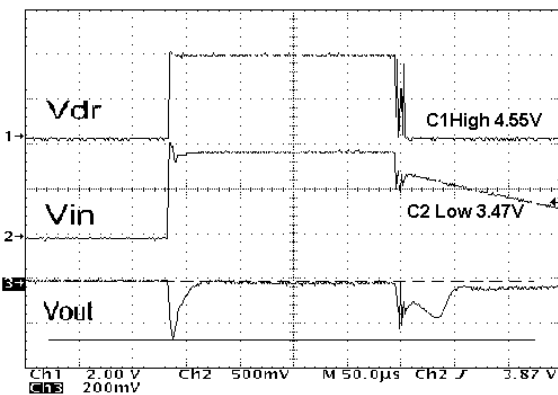


Figure 14 : Threshold



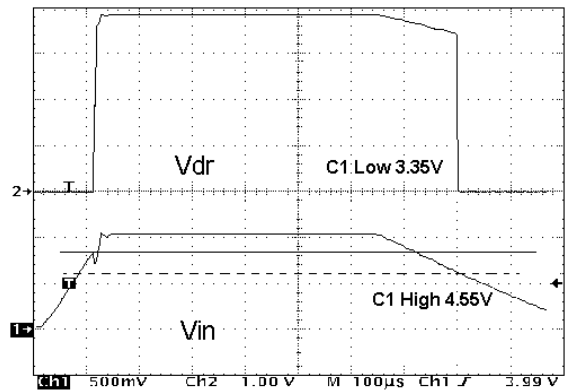
$V_I=3.5$ to $4.5V$, $t_s=t_f>100\mu s$, $I_O=500mA$, $C_I=0.1+4.7\mu F$, $C_O=33+0.1\mu F$

Figure 15 : Glitch



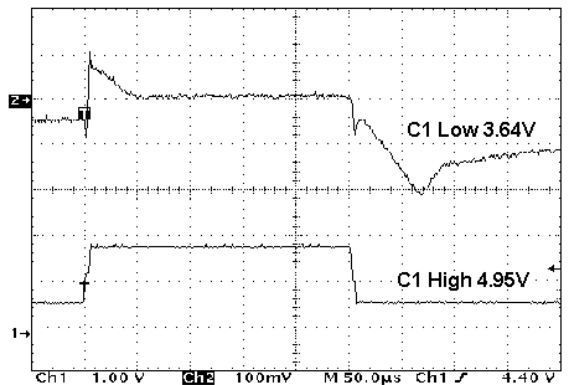
$V_I=3.5$ to $5V$, $I_O=500mA$, $C_O=33+0.1\mu F$, with P-Channel

Figure 16 : Threshold



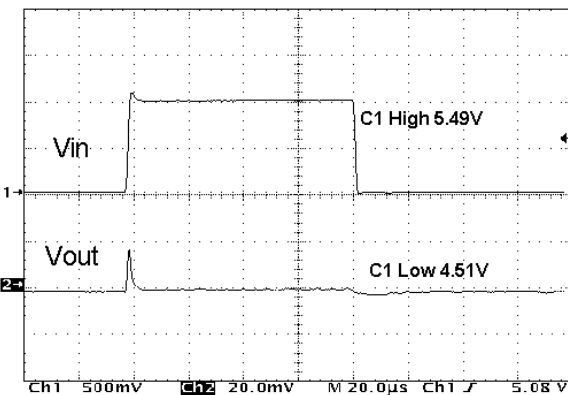
$V_I=3.5$ to $4.5V$, $t_s=t_f>100\mu s$, No Load $C_I=0.1+4.7\mu F$, $C_O=33+0.1\mu F$

Figure 17 : Glitch



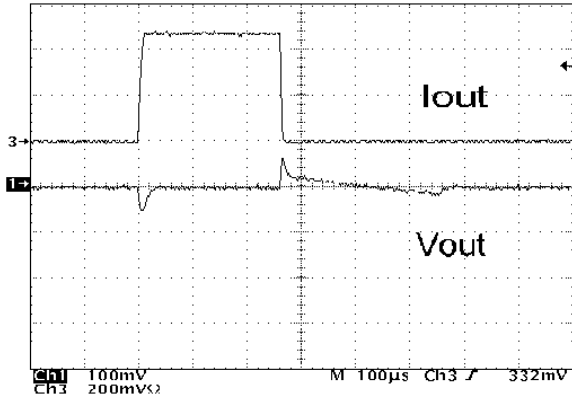
$V_I=3.5$ to $5V$, $I_O=500mA$, $C_O=33+0.1\mu F$, with P-Channel

Figure 18 : Line Transient



$V_I=4.5$ to $5.5V$, $I_O=10mA$, $C_I=0.1+4.7\mu F$, $C_O=33+0.1\mu F$, $C_{AUX}=0.1\mu F$

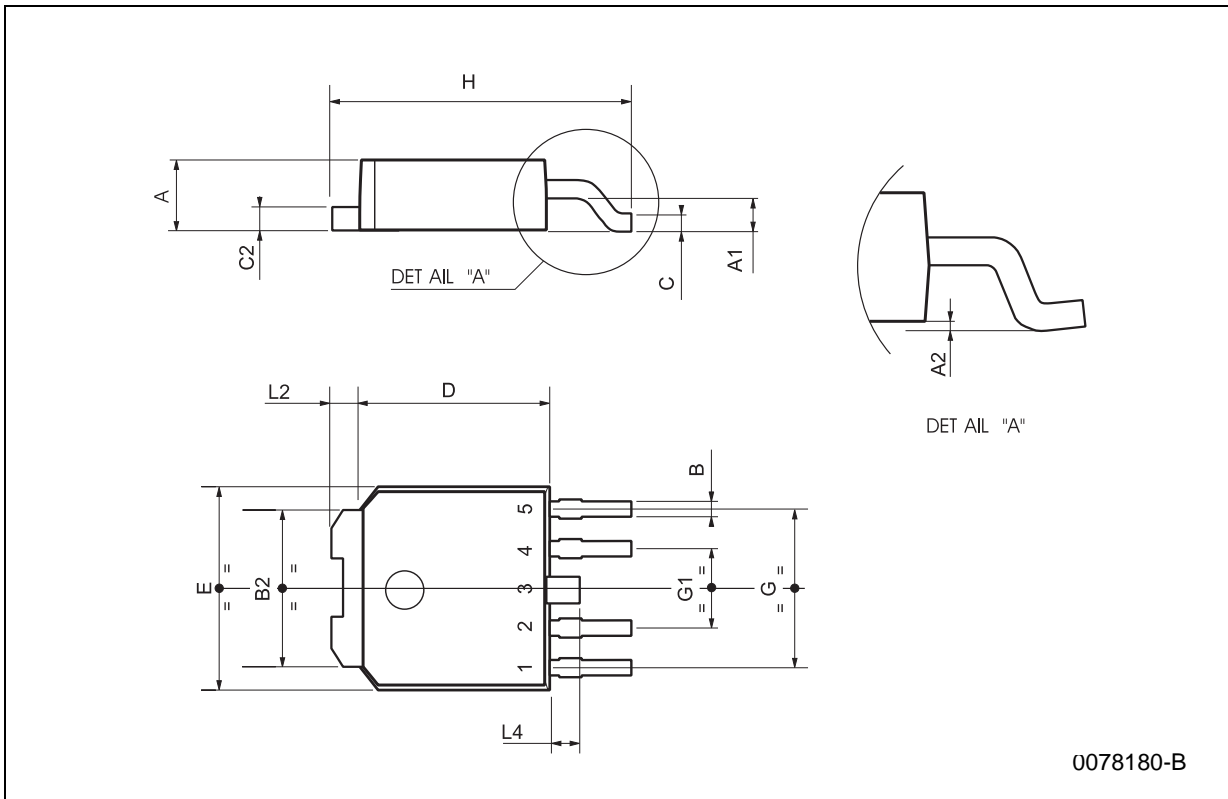
Figure 19 : Load Transient



$V_I=5\text{ V}$, $I_O=0\text{ to }500\text{mA}$, $C_I=4.7+0.1\mu\text{F}$, $C_O=0.1+33\mu\text{F}$, $C_{AUX}=0.1\mu\text{F}$

PPAK MECHANICAL DATA

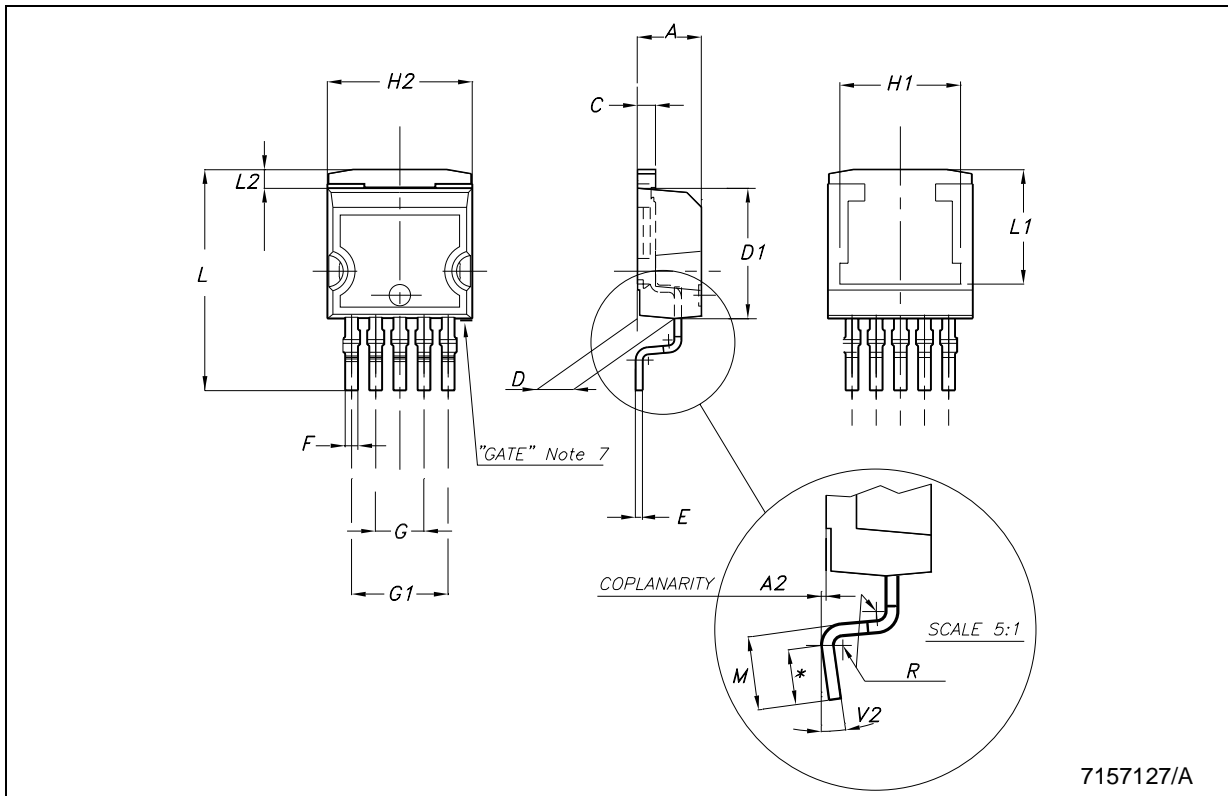
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



0078180-B

P²PAK/A MECHANICAL DATA

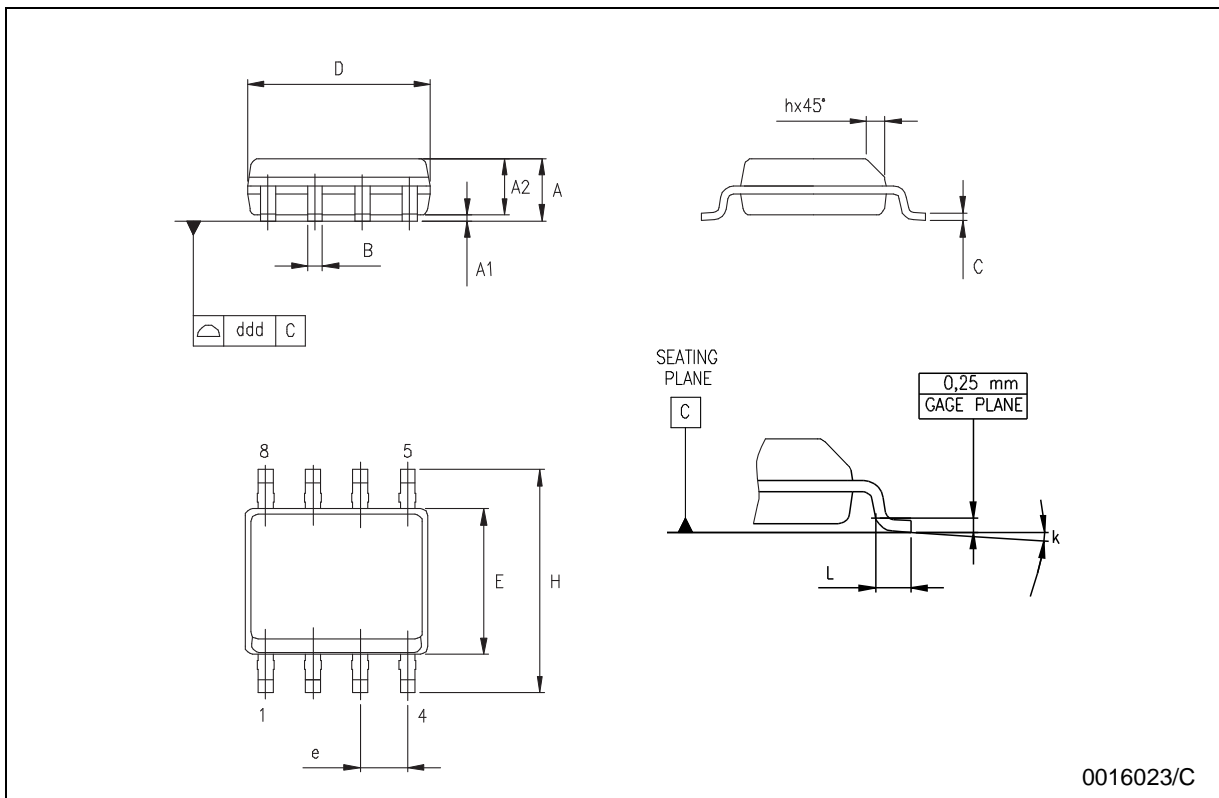
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.30		4.80	0.169		0.188
A2	0.03		0.23	0.001		0.009
C	1.17		1.37	0.046		0.053
D	2.40		2.80	0.094		0.110
D1	8.95		9.35	0.352		0.368
E	0.45		0.60	0.017		0.023
F	0.80		1.05	0.031		0.041
G	3.20		3.60	0.126		0.142
G1	6.60		7.00	0.260		0.275
H1		8.5			0.334	0.409
H2	10.00		10.40	0.393		0.409
L	15		15.85	0.590		0.624
L1		8			0.315	
L2	1.27		1.40	0.050		0.055
M	2.4		3.2	0.094		0.126
R		0.40			0.016	
V2	0°		8°	0°		8°



7157127/A

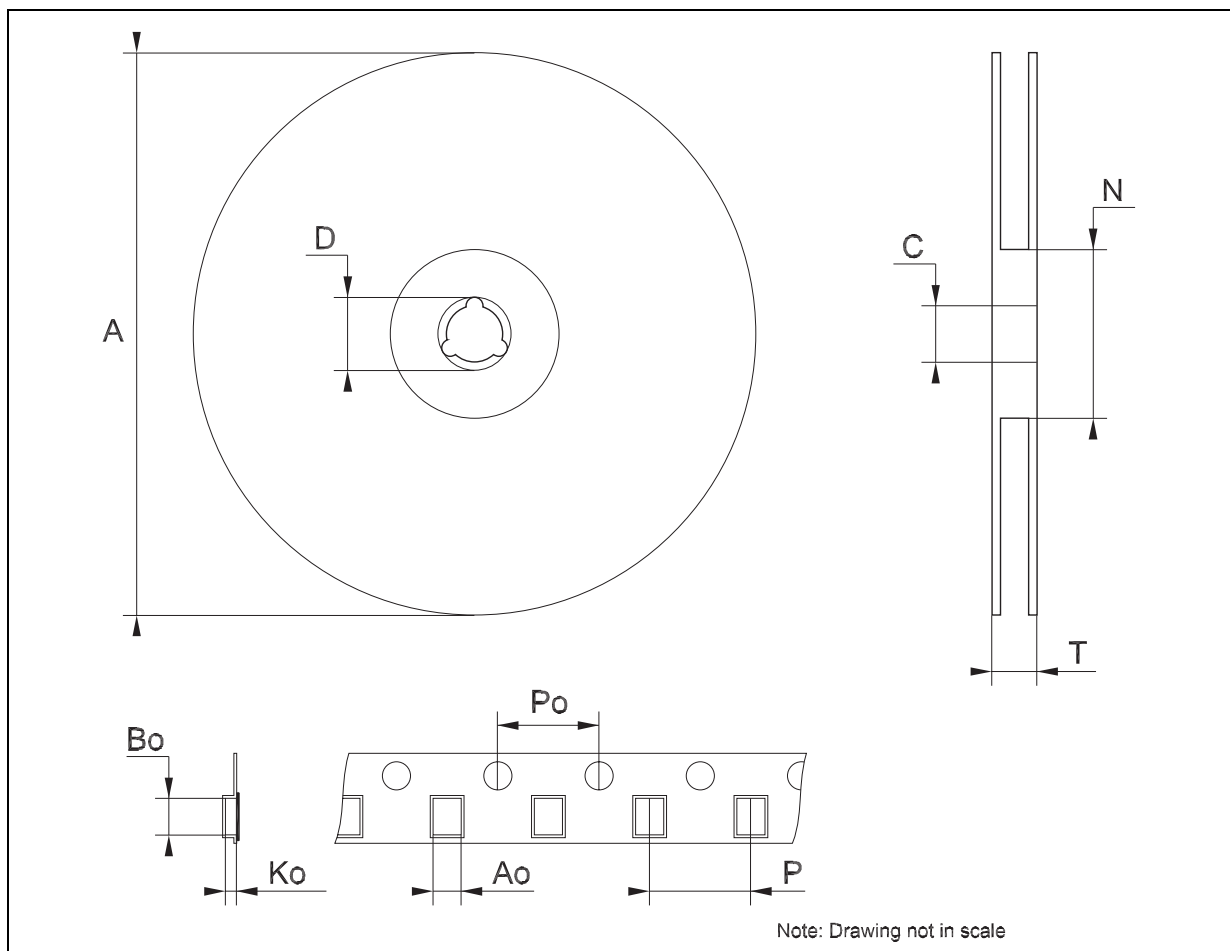
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



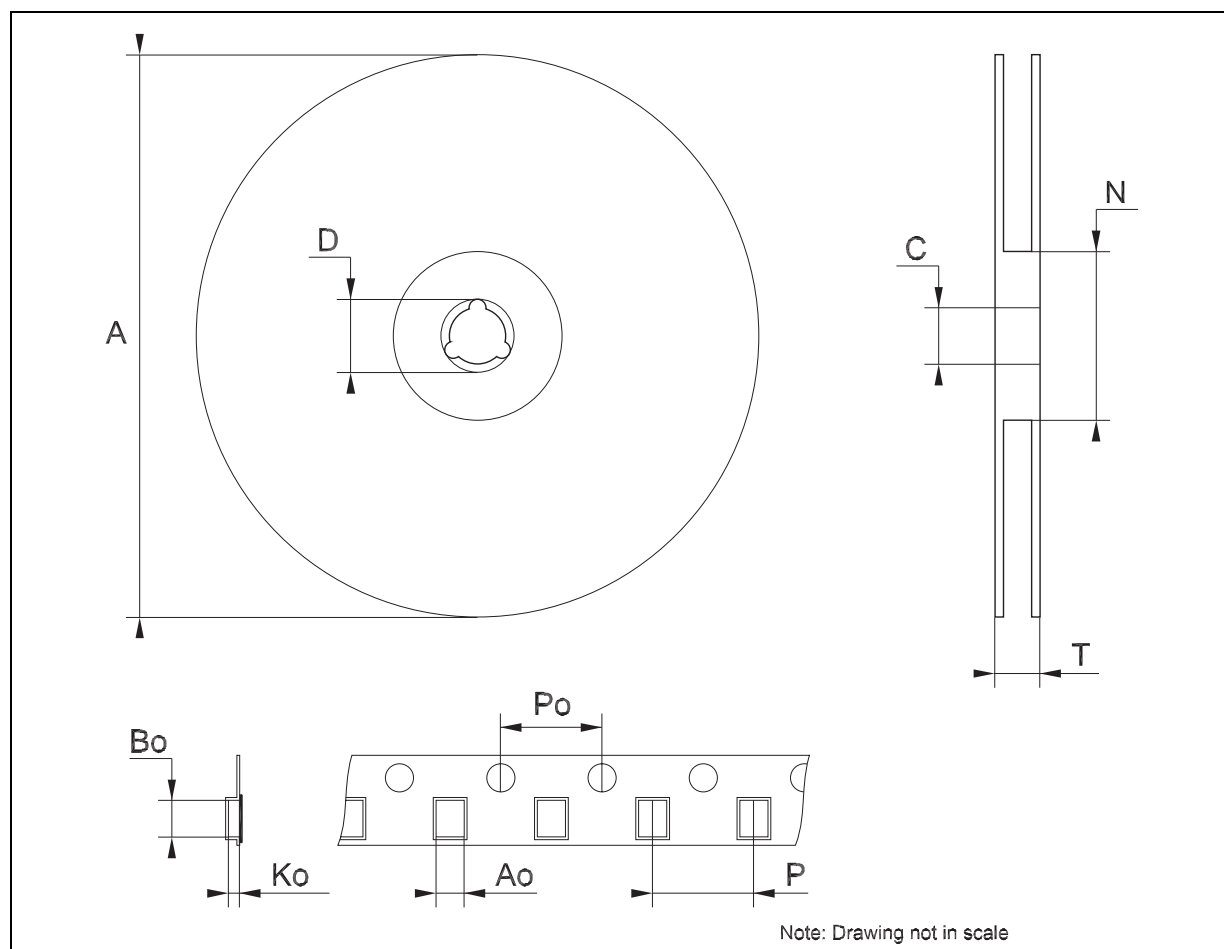
Tape & Reel DPAK-PPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	6.80	6.90	7.00	0.268	0.272	0.276
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



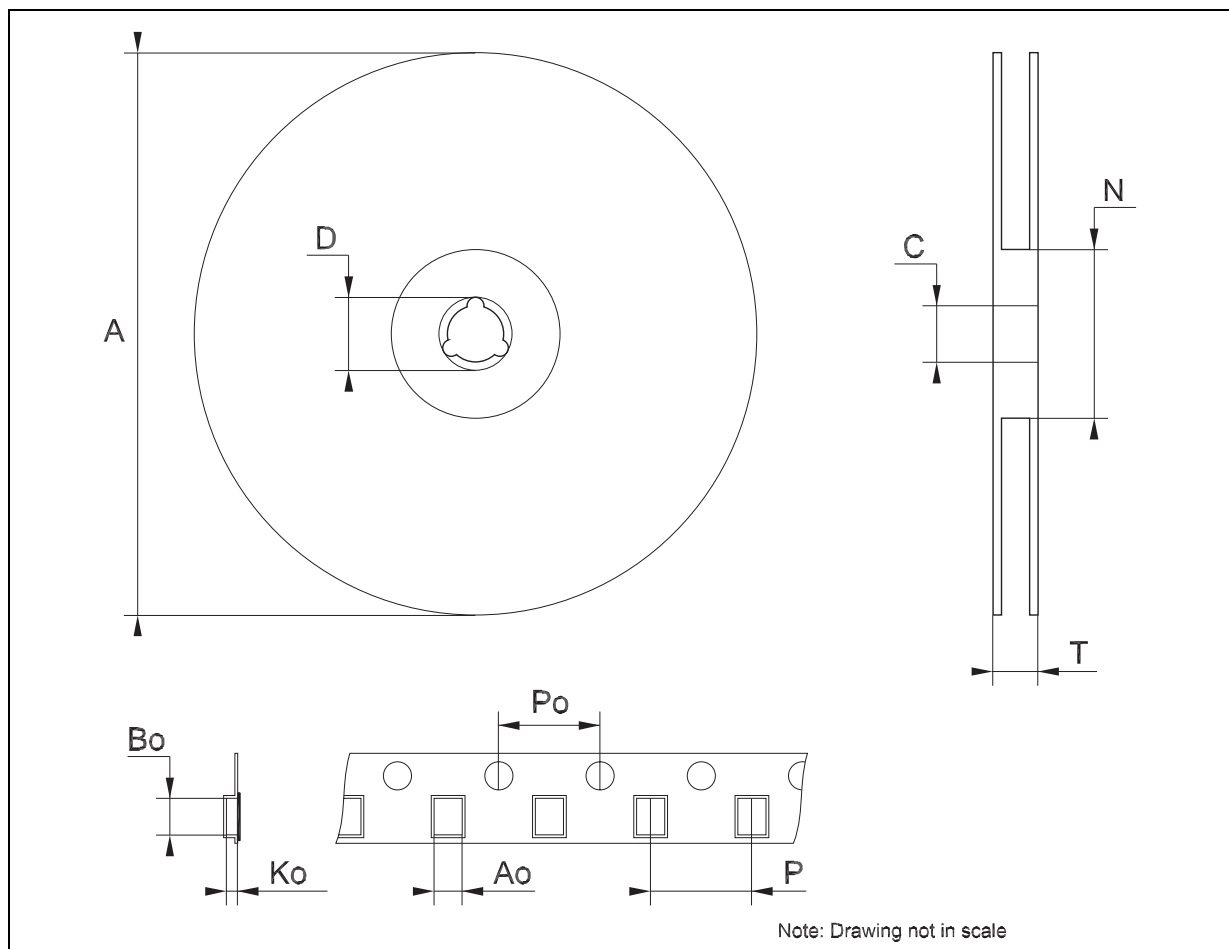
Tape & Reel D²PAK-P²PAK-D²PAK/A-P²PAK/A MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	10.50	10.6	10.70	0.413	0.417	0.421
Bo	15.70	15.80	15.90	0.618	0.622	0.626
Ko	4.80	4.90	5.00	0.189	0.193	0.197
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	11.9	12.0	12.1	0.468	0.472	0.476



Tape & Reel SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



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