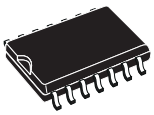
ST3M01

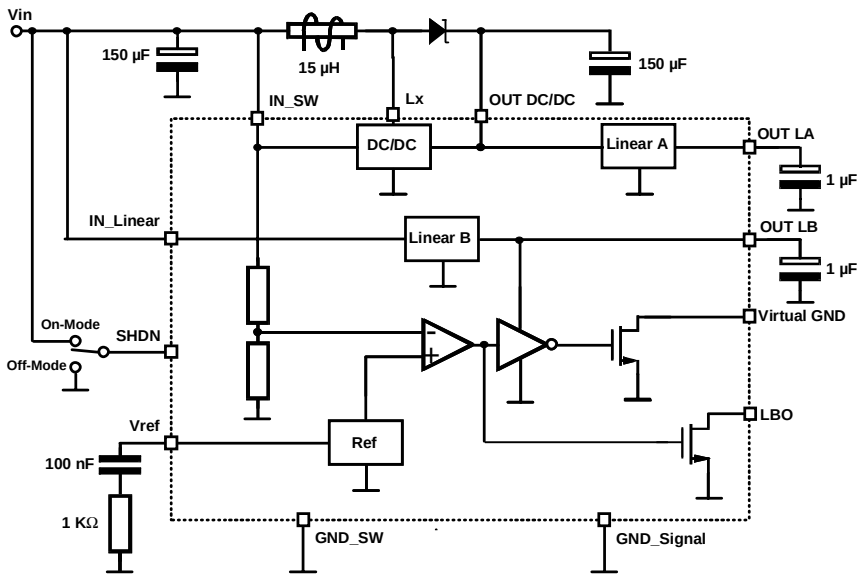
TRIPLE VOLTAGE REGULATOR

- ONLY TWO CELL NEED AS INPUT
- THREE REGULATED OUTPUT
  1) HIGH EFFICENCY PFM DC/DC CONVERTER 3.3V AT 200mA (87% EFFICENCY)
  2) VERY LOW NOISE AND VERY LOW DROP V_{REG} (3V AT 20mA)
  3) VERY LOW NOISE AAND VERY LOW DROP V_{REG} (1.9V AT 20mA)
- LOGIC CONTROLLED ELECTRONIC SHUTDOWN
- LOW BATTERY DETECTOR
- VIRTUAL GND PIN
- TEMPERATURA RANGE: -40 TO 85°C



SO-14

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage (Both IN_Linear and IN_SW)	-0.3 to 7	V
V_{SHDN}	Shutdown Input Voltage	-0.3 to V_{IN}+0.3	V
V_{LX}	Switch Voltage	-0.3 to 7	V
V_{LBO}	Low Battery Output Voltage	-0.3 to 7	V
$V_{virtual\_GND}$	Virtual GND Output Voltage	-0.3 to 7	V
I_{LBO}	Low Battery Output Maximum Current	30	mA
$I_{virtual\_GND}$	Virtual GND Output Maximum Current	30	mA
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_{op}	Operating Junction Temperature Range	-40 to +85	°C

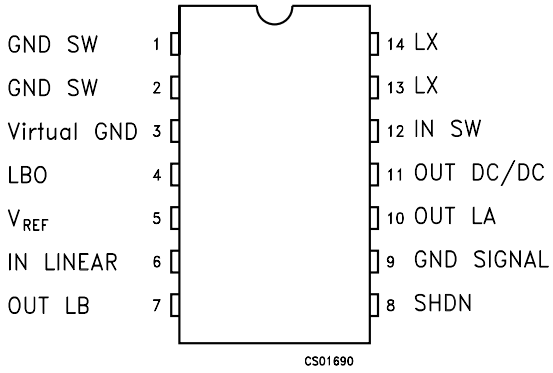
THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (*)	160	°C/W

ORDER CODES

Type	Package	Comment
ST3M01D	SO-14	50 parts per tube / 20 tube per box
ST3M01DTR	SO-14 (Tape & Reel)	2500 parts per reel

CONNECTION DIAGRAM (top view)



PIN DESCRIPTION

Pin N°	Symbol	Name and Function
1	GND SW	Switching Ground. Must be low impedance; solder directly to GND plane
2	GND SW	Switching Ground. Must be low impedance; solder directly to GND plane
3	Virtual GND	Virtual GND. Open Drain N-Cnannel MOSFET: must be high impedance when the Low Battery condition is detected.
4	LBO	Low Battery Output. Open Drain N-Cnannel MOSFET: sinks current when the input voltage drops below 2V typically.
5	V_{REF}	Reference Voltage Output. Bypass with 0.1 µF to improve the linears V_{REF} thermal noise performance.
6	IN Linear	Linear Input. Must be connected togheter with IN SW to the input supply.
7	OUT L_B	Linear B Output port. 1.9V typically.
8	SHDN	Shutdown Input. Disables the SMPS and L_A output, but the L_B, the referencevoltage and the low batery comparator remain active.
9	GND Signal	Signal GND. Must be connected togheter with the Switching Ground.
10	OUT L_A	Linear A Output port. 3V typically.
11	OUT DC/DC	DC/DC Output Port: 3.3V typically.
12	IN SW	SMPS Input. Must be connected togheter with IN_Linear to the input supply.
13	LX	1.5A N-Channel Power MOSFET Drain.
14	LX	1.5A N-Channel Power MOSFET Drain.

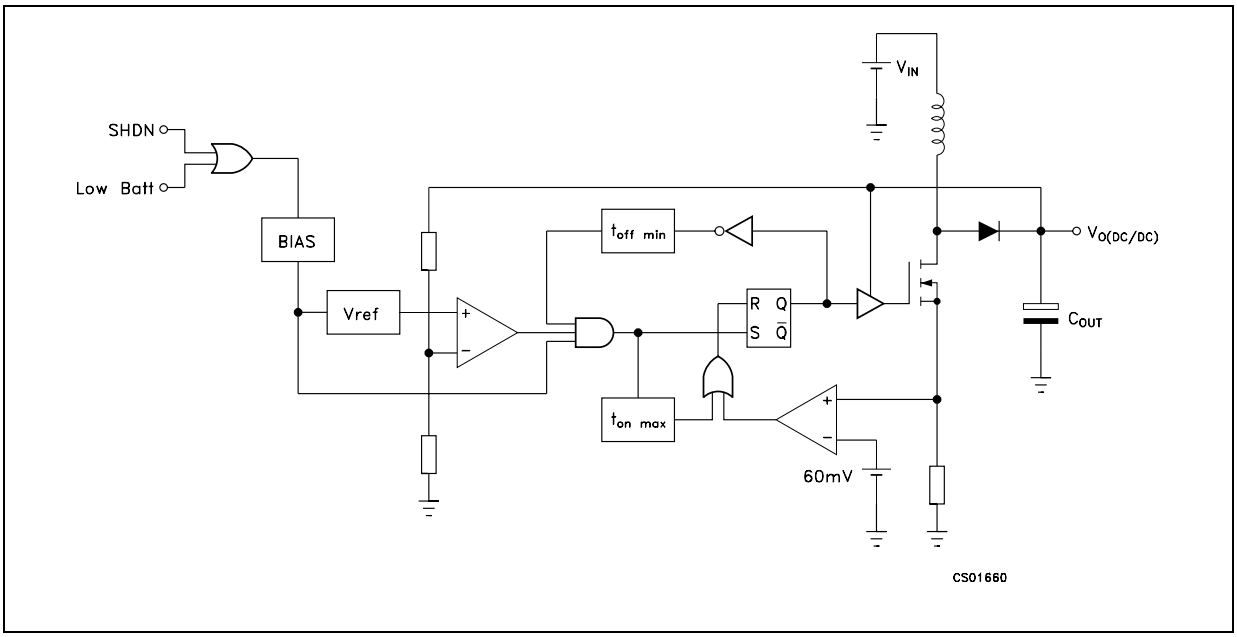
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, please refer to the typical operating circut of the pag 1 for the external components values and connections. Unless otherwise noted V_{SHDN}=HIGH)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_I	Operating Input Voltage		1.9		3.3	V
$V_{O(DC/DC)}$	DC/DC Converter Output Voltage (Test Circuit A)	2.24<V_{IN}<3.3V; 0<$I_{O(DC/DC)}$<200mA; 0<$I_{O(LA)}$<20mA; 0<$I_{O(LB)}$<20mA; -40 < T_J < 85 °C	3.2	3.3	3.415	V
ν	DC/DC Converter Efficency	V_{IN}=2.4V; $I_{O(DC/DC)}$=100mA; $I_{O(LA)}$=0mA; $I_{O(LB)}$=0mA; T_J = 25°C		87		%
$V_{O(LA)}$	Linear A Output Voltage (Test Circuit A)	2.24<V_{IN}<3.3V; 0<$I_{O(DC/DC)}$<200mA; 0<$I_{O(LA)}$<20mA; 0<$I_{O(LB)}$<20mA; -40 < T_J < 85°C	2.93	3	3.09	V
$V_{O(LB)}$	Linear B Output Voltage (Test Circuit A)	2.24<V_{IN}<3.3V; 0<$I_{O(DC/DC)}$<200mA; 0<$I_{O(LA)}$<20mA; 0<$I_{O(LB)}$<20mA; -40 < T_J < 85°C	1.86	1.9	1.955	V
$e_{N(LA)}$	Linear A Thermal Output Noise Voltage (Note 2)	V_{IN}=2.4V; $V_{O(DC/DC)}$=3.5V; $I_{O(LA)}$=20mA; 10 < f < 80KHz; $C_{O(LA)}$=1µF; C_{REF}=0.1µF; T_J = 25°C		60		μV_{rms}
$e_{N(LB)}$	Linear B Thermal Output Noise Voltage (Note 2)	V_{IN}=2.4V; $V_{O(DC/DC)}$=3.5V; $I_{O(LB)}$=20mA; 10 < f < 80KHz; $C_{O(LB)}$=1µF; C_{REF}=0.1µF; T_J = 25°C		35		μV_{rms}
$I_{q(OFF)}$	Quiescent Current OFF Mode DC/DC & L_A OFF L_B ON) (Test Circuit E)	V_{IN}=3.3V; No Load; V_{SHDN}=LOW; T_J = 25°C		75		µA
$I_{q(OFF)}$	Quiescent Current OFF Mode (DC/DC & L_A OFF L_B ON) (Test Circuit F)	V_{IN}=1.9V; No Load; V_{SHDN}=HIGH; T_J = 25°C		50		µA
$I_{S(DC/DC)}$	DC/DC Supply Current (Test Circuit B)	V_{IN}=2.24V; No Load; T_J = 25°C		100		µA
$I_{q(LA)}$	Linear A Quiescent Current (Test Circuit C)	V_{IN}=2.24V; $V_{O(DC/DC)}$=3.5V; $I_{O(LA)}$=10mA; T_J = 25°C		220		µA
$I_{q(LB)}$	Linear B Quiescent Current (Test Circuit C)	V_{IN}=2.24V; $V_{O(DC/DC)}$=3.5V; $I_{O(LB)}$=10mA; T_J = 25°C		75		µA
V_{BATT}	Low Battery Detection Range	V_{SHDN}=HIGH with falling edge	1.96	2	2.04	V
$V_{BATT(HYS)}$	Low Battery Detection Hysteresys			150	200	mV
$R_{ON(LBO)}$	LBO R_{DSON}	V_{IN}=1.9V; I_D=5mA; T_J = 25°C		10		Ω
V_{ih}	Control Input Logic Low	V_{IN}>2.24V; -40 < T_J < 85°C			0.4	V
V_{il}	Control Input Logic High	V_{IN}>2.24V; -40 < TJ < 85°C	1.5			V
T_{on}	Timer On Response Time on DC/DC	V_{IN}=2.4V; C_O=100µF; T_J = 25°C $I_{O(DC/DC)}$=200mA V_{SHDN}=from GND to $V_{SHDN(MAX)}$		0.6	9	ms
$R_{ON(V\_GND)}$	Virtual GND RDSON	V_{IN}>2.24V; I_D=5mA; T_J = 25°C		10		Ω

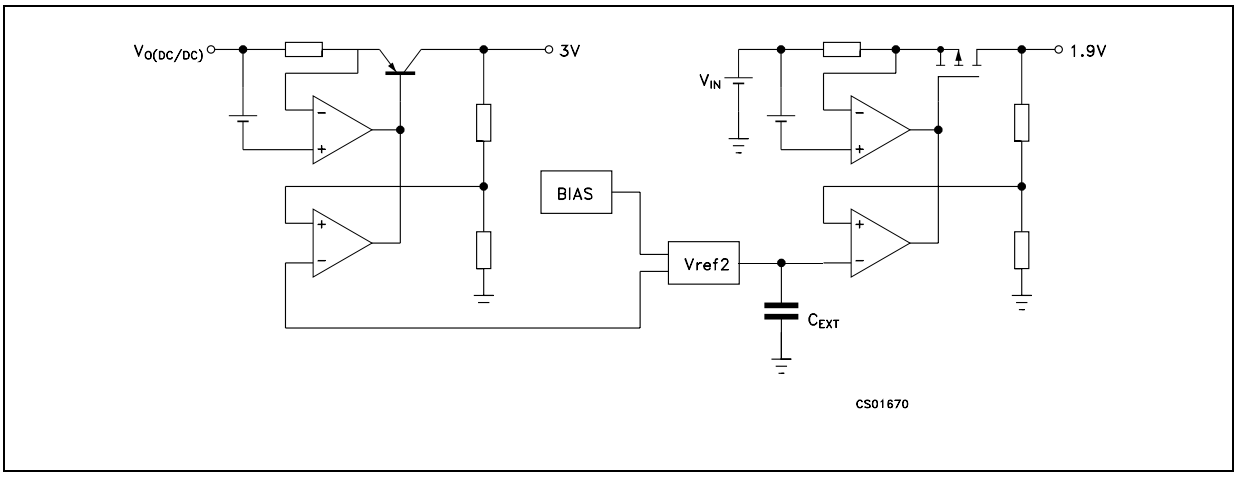
Note 1: For V_{IN} < 1.9V the $V_{O(LB)}$ is out of regulation because of under dropout condition

Note 2: $V_{O(DC/DC)}$ = 3.5V force for an external DC source to avoid switching noise

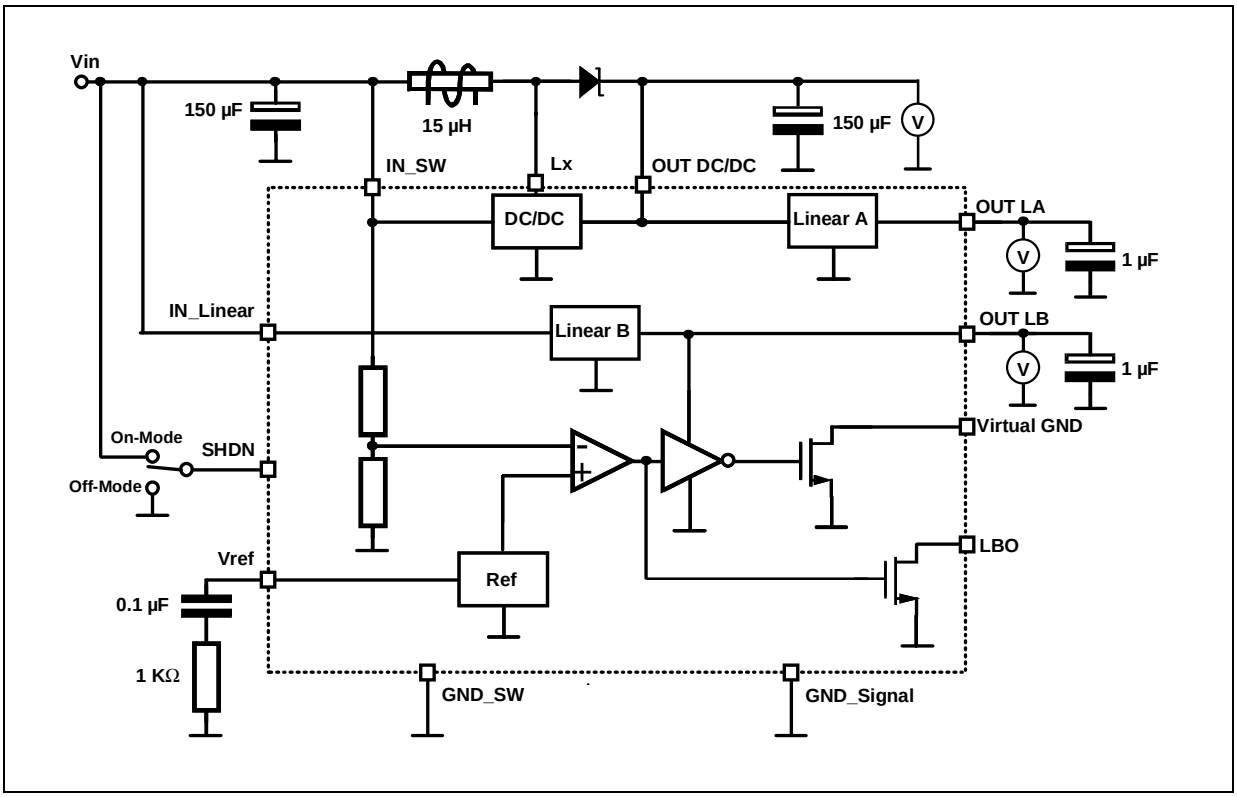
DC/DC CONVERTER BLOCK DIAGRAM



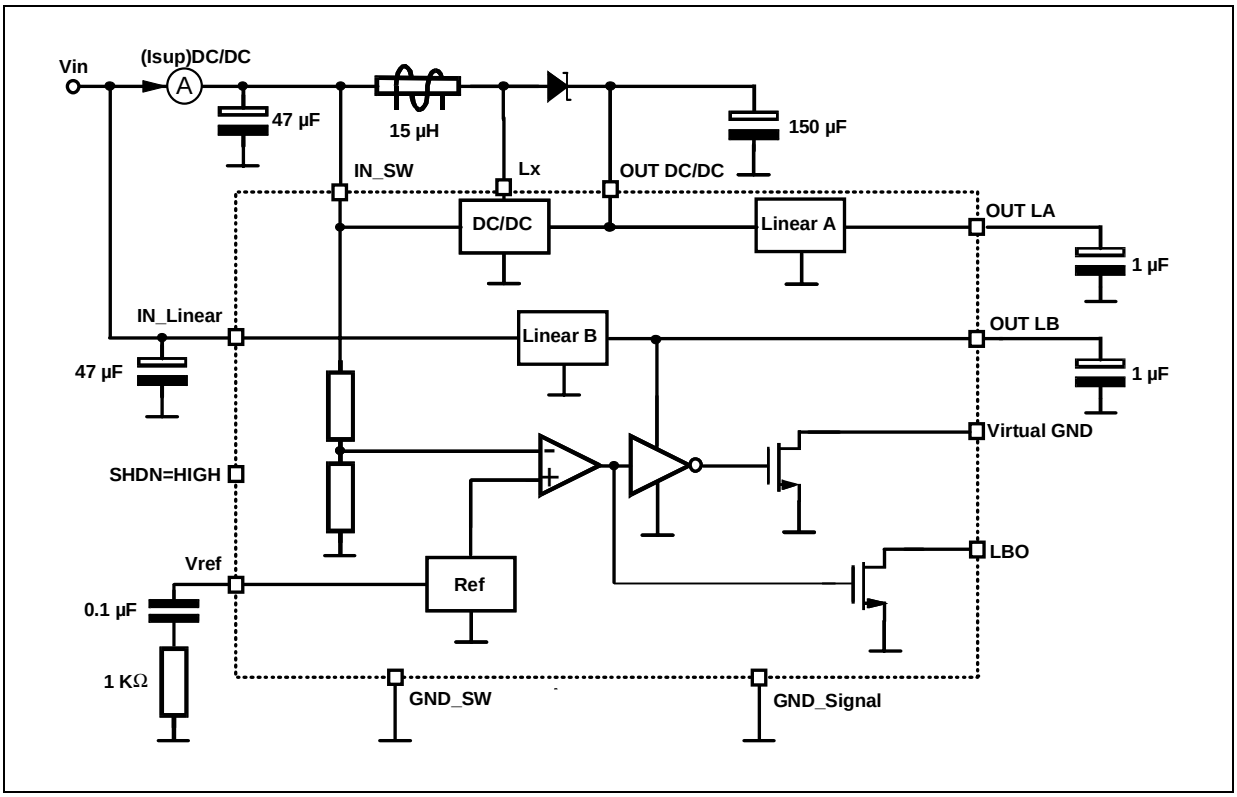
LINEAR VREG BLOCK DIAGRAM



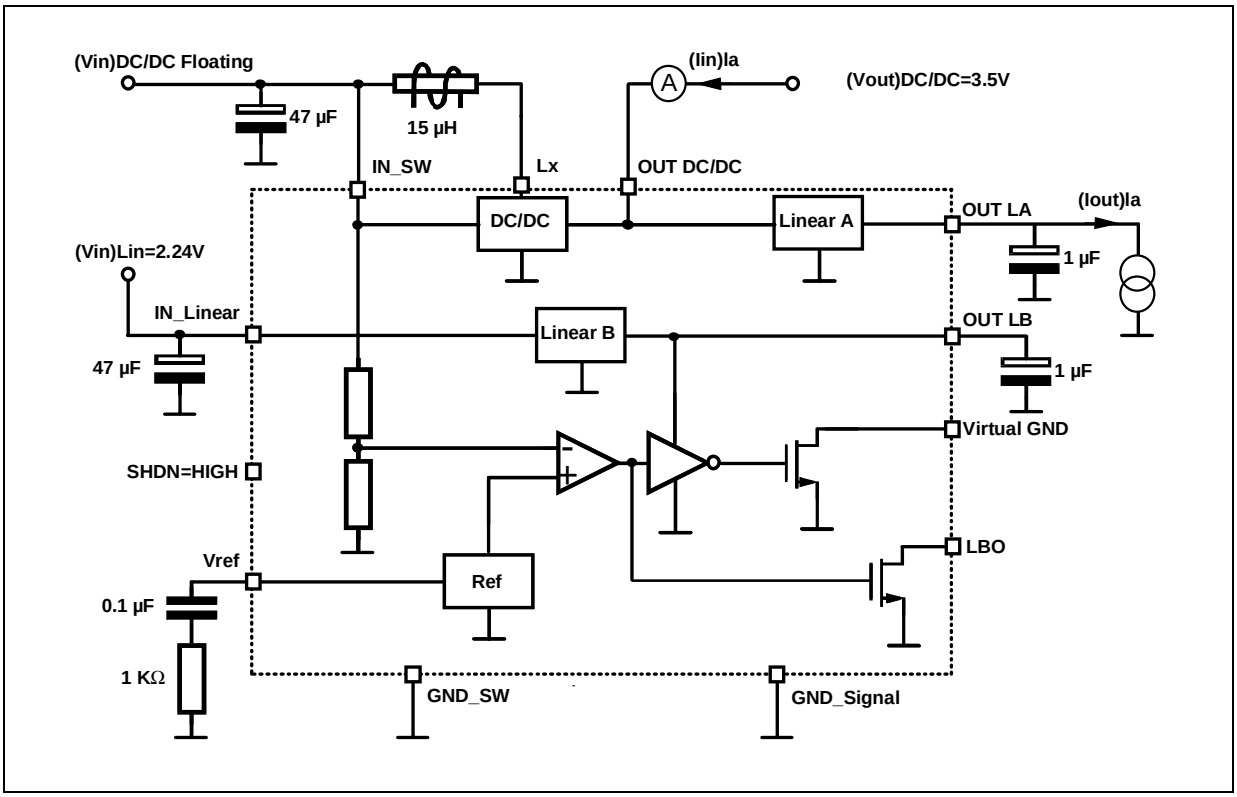
TEST CIRCUIT A



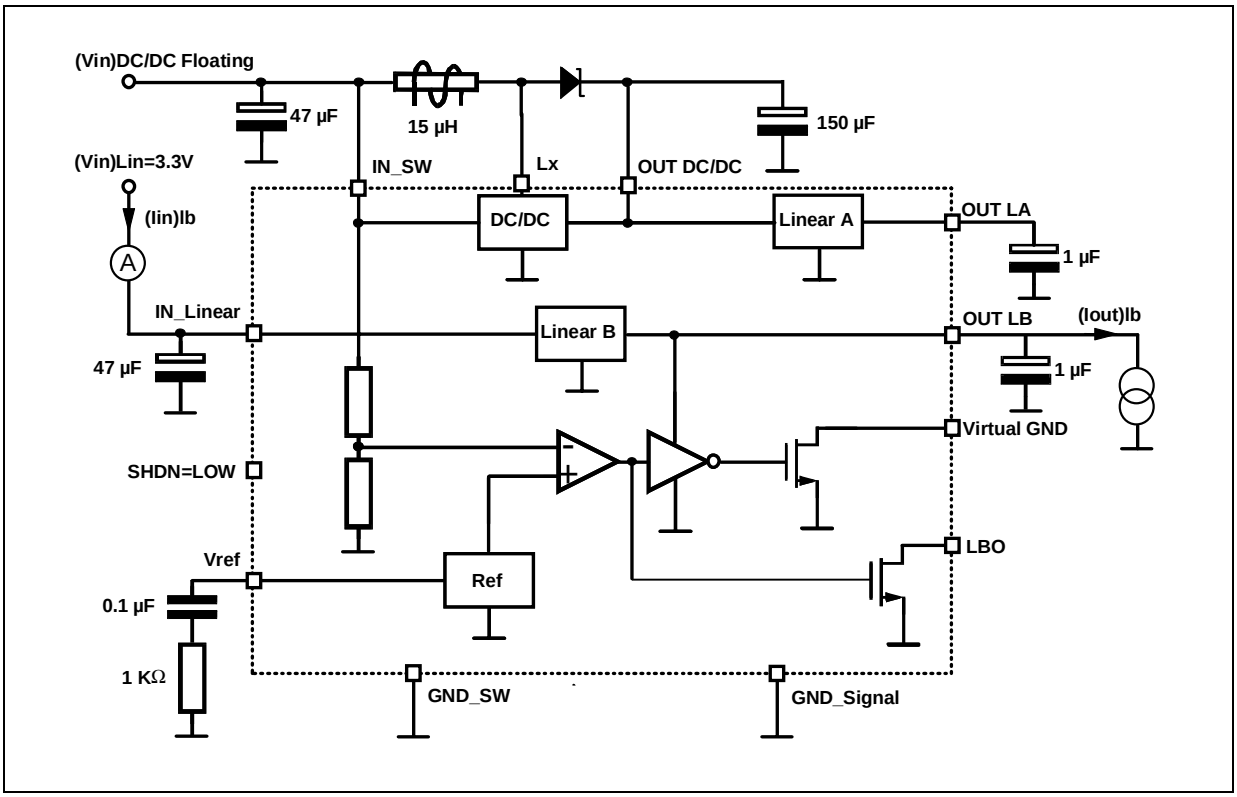
TEST CIRCUIT B



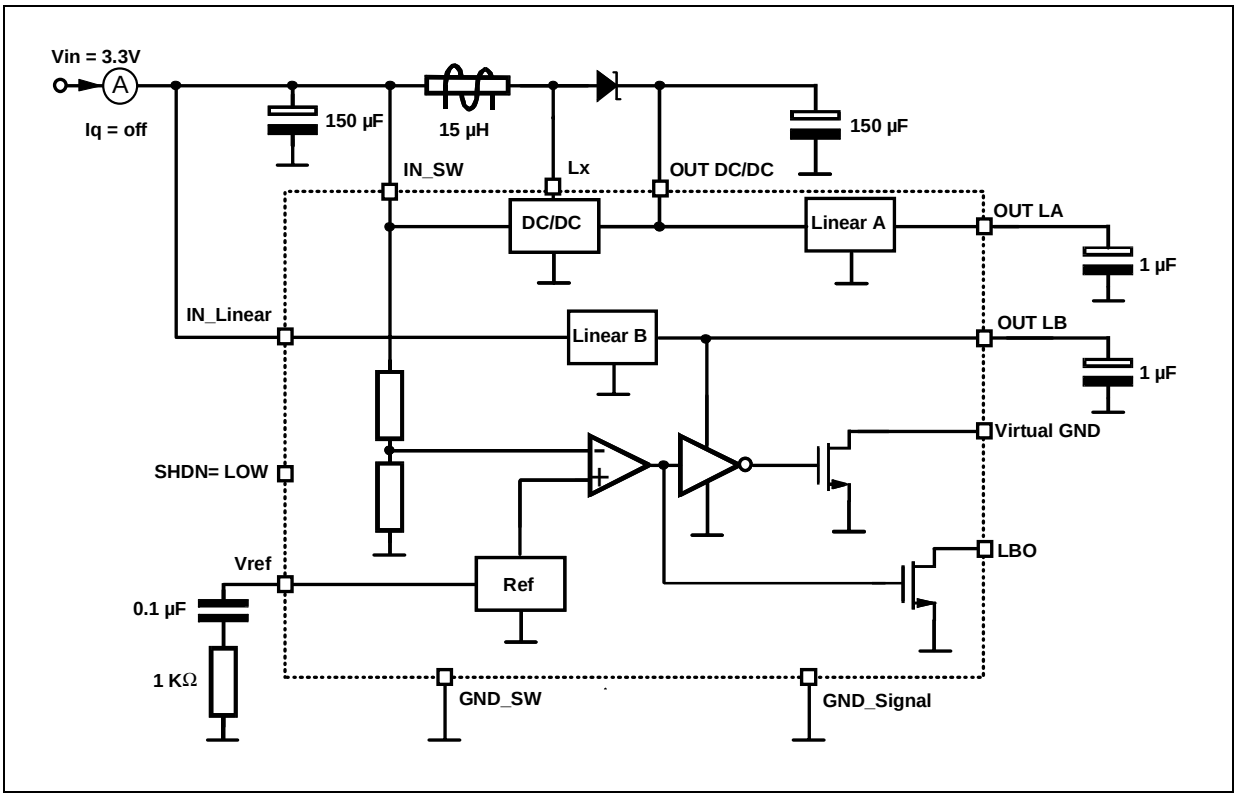
TEST CIRCUIT C (Iq)Ia=(Iin)Ia-(Iout)Ia



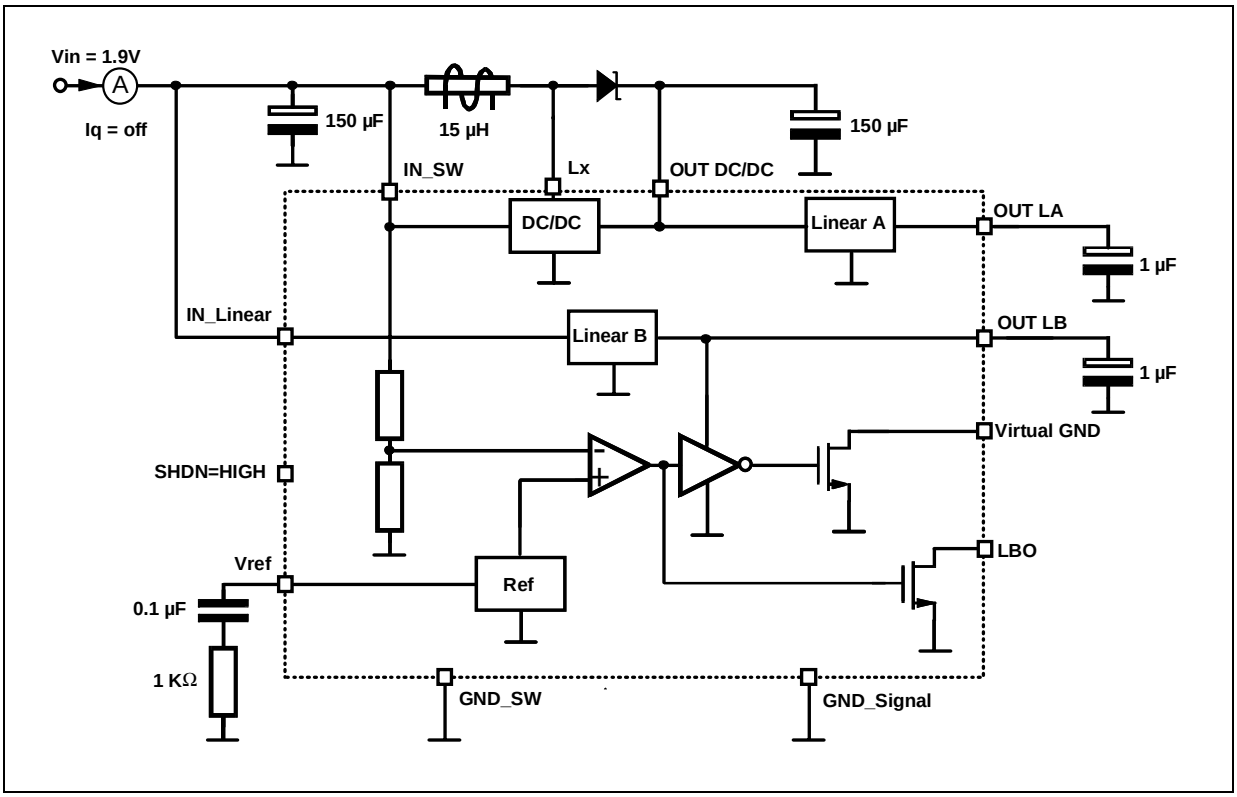
TEST CIRCUIT D (Iq)Ib=(Iin)Ib-(Iout)Ib



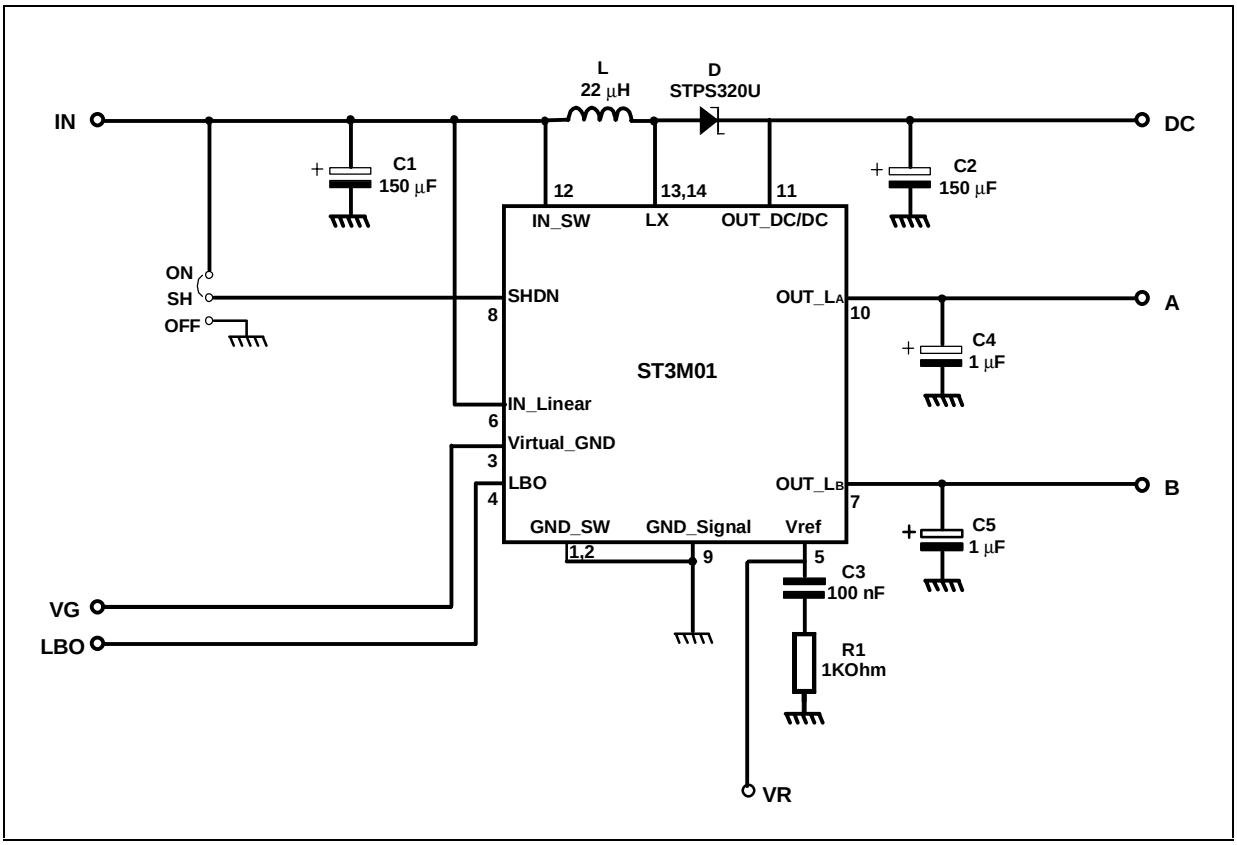
TEST CIRCUIT E



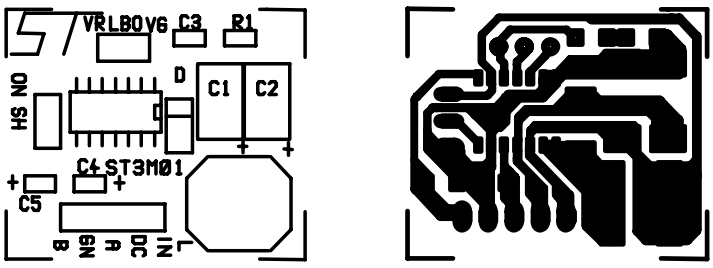
TEST CIRCUIT F



DEMOBOARD CIRCUIT

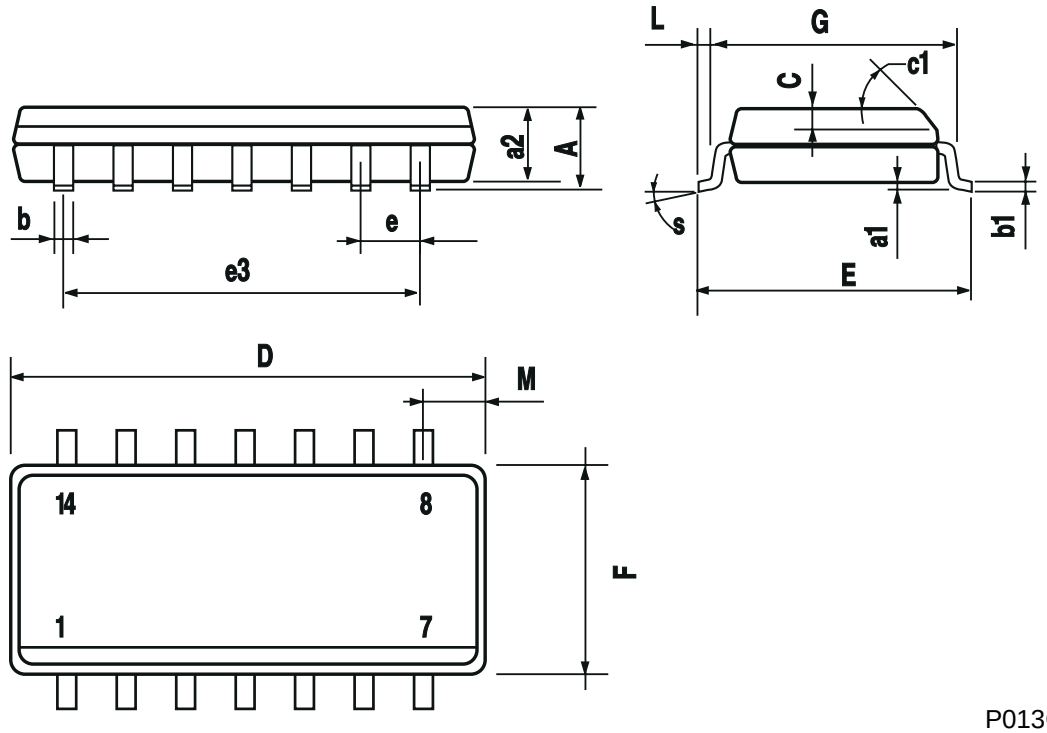


PC BOARD LAYOUT



SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



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