



# STP11NM60A STP11NM60AFP - STB11NM60A-1

N-CHANNEL 600V - 0.4Ω - 11A TO-220/TO-220FP/I<sup>2</sup>PAK

MDmesh™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP11NM60A	600 V	<0.45Ω	11 A
STP11NM60AFP	600 V	<0.45Ω	11 A
STB11NM60A-1	600 V	<0.45Ω	11 A

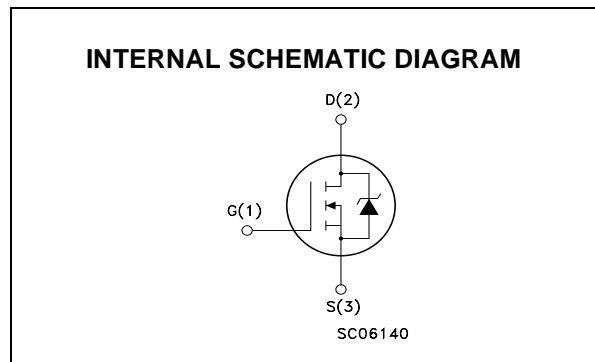
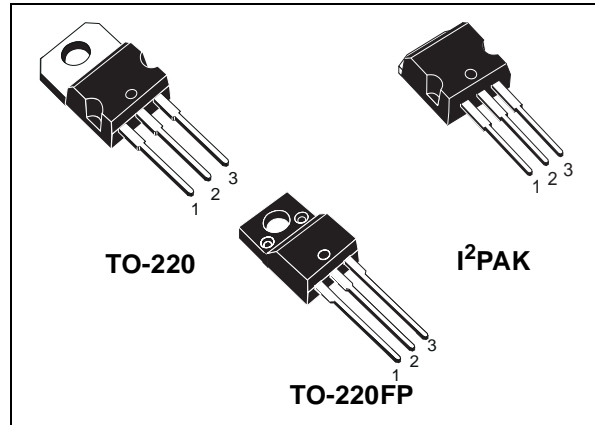
- TYPICAL R<sub>DS(on)</sub> = 0.4Ω
- HIGH dv/dt
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

## DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

## APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP11NM60A	P11NM60A	TO-220	TUBE
STP11NM60AFP	P11NM60AFP	TO-220FP	TUBE
STB11NM60A-1	B11NM60A	I <sup>2</sup> PAK	TUBE

## STP11NM60A/STP11NM60AFP/STB11NM60A-1

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP11NM60A STB11NM60A-1	STP11NM60AFP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	600		V
V <sub>GS</sub>	Gate- source Voltage	± 30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	11	11 (*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	7	7 (*)	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	44	44 (*)	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	110	35	W
	Derating Factor	0.88	0.28	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2500	V
T <sub>j</sub>	Operating Junction Temperature	-55 to 150		°C
T <sub>stg</sub>	Storage Temperature	-55 to 150		°C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 11A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		TO-220 / I <sup>2</sup> PAK	TO-220-FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.13	3.57	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.5 A		0.4	0.45	Ω

**ELECTRICAL CHARACTERISTICS** (TCASE =25°C UNLESS OTHERWISE SPECIFIED)

**DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 5.5\text{ A}$		10		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$		1211 248 21		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 480\text{ V}$		116		pF
$R_G$	Gate Input Resistance	$f=1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.9		$\Omega$

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 300\text{ V}, I_D = 5.5\text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		14 15		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V}$		35 9 14	49	nC nC nC

**SWITCHING OFF**

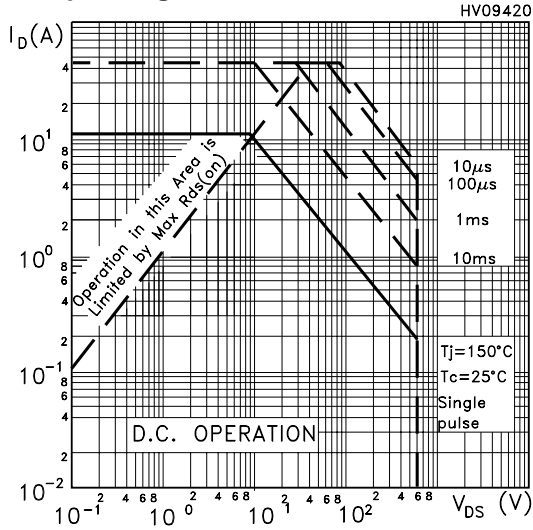
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 480\text{ V}, I_D = 11\text{ A},$ $R_G = 4.7\Omega, V_{GS} = 10\text{ V}$ (Inductive Load see, Figure 5)		39 10 20		ns ns ns

**SOURCE DRAIN DIODE**

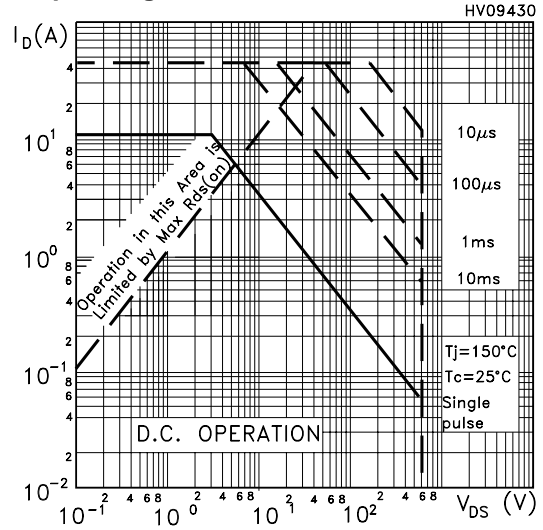
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				11 44	A A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 11\text{ A}, V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}, T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		560 5.7 20.5		ns $\mu\text{C}$ A

- Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
 2. Pulse width limited by safe operating area.  
 3.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

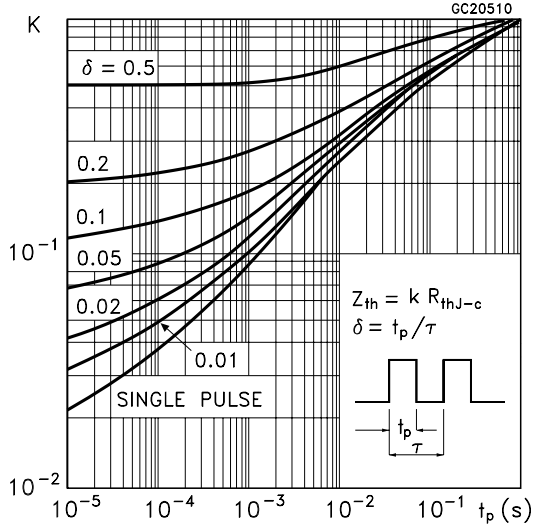
Safe Operating Area for TO-220 / I2PAK



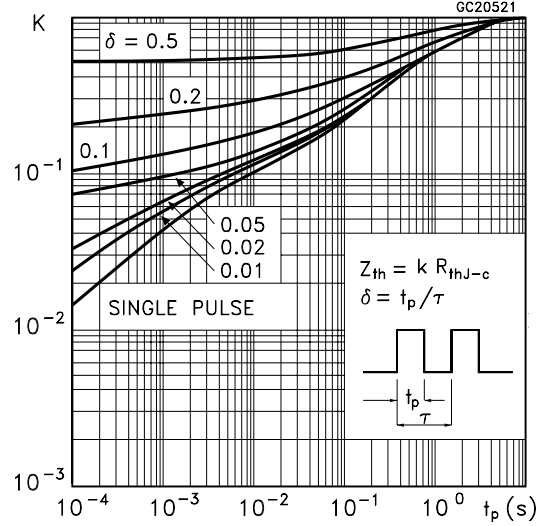
Safe Operating Area for TO-220FP



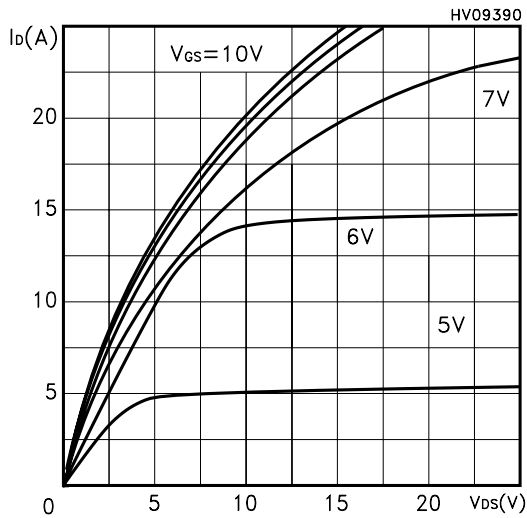
Thermal Impedance for TO-220 / I2PAK



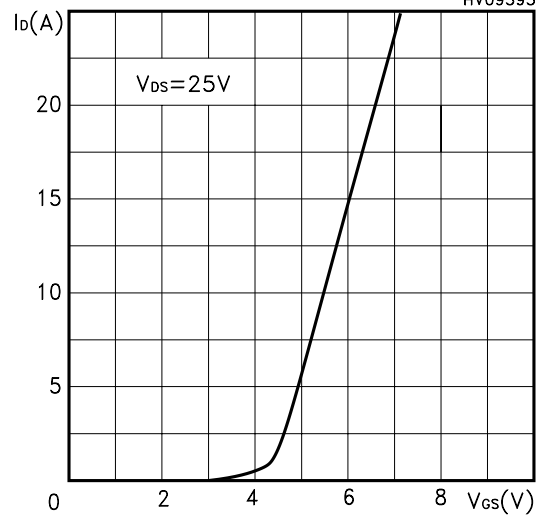
Thermal Impedance for TO-220FP



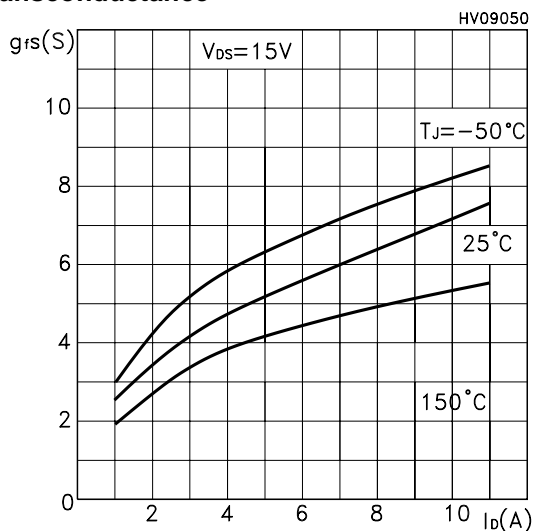
Output Characteristics



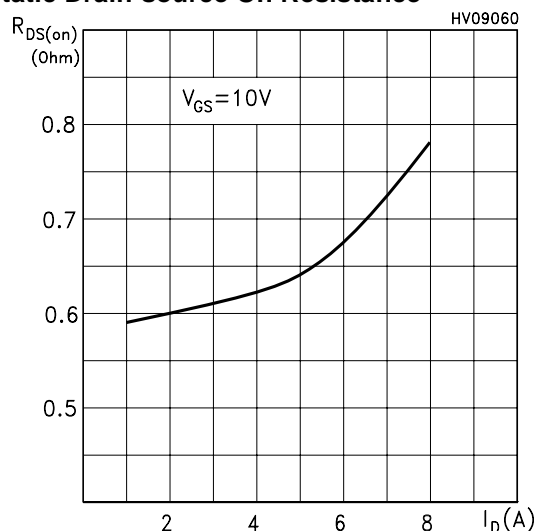
Transfer Characteristics



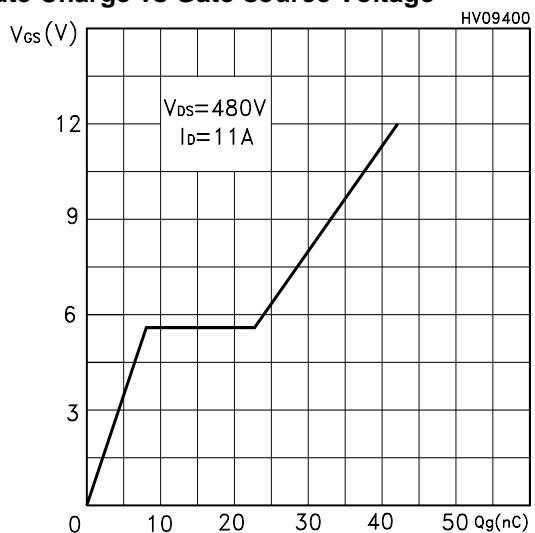
**Transconductance**



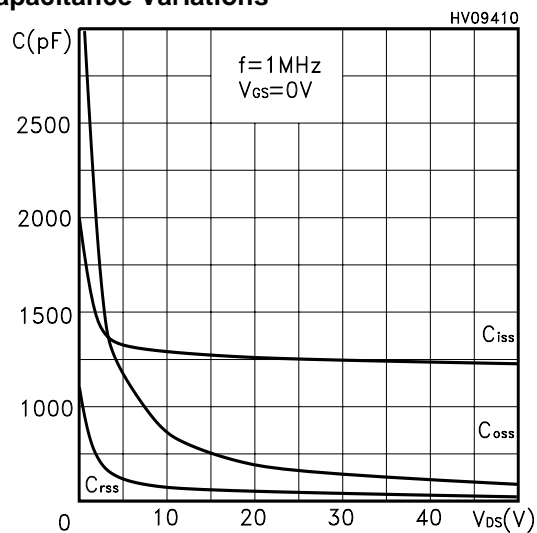
**Static Drain-source On Resistance**



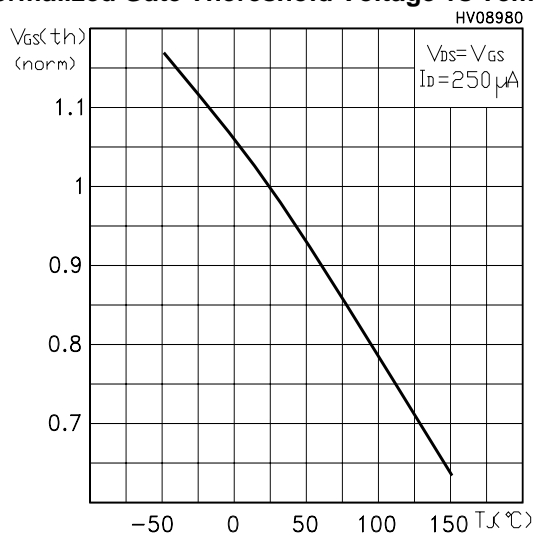
**Gate Charge vs Gate-source Voltage**



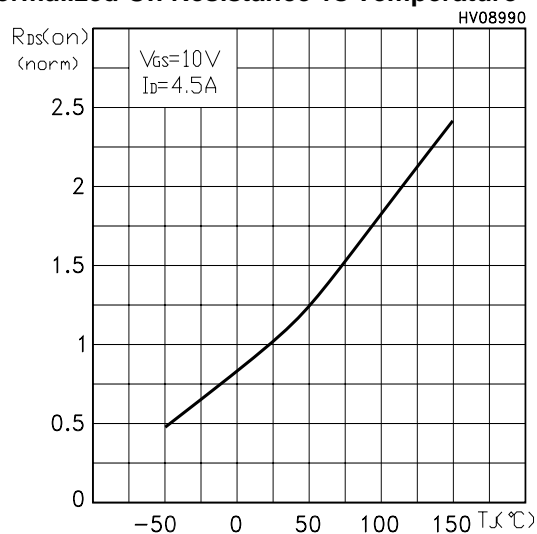
**Capacitance Variations**



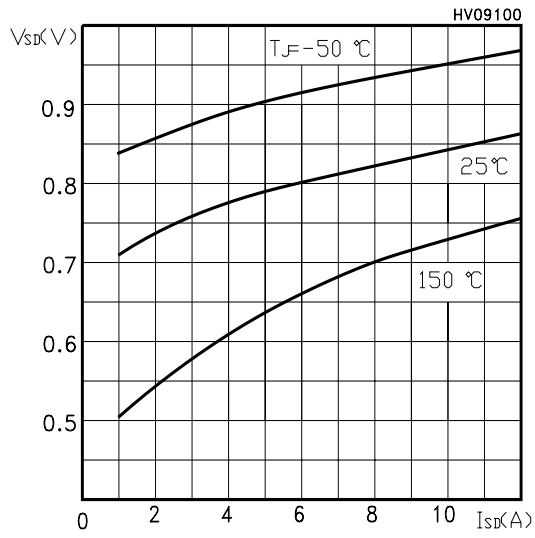
**Normalized Gate Threshold Voltage vs Temp.**



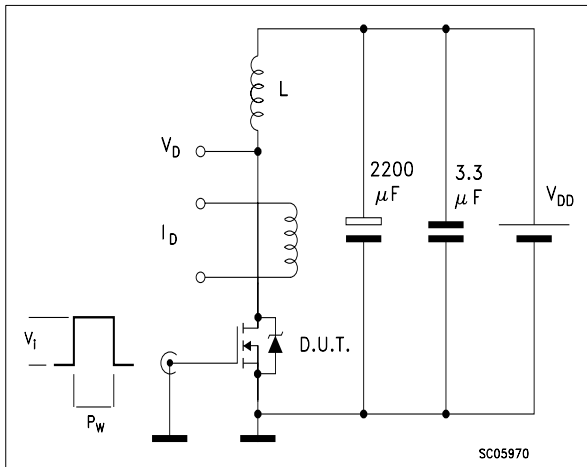
**Normalized On Resistance vs Temperature**



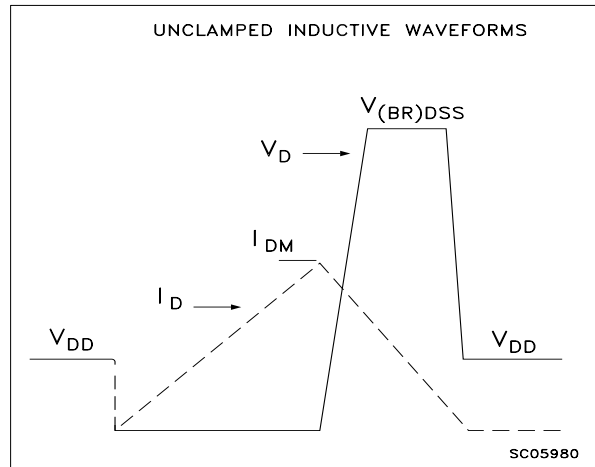
Source-drain Diode Forward Characteristics



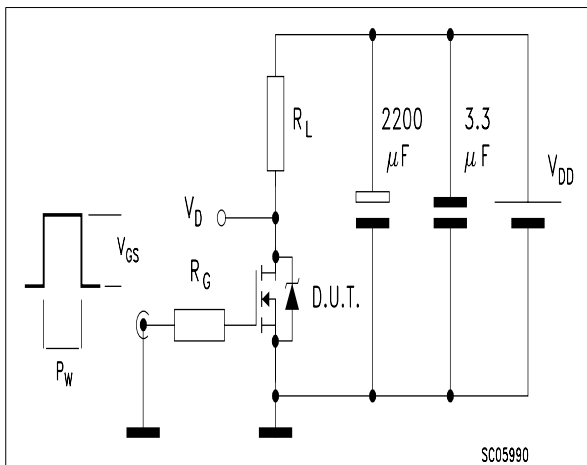
**Fig. 1: Unclamped Inductive Load Test Circuit**



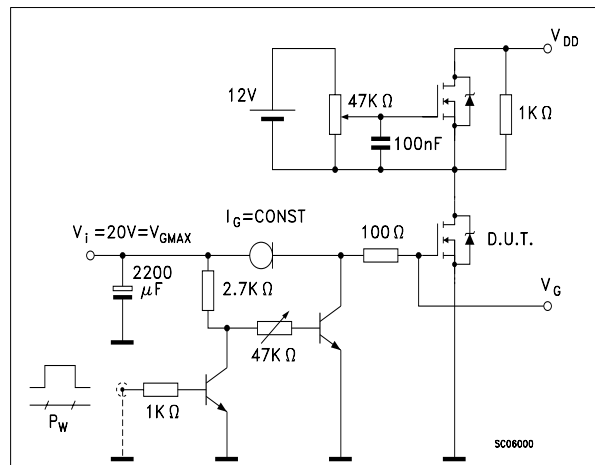
**Fig. 2: Unclamped Inductive Waveform**



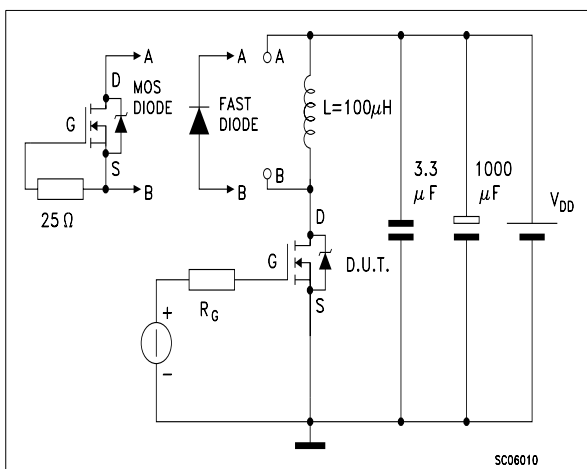
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

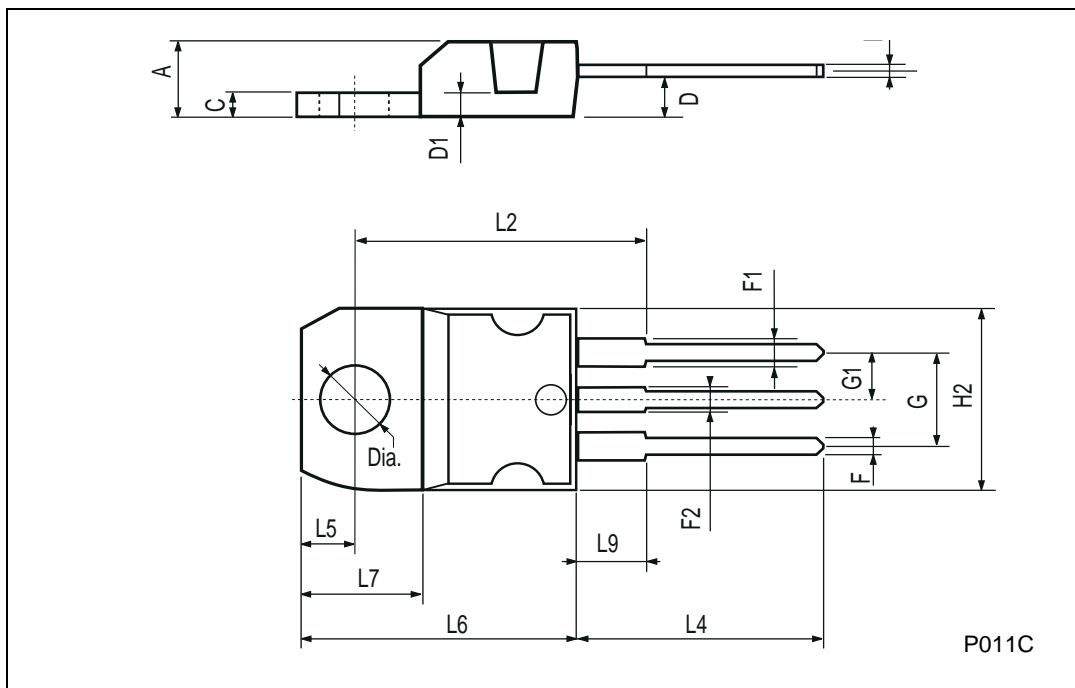


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



TO-220 MECHANICAL DATA

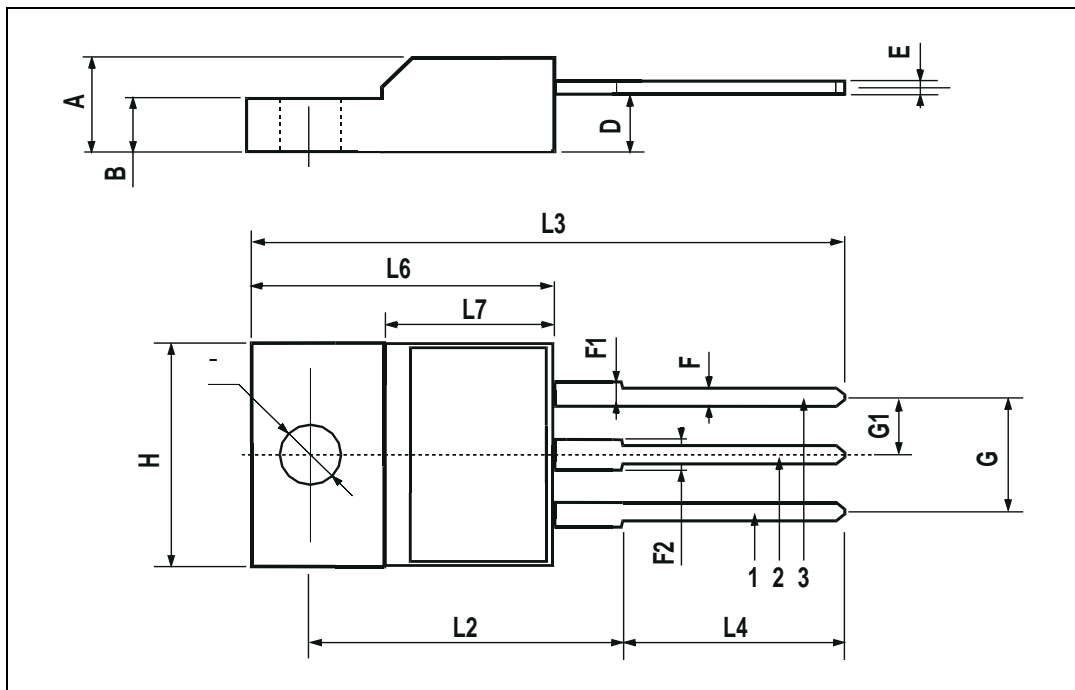
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151





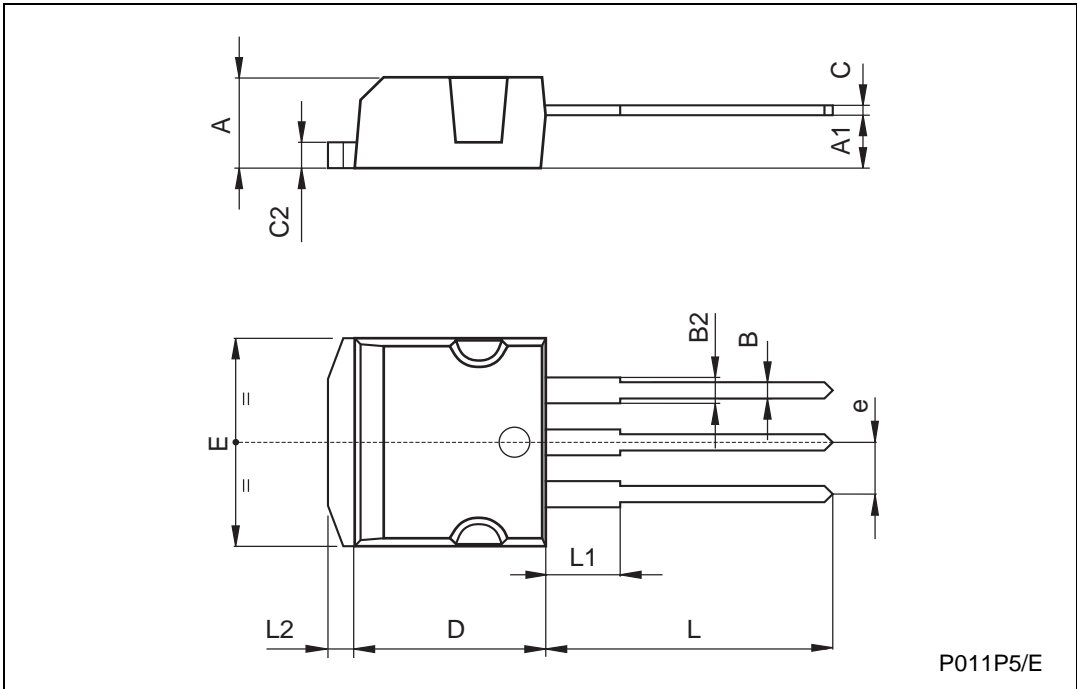
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



**TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



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