STB80PF55

P-CHANNEL 55V - 0.016 Ω - 80A D²PAK
STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB80PF55	55 V	< 0.018 Ω	80 A

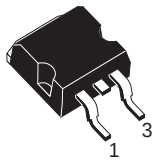
- TYPICAL $R_{DS}(on)$ = 0.016 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

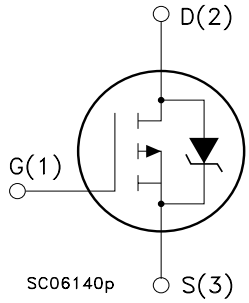
- MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS



D²PAK
TO-263
(Suffix "T4")

ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	55	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	55	V
V_{GS}	Gate- source Voltage	± 16	V
$I_{D(*)}$	Drain Current (continuos) at T_C = 25°C	80	A
I_D	Drain Current (continuos) at T_C = 100°C	57	A
I_{DM}(•)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	1.4	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area
(*) Current Limited by Package

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed
(1) $I_{SD} \le 40A$, $di/dt \le 300A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX.}$
(2) Starting T_j = 25 °C, I_D = 80A, V_{DD} = 40V

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	55			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 40 A		0.016	0.018	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 40 A		32		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		5500 1130 600		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 25 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		35 190		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 25 V I_D = 80 A V_{GS}= 10V		190 27 65	258	nC nC nC

SWITCHING OFF (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 25 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		165 80		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{clamp} = 40 V I_D = 80 A R_G = 4.7 Ω V_{GS} = 10 V (Inductive Load, Figure 5)		60 40 85		ns ns ns

SOURCE DRAIN DIODE (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 80 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 80 A di/dt = 100A/µs V_{DD} = 25 V T_j = 150°C (see test circuit, Figure 5)		110 495 9		ns nC A

(*) Pulse width ≤ 300 µs, duty cycle 1.5 %.
(•) Pulse width limited by T_{JMAX}

Fig. 1: Unclamped Inductive Load Test Circuit

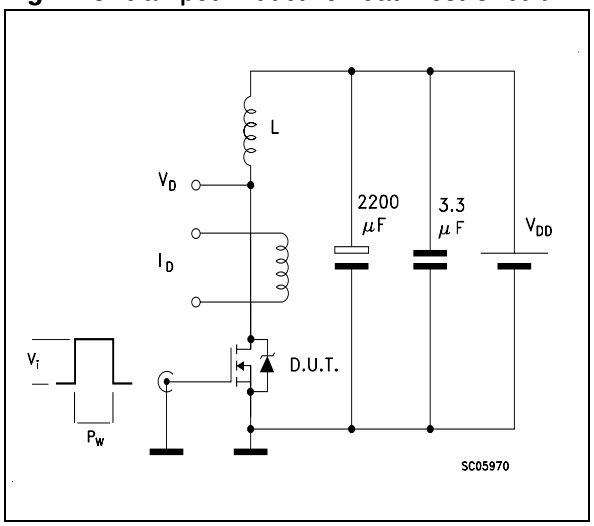


Fig. 2: Unclamped Inductive Waveform

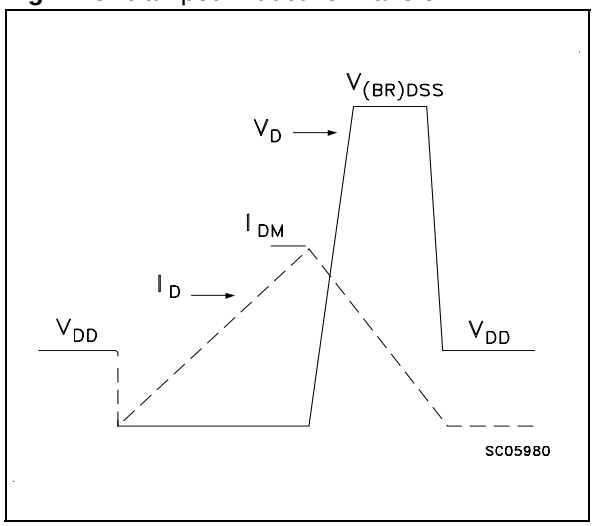


Fig. 3: Switching Times Test Circuits For Resistive Load

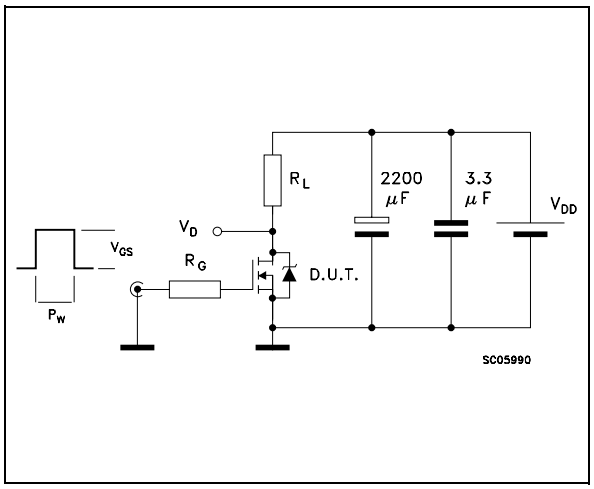


Fig. 4: Gate Charge test Circuit

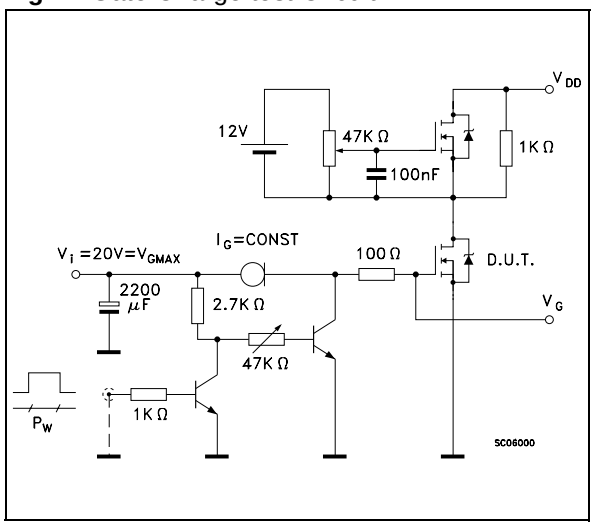
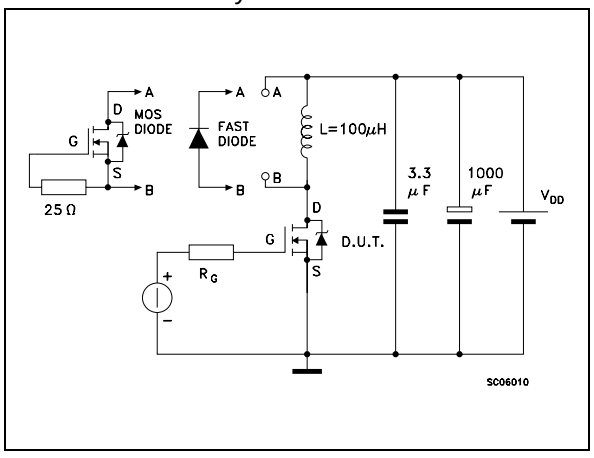
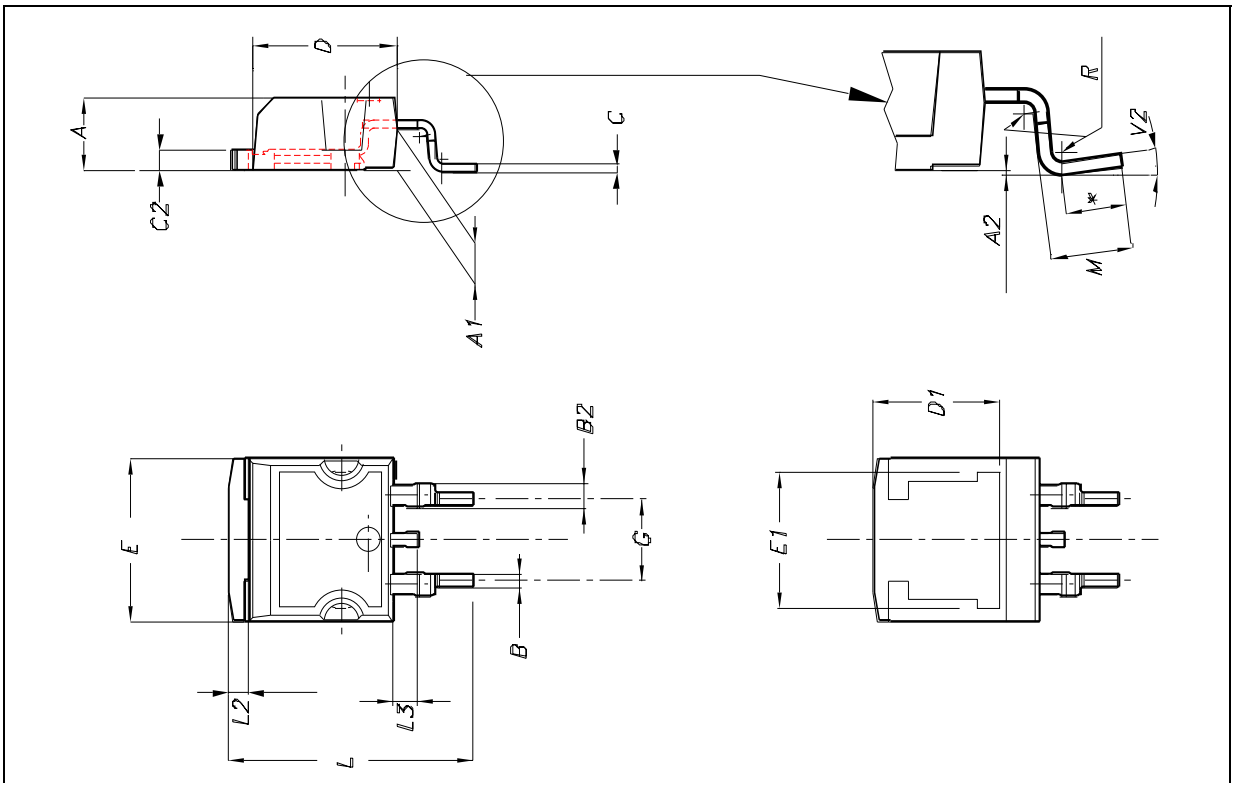


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

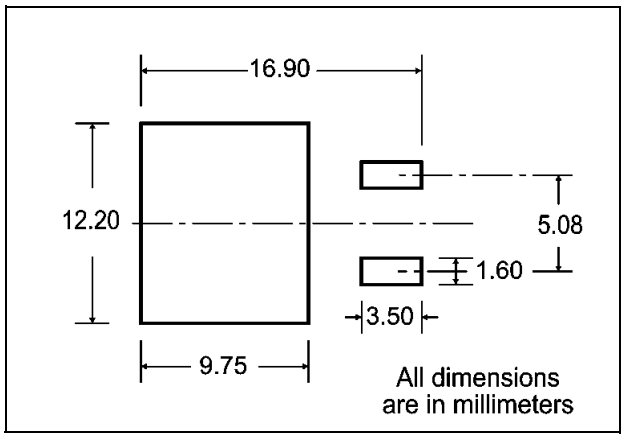


D²PAK MECHANICAL DATA

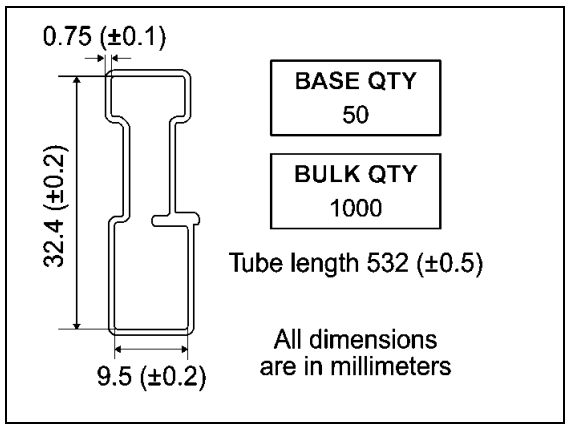
DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1	8.5				0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.016	
V2	0°		8°	0°		8°



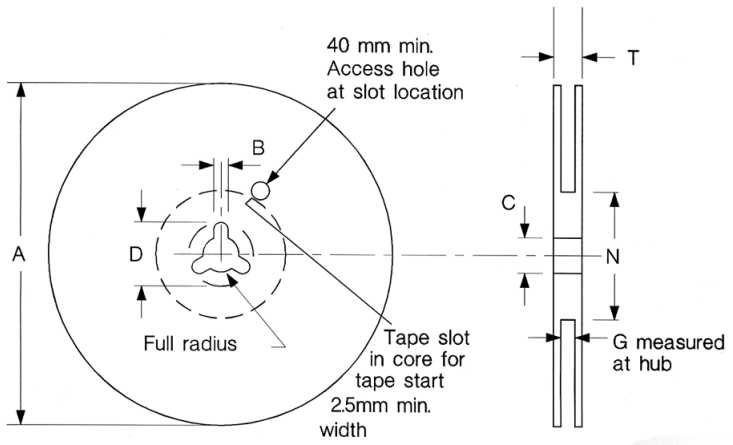
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



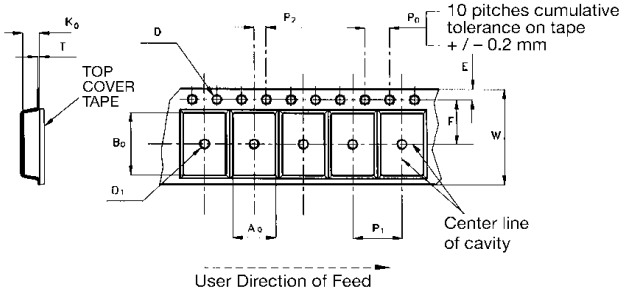
REEL MECHANICAL DATA

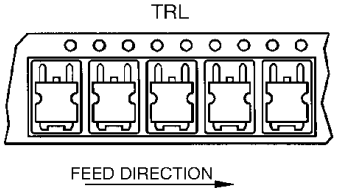
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

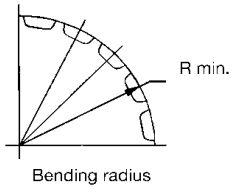
BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0075	0.082
R	50		1.574	
T	0.25	0.35	.0.0098	0.0137
W	23.7	24.3	0.933	0.956







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