



# STL22NF10

## N-CHANNEL 100V - 0.055 Ω - 22A PowerFLAT™ LOW GATE CHARGE STripFET™ II MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL22NF10	100 V	<0.060 Ω	22 A <sup>(1)</sup>

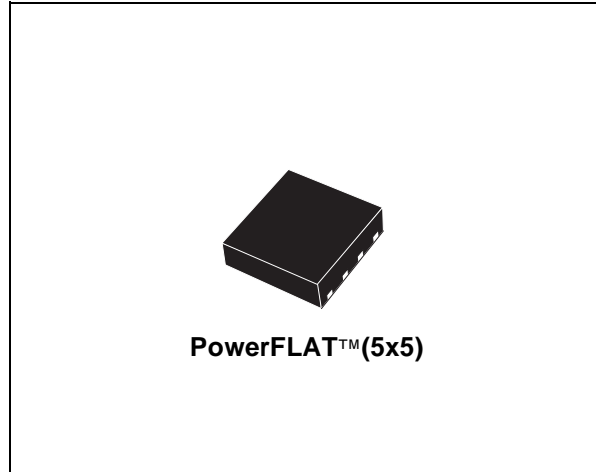
- TYPICAL R<sub>DS(on)</sub> = 0.055 Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE

### DESCRIPTION

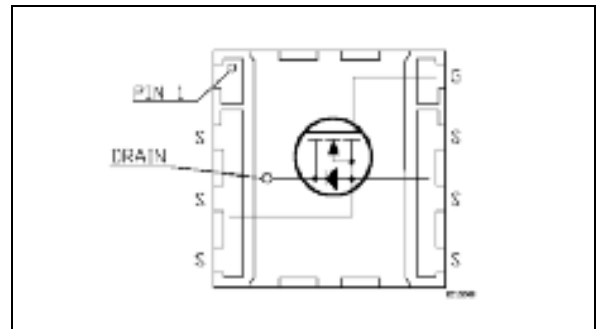
This application specific Power MOSFET is the second generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor shows extremely low on-resistance and minimal gate charge. The new PowerFLAT™ package allows a significant reduction in board space without compromising performance.

### APPLICATIONS

- HIGH-EFFICIENCY ISOLATED DC-DC CONVERTERS
- TELECOM AND AUTOMOTIVE



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	100	V
V <sub>GS</sub>	Gate- source Voltage	± 20	V
I <sub>D</sub> <sup>(2)</sup>	Drain Current (continuous) at T <sub>C</sub> = 25°C (Steady State)	5.3	A
I <sub>D</sub> <sup>(2)</sup>	Drain Current (continuous) at T <sub>C</sub> = 100°C	3.8	A
I <sub>DM</sub> <sup>(3)</sup>	Drain Current (pulsed)	22	A
P <sub>tot</sub> <sup>(2)</sup>	Total Dissipation at T <sub>C</sub> = 25°C (Steady State)	4	W
P <sub>tot</sub> <sup>(1)</sup>	Total Dissipation at T <sub>C</sub> = 25°C	70	W
	Derating Factor	0.03	W/°C
dv/dt <sup>(5)</sup>	Peak Diode Recovery voltage slope	16	V/ns
E <sub>AS</sub> <sup>(6)</sup>	Single Pulse Avalanche Energy	82	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 150	°C
T <sub>j</sub>	Operating Junction Temperature		

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## THERMAL DATA

Rthj-F	(*)Thermal Resistance Junction-Foot (Drain)	1.8	°C/W
Rthj-pcb(4)	Thermal Operating Junction-pcb	31.5	°C/W

(\*) Mounted on FR-4 board ( $t \leq 10$  sec.)

## ELECTRICAL CHARACTERISTICS ( $T_{case} = 25$ °C unless otherwise specified)

### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating } T_C = 125^\circ C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA

### ON (7)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS} \quad I_D = 250 \mu A$	2			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 V \quad I_D = 11 A$		0.055	0.060	$\Omega$

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(7)}$	Forward Transconductance	$V_{DS} = 20 V \quad I_D = 11 A$		16		S
$C_{iss}$	Input Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		885		pF
$C_{oss}$	Output Capacitance			130		pF
$C_{rss}$	Reverse Transfer Capacitance			56		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 11\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		20 45		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80\text{ V}$ $I_D = 22\text{ A}$ $V_{GS} = 10\text{ V}$		30 6 10	40	nC nC nC

**SWITCHING OFF**

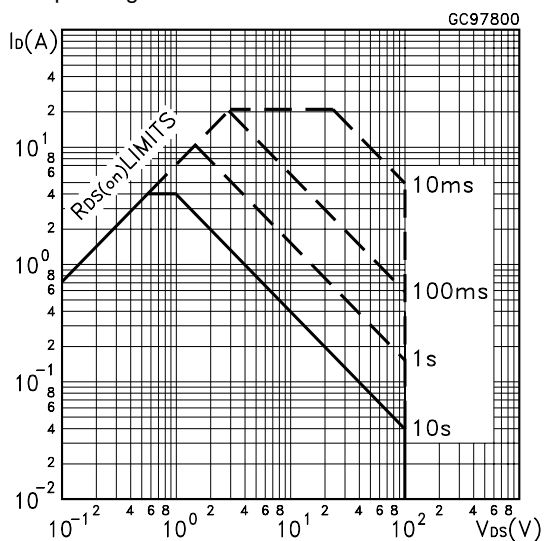
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 11\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		45 10		ns ns

**SOURCE DRAIN DIODE**

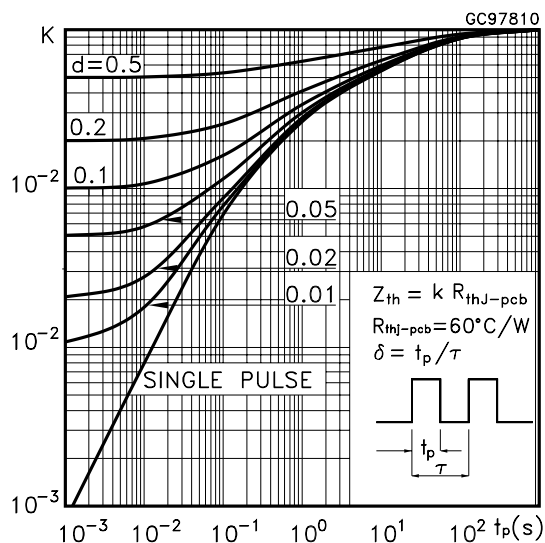
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$	Source-drain Current Source-drain Current (pulsed)				5.3 22	A A
$V_{SD}^{(7)}$	Forward On Voltage	$I_{SD} = 22\text{ A}$ $V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 22\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		100 375 7.5		ns nC A

- (1) The value is rated according  $R_{thj-F}$ .
- (2) The value is rated according  $R_{thj-pcb}$ .
- (3) Pulse width limited by safe operating area.
- (4) When Mounted on FR-4 Board of 1 inch<sup>2</sup>, 2 oz Cu,  $t < 10\text{s}$ .
- (5)  $I_{SD} \leq 22\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{jMAX}$ .
- (6) Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 11\text{ A}$ ,  $V_{DD} = 30\text{ V}$ .
- (7) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

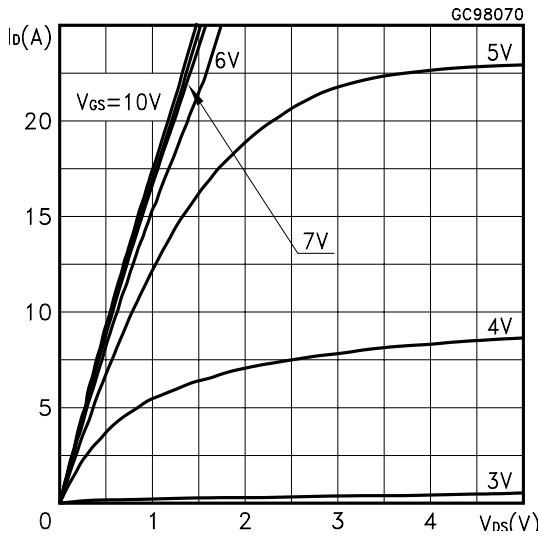
**Safe Operating Area**



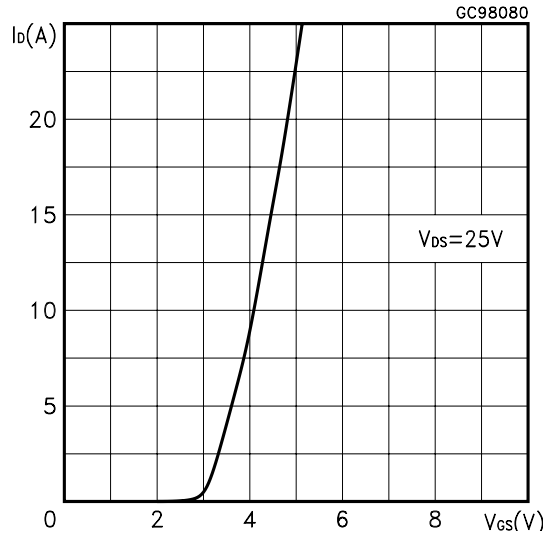
**Thermal Impedance**



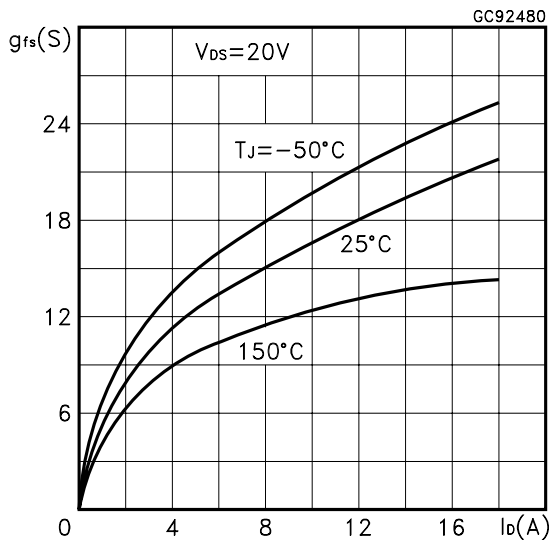
Output Characteristics



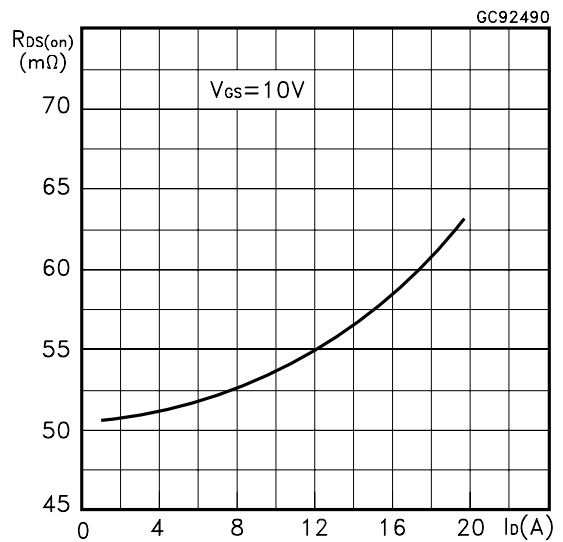
Transfer Characteristics



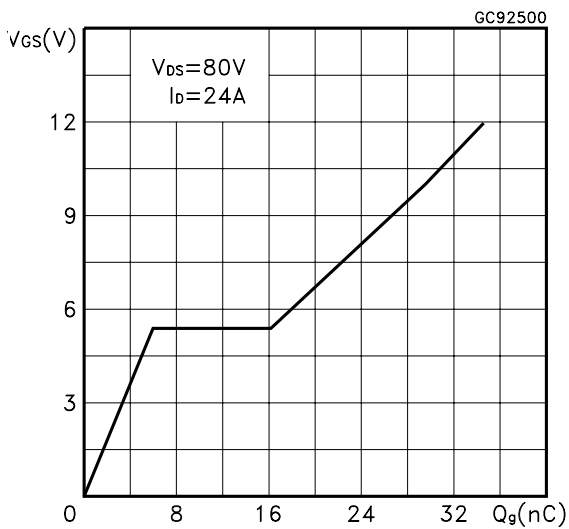
Transconductance



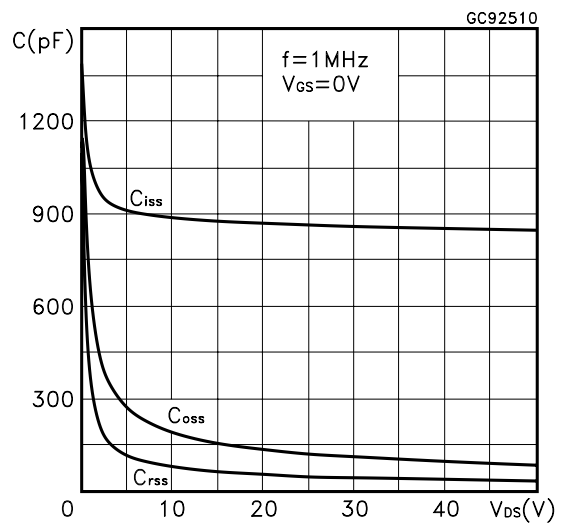
Static Drain-source On Resistance



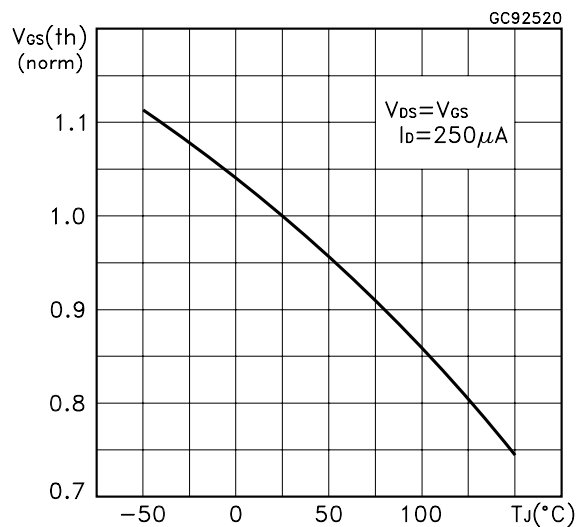
Gate Charge vs Gate-source Voltage



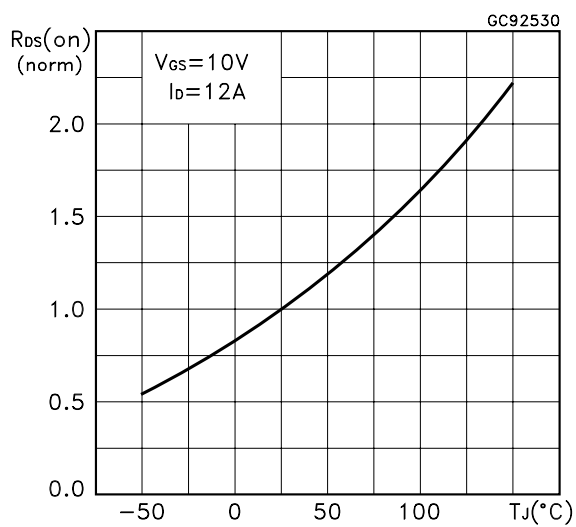
Capacitance Variations



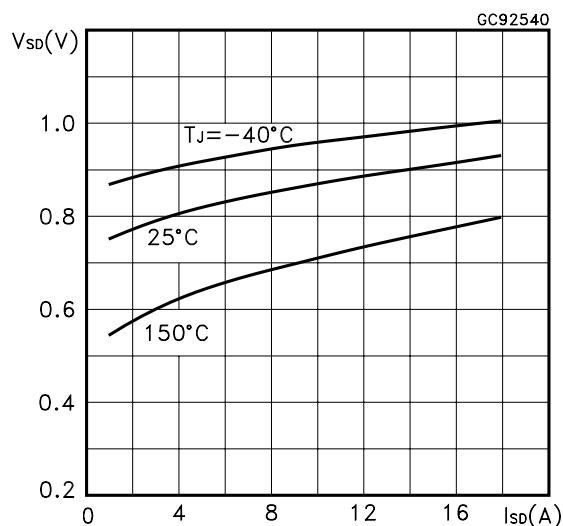
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.

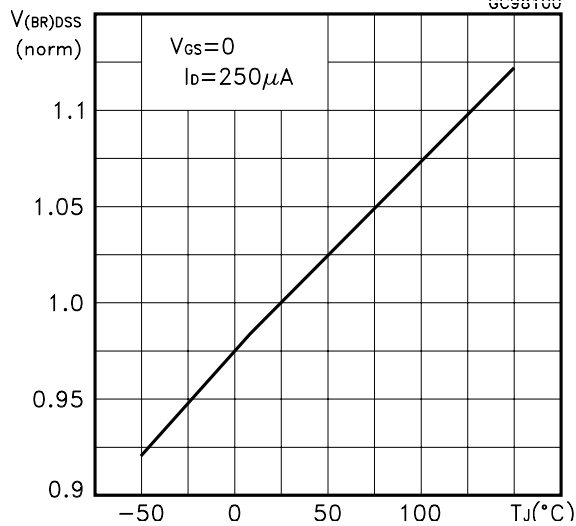


Fig. 1: Unclamped Inductive Load Test Circuit

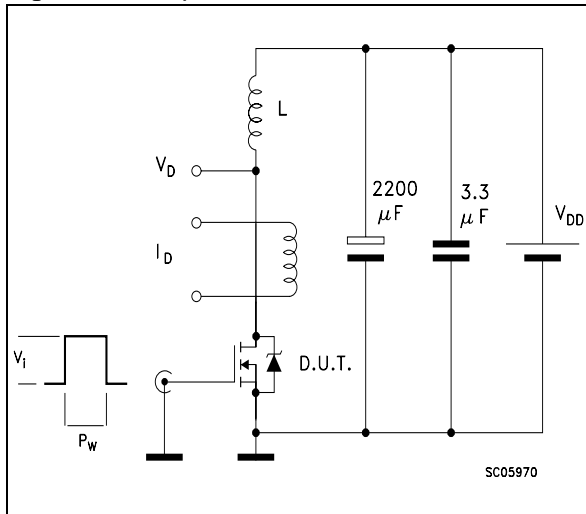


Fig. 2: Unclamped Inductive Waveform

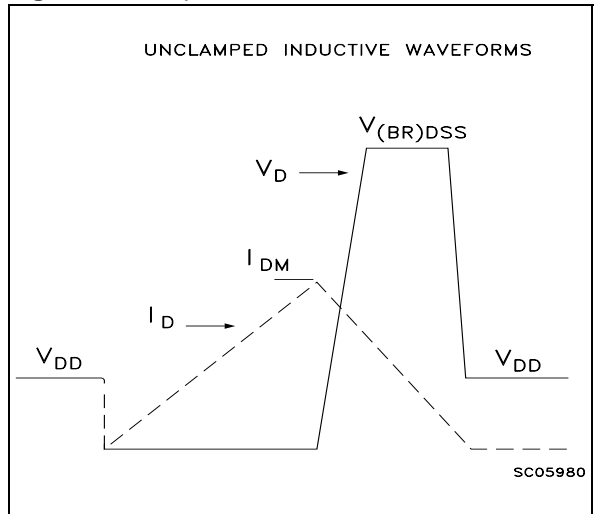


Fig. 3: Switching Times Test Circuits For Resistive Load

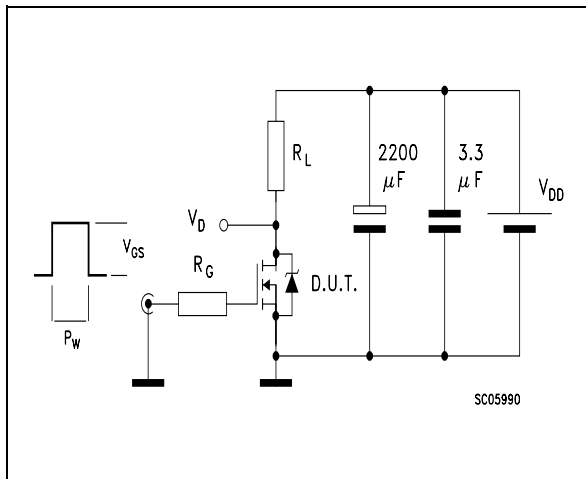


Fig. 4: Gate Charge test Circuit

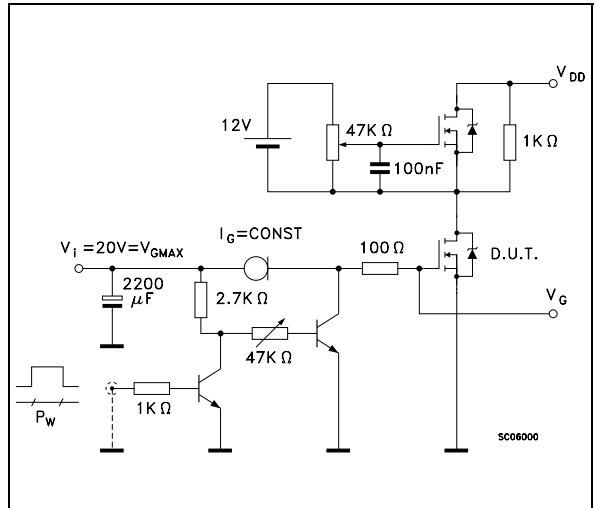
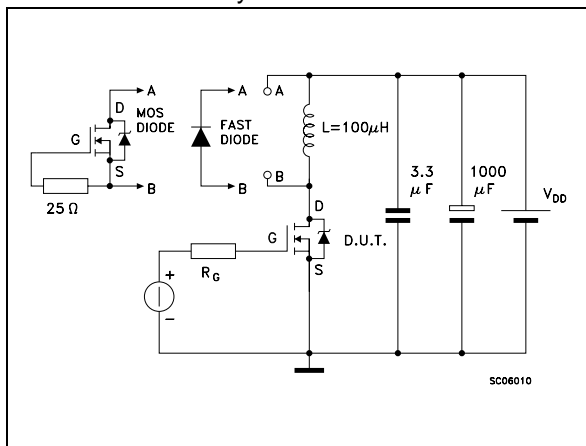
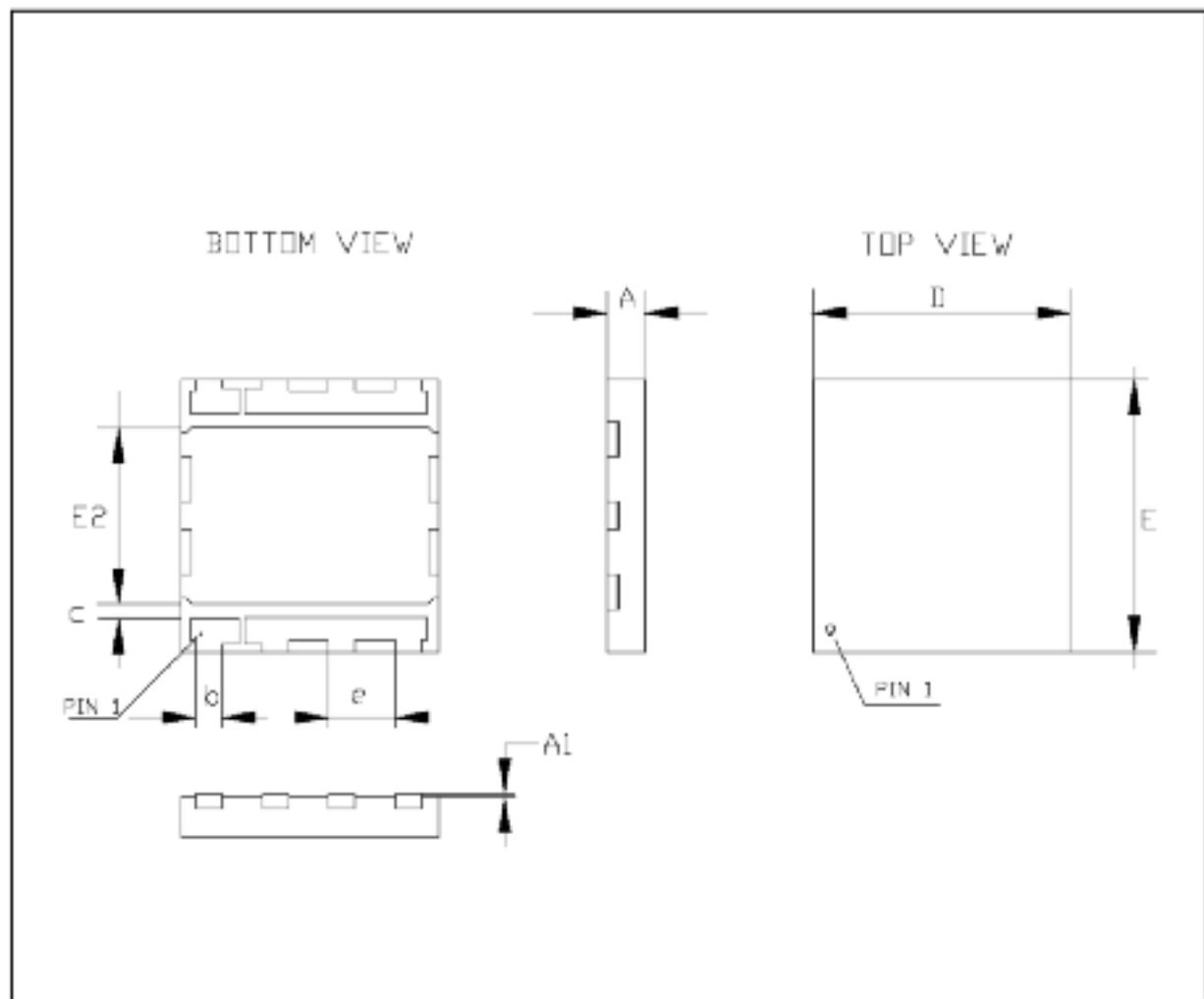


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



### PowerFLAT™ (5x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.33	0.41	0.48	0.013	0.016	0.019
D		5.00			0.197	
E		5.00			0.197	
E2	3.10	3.18	3.25	0.122	0.125	0.128
e		1.27			0.050	



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