

STL34NF06

N-CHANNEL 60V - 0.024Ω - 34A PowerFLAT™ LOW GATE CHARGE STripFET™II MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STL34NF06	60 V	< 0.028Ω	34 A

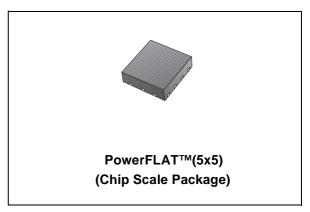
- TYPICAL $R_{DS}(on) = 0.024\Omega$
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE

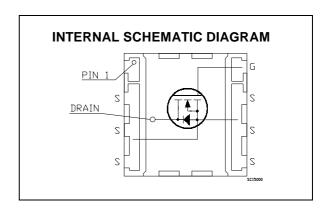
DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "STripFETTM" technology. The resulting transistor shows extremely low onresistance and minimal gate charge. The new PowerFLATTM package allow a significant reduction in board space without compramising performance.

APPLICATIONS

- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	60	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at $T_C = 25^{\circ}C$ (*) Drain Current (continuous) at $T_C = 100^{\circ}C$	34 20	A A
I _{DM} (•)	Drain Current (pulsed)	136	А
P _{TOT}	Total Dissipation at T _C = 25°C	70	W
	Derating Factor	0.56	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	250	mJ
T _{stg}	Storage Temperature	-55 to 150	°C
Tj	Max. Operating Junction Temperature	-35 to 130	

(•)Pulse width limited by safe operating area

(1) Starting $T_i = 25^{\circ}C$, $I_D = 17A$, $V_{DD} = 42V$

1/6

(*) Current Limited by Wire Bonding is 20A

November 2002

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.8	°C/W
Rthj-pcb (#)	Thermal Resistance Junction-ambient Max	31.2	°C/W

^(*) When mounted on 1inch² FR4 Board, 2oz of Cu, $t \le 10$ sec.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25~^{\circ}C$ UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	60			V
I _{DSS}	Zero Gate Voltage	V _{DS} = Max Rating			1	μA
	Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, T _C = 125 °C			10	μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 17A		0.024	0.028	Ω

DYNAMIC

Symbol	ymbol Parameter Test Conditions		Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 30 V , I _D = 17 A		TBD		S
C _{iss}	Input Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		920		pF
Coss	Output Capacitance			225		pF
C _{rss}	Reverse Transfer Capacitance			80		pF

^{1.} Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2/6

ELECTRICAL CHARACTERISTICS (CONTINUED) SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on Delay Time	V _{DD} = 30V, I _D = 17 A		11		ns
t _r	Rise Time	$R_G = 4.7\Omega V_{GS} = 10V$ (see test circuit, Figure 3)		50		ns
Qg	Total Gate Charge	V _{DD} = 48V, I _D = 34 A,		32	43	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10V		6.5		nC
Q_{gd}	Gate-Drain Charge			14.4		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)}	Turn-Off-Delay Time	$V_{DD} = 30V, I_D = 17A,$		27		ns
t _f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		11		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Parameter Test Conditions Min.		Тур.	Max.	Unit
I _{SD} (3)	Source-drain Current				34	Α
I _{SDM} (2)	Source-drain Current (pulsed)				136	Α
V _{SD} (1)	Forward On Voltage	I _{SD} = 34 A, V _{GS} = 0			1.2	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 34 \text{ A}, \text{ di/dt} = 100 \text{A/} \mu \text{s},$		63		ns
Qrr	Reverse Recovery Charge	$V_{DD} = 10V$, $T_j = 150$ °C (see test circuit, Figure 5)		151		nC
I _{RRM}	Reverse Recovery Current	(SOC COST OFFICIALLY FINANCE OF		4.8		Α

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. Current Limited by Wire Bonding is 20A

Fig. 1: Unclamped Inductive Load Test Circuit

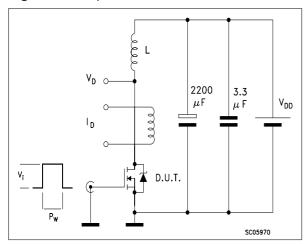


Fig. 3: Switching Times Test Circuit For Resistive Load

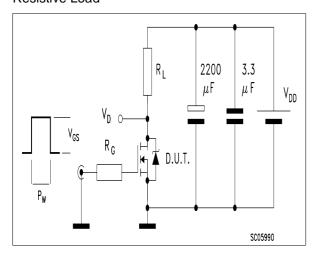


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

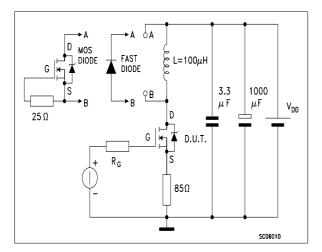


Fig. 2: Unclamped Inductive Waveform

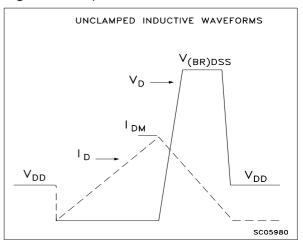
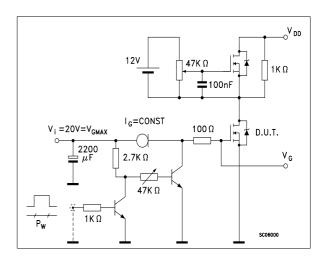


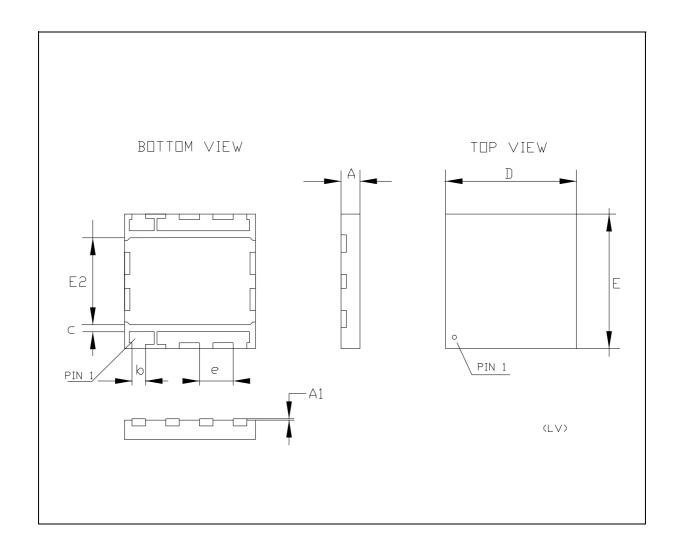
Fig. 4: Gate Charge test Circuit



4/6

PowerFLAT™(5x5) MECHANICAL DATA

DIM.		mm.				
DIIVI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
С	0.33	0.41	0.48	0.013	0.016	0.019
D		5.00			0.197	
E		5.00			0.197	
E2	3.10	3.18	3.25	0.122	0.125	0.128
е		1.27			0.050	



5/6

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States. © http://www.st.com

477.