



# 74VCXH162374

## LOW VOLTAGE CMOS 16-BIT D-TYPE FLIP-FLOP (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
  - $t_{PD} = 3.4 \text{ ns (MAX.)}$  at  $V_{CC} = 3.0 \text{ to } 3.6\text{V}$
  - $t_{PD} = 4.8 \text{ ns (MAX.)}$  at  $V_{CC} = 2.3 \text{ to } 2.7\text{V}$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  - $|I_{OH}| = I_{OL} = 12\text{mA (MIN)}$  at  $V_{CC} = 3.0\text{V}$
  - $|I_{OH}| = I_{OL} = 8\text{mA (MIN)}$  at  $V_{CC} = 2.3\text{V}$
- $26\Omega$  SERIE RESISTORS IN OUTPUTS
- OPERATING VOLTAGE RANGE:
  - $V_{CC(OPER)} = 2.3\text{V to } 3.6\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES H162374
- BUS HOLD PROVIDED ON DATA INPUTS
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORMANCE:
  - HBM > 2000V (MIL STD 883 method 3015);
  - MM > 200V

### DESCRIPTION

The 74VCXH162374 is a low voltage CMOS 16 BIT D-TYPE FLIP-FLOP with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and very high speed 2.3 to 3.6V applications; it can be interfaced to 3.6V signal environment for both inputs and outputs.

These 16 bit D-TYPE flip-flops are controlled by two clock inputs (nCK) and two output enable inputs (nOE).

On the positive transition of the (nCK), the nQ outputs will be set to the logic state that were setup at the nD inputs.

While the (nOE) input is low, the 8 outputs (nQ) will be in a normal state (HIGH or LOW logic level) and while high level the outputs will be in a high impedance state.

Any output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

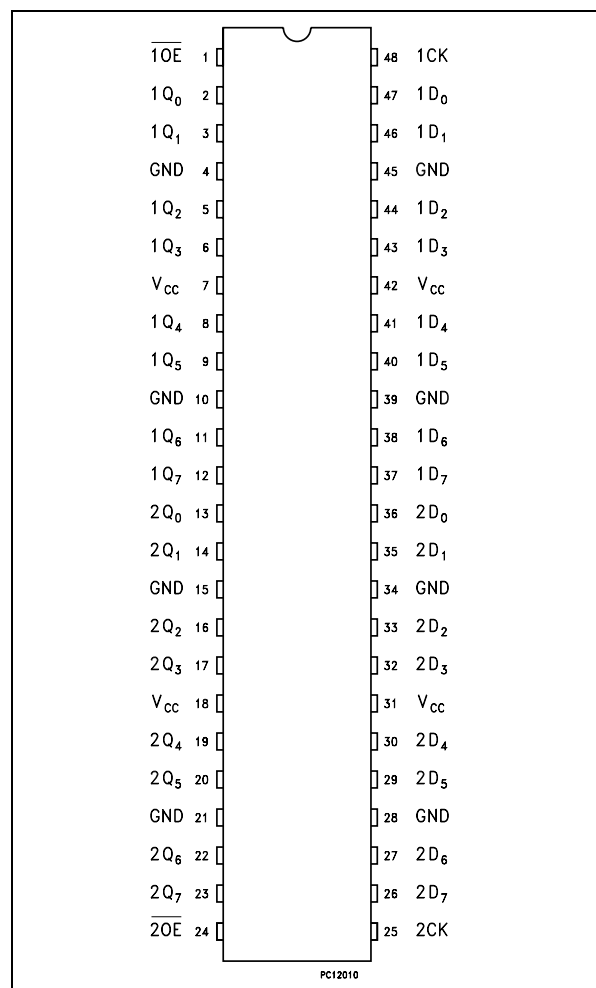
Bus hold on data inputs is provided in order to eliminate the need for external pull-up or pull-down resistor.



### ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74VCXH162374TTR

### PIN CONNECTION

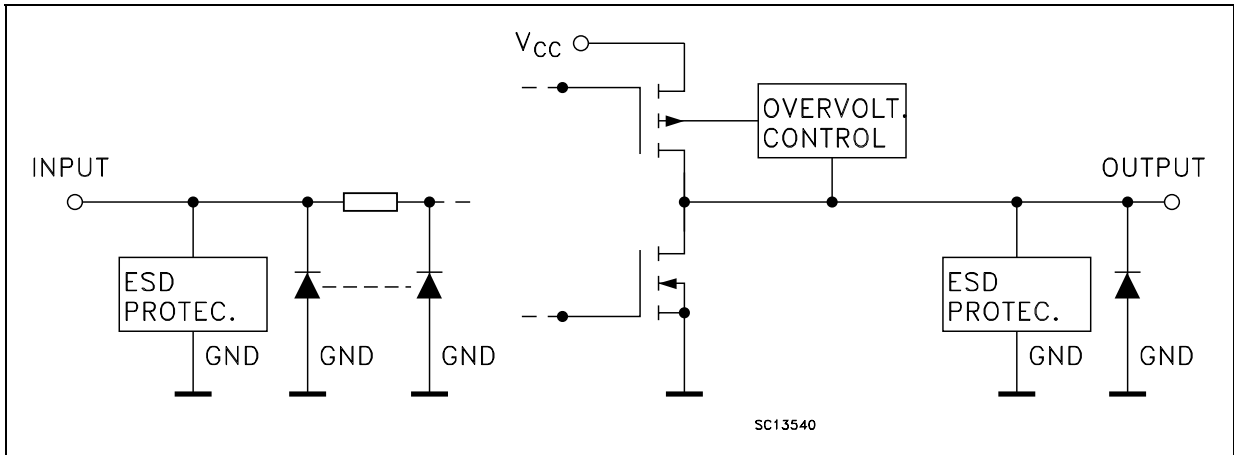


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The device circuit is including 26Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

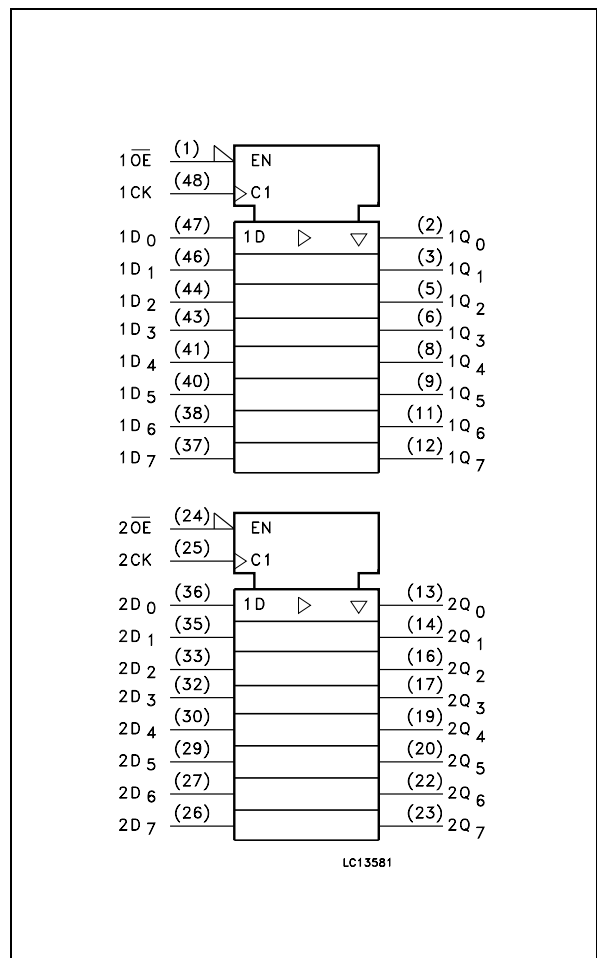
## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2CK	Clock Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1CK	Clock Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive Supply Voltage

## IEC LOGIC SYMBOLS

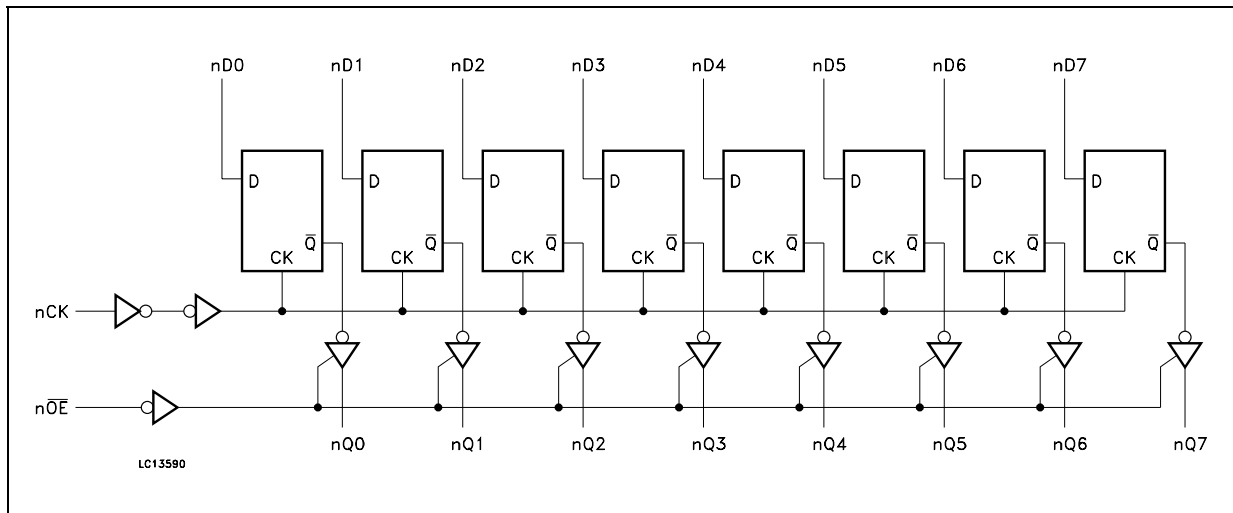


## TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE*
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance

## LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +4.6	V
$V_I$	DC Input Voltage	-0.5 to +4.6	V
$V_O$	DC Output Voltage (OFF State)	-0.5 to +4.6	V
$V_O$	DC Output Voltage (High or Low State) (note 1)	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 50	mA
$I_{OK}$	DC Output Diode Current (note 2)	- 50	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Supply Pin	$\pm 100$	mA
$P_D$	Power Dissipation	400	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

- 1)  $I_O$  absolute maximum rating must be observed  
 2)  $V_O < GND$ ,  $V_O > V_{CC}$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2.3 to 3.6	V
$V_I$	Input Voltage	-0.3 to 3.6	V
$V_O$	Output Voltage (OFF State)	0 to 3.6	V
$V_O$	Output Voltage (High or Low State)	0 to $V_{CC}$	V
$I_{OH}$ , $I_{OL}$	High or Low Level Output Current ( $V_{CC} = 3.0$ to $3.6V$ )	$\pm 12$	mA
$I_{OH}$ , $I_{OL}$	High or Low Level Output Current ( $V_{CC} = 2.3$ to $2.7V$ )	$\pm 8$	mA
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 1)	0 to 10	ns/V

- 1)  $V_{IN}$  from 0.8V to 2V at  $V_{CC} = 3.0V$

DC SPECIFICATIONS (2.7V < V<sub>CC</sub> ≤ 3.6V unless otherwise specified)

Symbol	Parameter	Test Condition		Value				Unit
		V <sub>CC</sub> (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
V <sub>IL</sub>	Low Level Input Voltage				0.8		0.8	
V <sub>OH</sub>	High Level Output Voltage	2.7 to 3.6	I <sub>O</sub> =-100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V
		2.7	I <sub>O</sub> =-6 mA	2.2		2.2		
		3.0	I <sub>O</sub> =-8 mA	2.4		2.4		
			I <sub>O</sub> =-12 mA	2.2		2.2		
V <sub>OL</sub>	Low Level Output Voltage	2.7 to 3.6	I <sub>O</sub> =100 μA		0.2		0.2	V
		2.7	I <sub>O</sub> =6 mA		0.4		0.4	
		3.0	I <sub>O</sub> =8 mA		0.55		0.55	
			I <sub>O</sub> =12 mA		0.8		0.8	
I <sub>I</sub>	Input Leakage Current	2.7 to 3.6	V <sub>I</sub> = 0 to 3.6V		± 5		± 5	μA
I <sub>I(HOLD)</sub>	Input Hold Current	3.0	V <sub>I</sub> = 0.8V	75		75		μA
			V <sub>I</sub> = 2V	-75		-75		
		3.6	V <sub>I</sub> = 0 to 3.6V		± 500		± 500	
I <sub>off</sub>	Power Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6V		10		10	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0 to 3.6V		± 10		± 10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 to 3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		20		20	μA
			V <sub>I</sub> or V <sub>O</sub> = V <sub>CC</sub> to 3.6V		± 20		± 20	
ΔI <sub>CC</sub>	I <sub>CC</sub> incr. per Input	2.7 to 3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		750		750	μA

**DC SPECIFICATIONS** ( $2.3V < V_{CC} \leq 2.7V$  unless otherwise specified)

Symbol	Parameter	Test Condition		Value				Unit
		V <sub>CC</sub> (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	2.3 to 2.7		1.6		1.6		V
V <sub>IL</sub>	Low Level Input Voltage				0.7		0.7	
V <sub>OH</sub>	High Level Output Voltage	2.3 to 2.7	I <sub>O</sub> =-100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V
			I <sub>O</sub> =-4 mA	2.0		2.0		
		2.3	I <sub>O</sub> =-6 mA	1.8		1.8		
			I <sub>O</sub> =-8 mA	1.7		1.7		
V <sub>OL</sub>	Low Level Output Voltage	2.3 to 2.7	I <sub>O</sub> =100 μA		0.2		0.2	V
			I <sub>O</sub> =6 mA		0.4		0.4	
		2.3	I <sub>O</sub> =8 mA		0.6		0.6	
I <sub>I</sub>	Input Leakage Current		2.3 to 2.7	V <sub>I</sub> = 0 to 3.6V		± 5		± 5
I <sub>I(HOLD)</sub>	Input Hold Current	2.3	V <sub>I</sub> = 0.7V	45		45		μA
			V <sub>I</sub> = 1.7V	-45		-45		
I <sub>off</sub>	Power Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6V		10		10	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	2.3 to 2.7	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0 to 3.6V		± 10		± 10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3 to 2.7	V <sub>I</sub> = V <sub>CC</sub> or GND		20		20	μA
			V <sub>I</sub> or V <sub>O</sub> = V <sub>CC</sub> to 3.6V		± 20		± 20	

**DYNAMIC SWITCHING CHARACTERISTICS** (T<sub>a</sub> = 25°C, Input t<sub>r</sub> = t<sub>f</sub> = 2.0ns, C<sub>L</sub> = 30pF, R<sub>L</sub> = 500Ω)

Symbol	Parameter	Test Condition		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min.	Typ.	Max.	
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 3)	2.5	V <sub>IL</sub> = 0V		0.25		V
		3.3	V <sub>IH</sub> = V <sub>CC</sub>		0.35		
V <sub>OLV</sub>	Dynamic Low Voltage Quiet Output (note 1, 3)	2.5	V <sub>IL</sub> = 0V		-0.25		V
		3.3	V <sub>IH</sub> = V <sub>CC</sub>		-0.35		
V <sub>OHV</sub>	Dynamic High Voltage Quiet Output (note 2, 3)	2.5	V <sub>IL</sub> = 0V		2.05		V
		3.3	V <sub>IH</sub> = V <sub>CC</sub>		2.65		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

2) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.

3) Parameters guaranteed by design.

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 30\text{pF}$ ,  $R_L = 500\Omega$ , Input  $t_r = t_f = 2.0\text{ns}$ )

Symbol	Parameter	Test Condition		Value				Unit
		$V_{CC}$ (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time CK to Qn	2.3 to 2.7		1.0	4.8	1.0	5.5	ns
		3.0 to 3.6		0.8	3.4	0.8	4.0	
$t_{PZL}$ $t_{PZH}$	Output Enable Time	2.3 to 2.7		1.0	5.4	1.0	6.2	ns
		3.0 to 3.6		0.8	3.9	0.8	4.5	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time	2.3 to 2.7		1.0	4.4	1.0	5.1	ns
		3.0 to 3.6		0.8	4.0	0.8	4.6	
$t_s$	Setup Time, HIGH or LOW level Dn to CK	2.3 to 2.7		1.0		1.0		ns
		3.0 to 3.6		1.0		1.0		
$t_h$	Hold Time High or LOW level Dn to CK	2.3 to 2.7		1.5		1.5		ns
		3.0 to 3.6		1.5		1.5		
$t_w$	CK Pulse Width, HIGH	2.3 to 2.7		1.5		1.5		ns
		3.0 to 3.6		1.5		1.5		
$f_{MAX}$	Clock Pulse Frequency	2.3 to 2.7		200		190		MHz
		3.0 to 3.6		250		235		
$t_{OSLH}$ $t_{OSHL}$	Output To Output Skew Time (note1, 2)	2.3 to 2.7			0.5		0.5	ns
		3.0 to 3.6			0.5		0.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ )

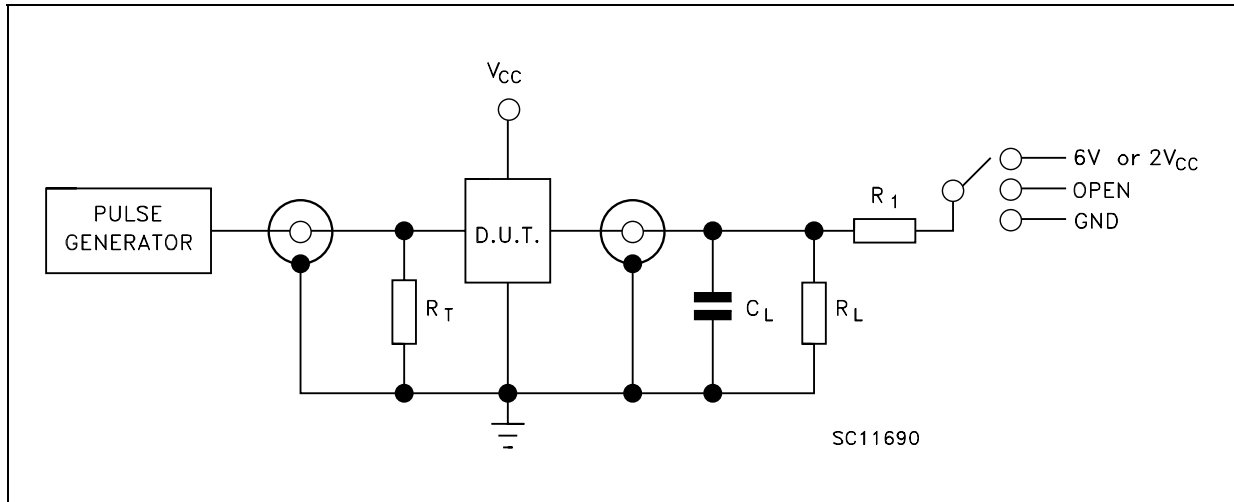
2) Parameter guaranteed by design

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value			Unit
		$V_{CC}$ (V)		$T_A = 25\text{ °C}$			
				Min.	Typ.	Max.	
$C_{IN}$	Input Capacitance	2.5 or 3.3	$V_{IN} = 0$ or $V_{CC}$		6		pF
$C_{OUT}$	Output Capacitance	2.5 or 3.3	$V_{IN} = 0$ or $V_{CC}$		7		pF
$C_{PD}$	Power Dissipation Capacitance (note 1)	2.5 or 3.3	$f_{IN} = 10\text{MHz}$ $V_{IN} = 0$ or $V_{CC}$		20		pF

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$  (per circuit)

## TEST CIRCUIT



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 3.0$ to $3.6V$ )	6V
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 2.3$ to $2.7V$ )	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 30$  pF or equivalent (includes jig and probe capacitance)

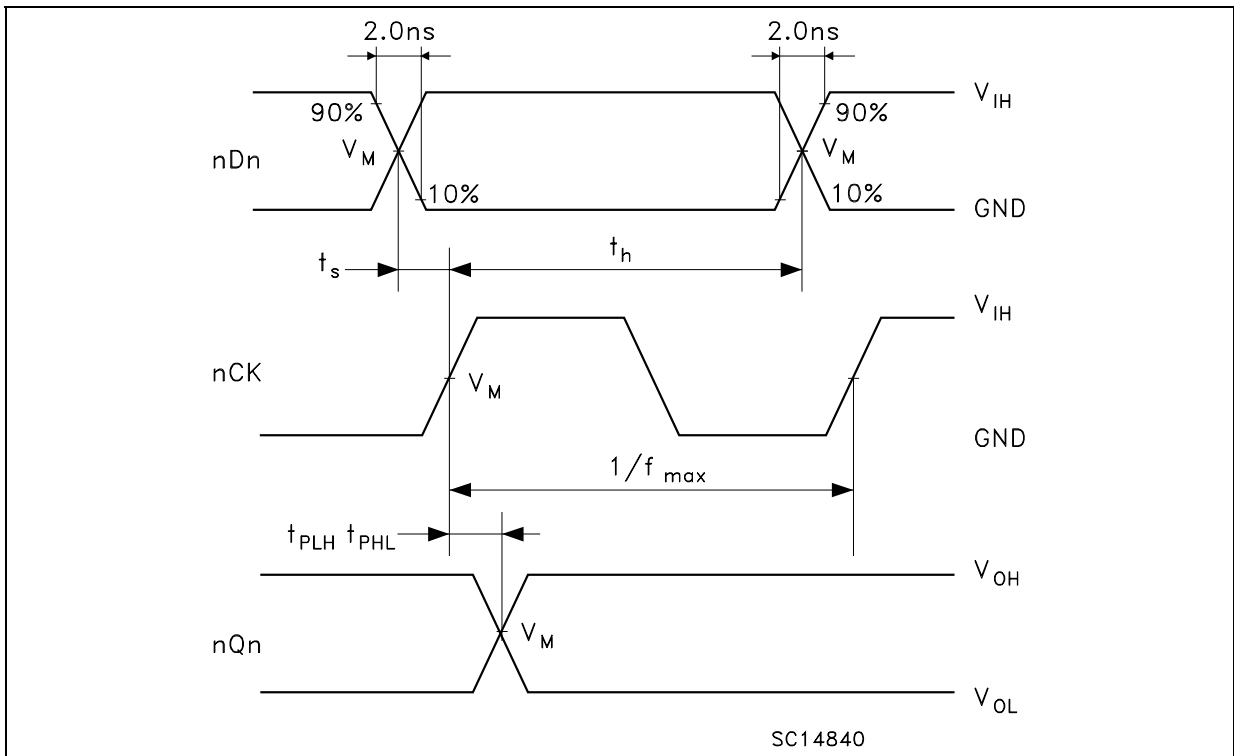
$R_L = R_1 = 500\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

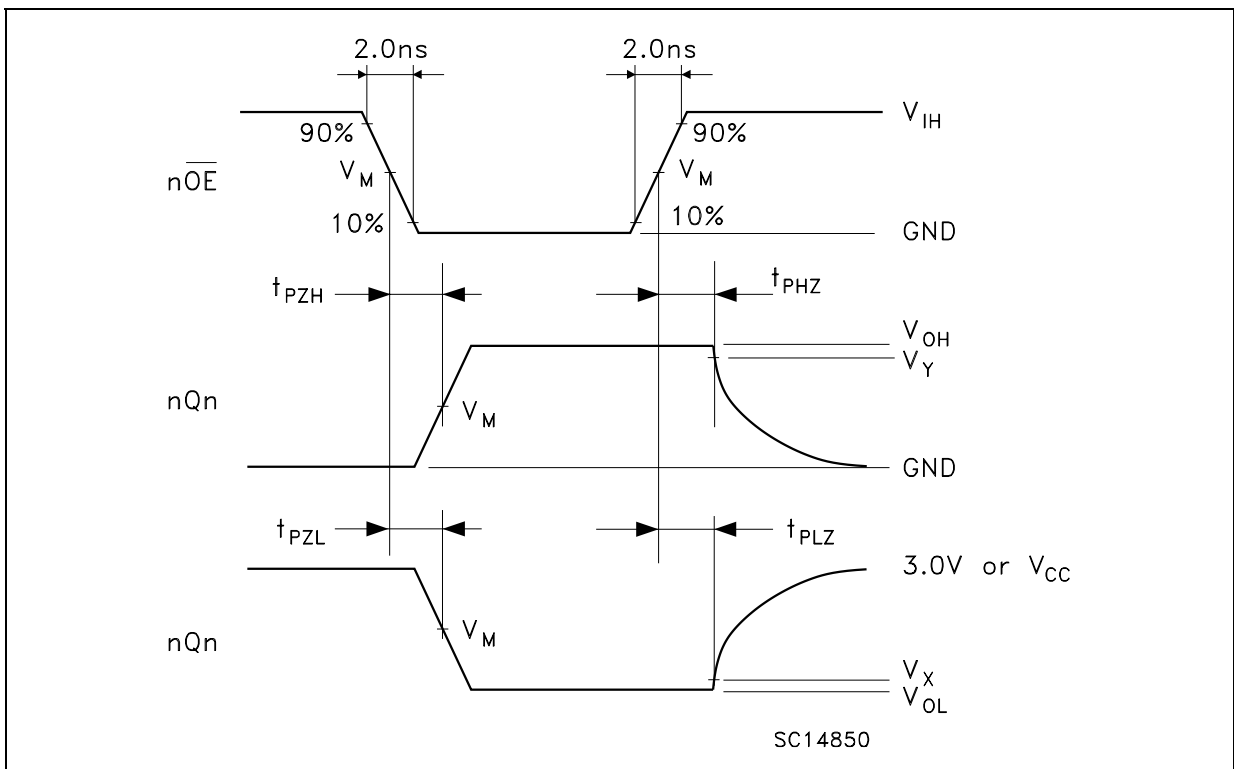
## WAVEFORM SYMBOL VALUES

Symbol	$V_{CC}$	
	3.0 to 3.6V	2.3 to 2.7V
$V_{IH}$	2.7V	$V_{CC}$
$V_M$	1.5V	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

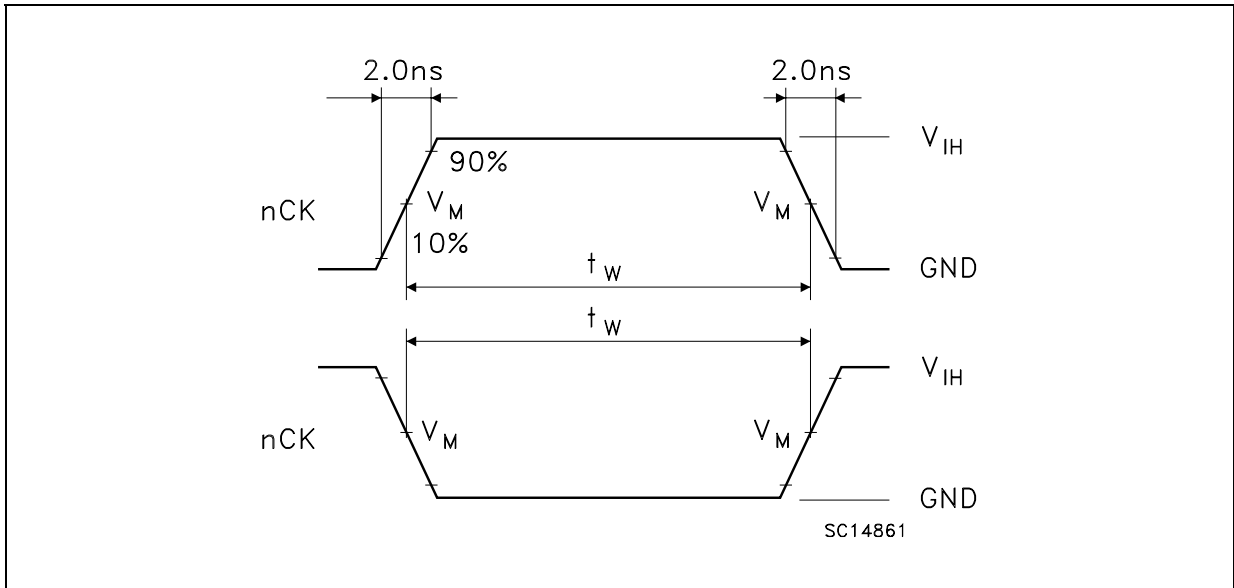
**WAVEFORM 1 : nCK TO Qn PROPAGATION DELAYS, nCK MAXIMUM FREQUENCY, Dn TO nCK SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)**



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)**

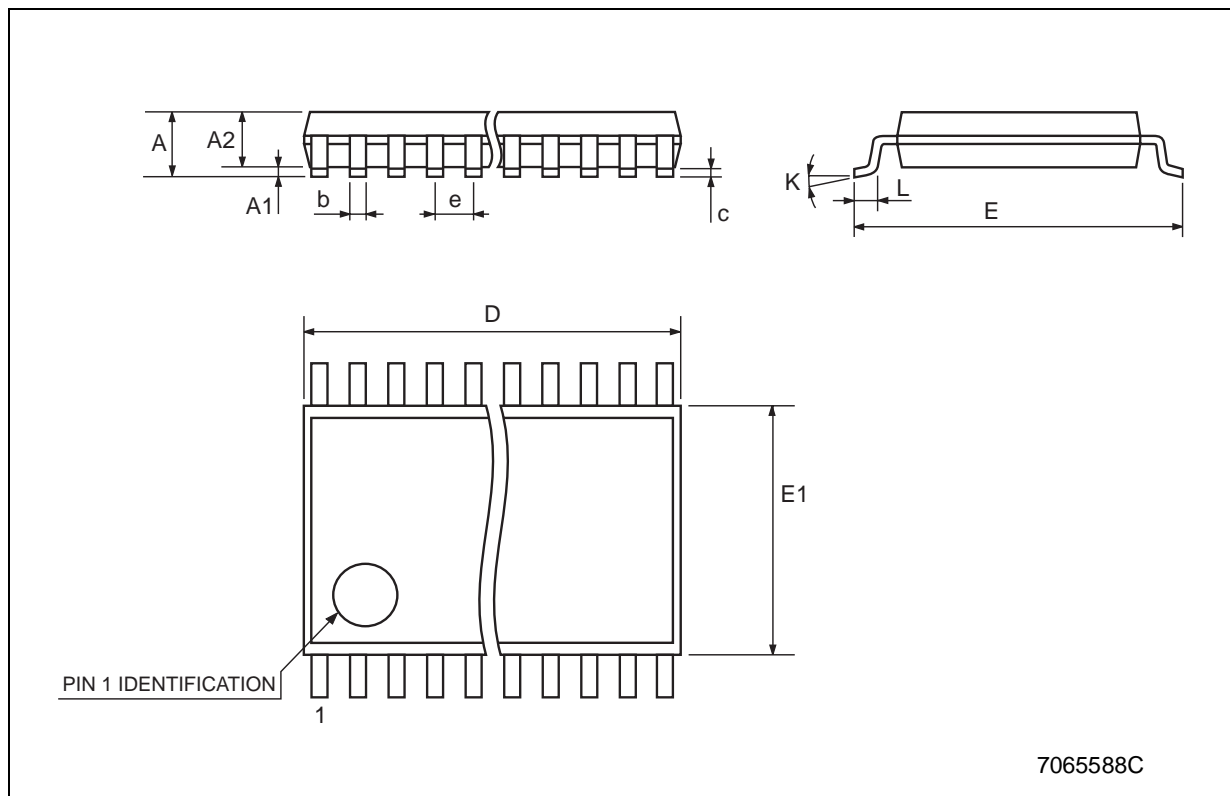




**WAVEFORM 3 : nCK MINIMUM PULSE WIDTH (f=1MHz; 50% duty cycle)**

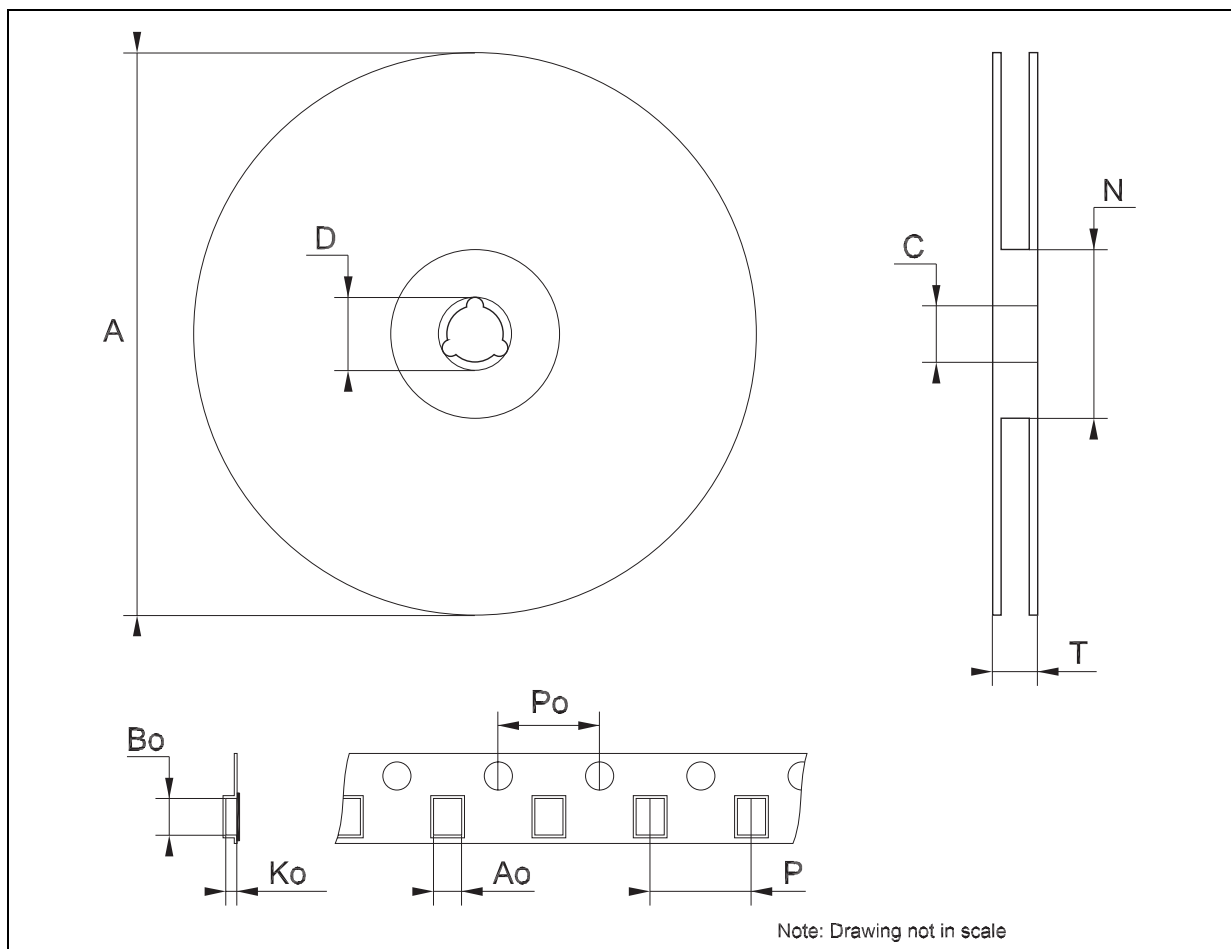
## TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



### Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



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