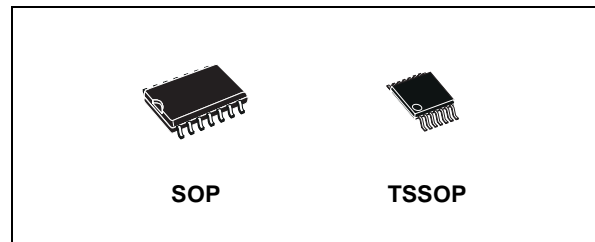


## DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:  
 $f_{MAX} = 170 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 2 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 2\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74VHC74M	74VHC74MTR
TSSOP		74VHC74TTR

### DESCRIPTION

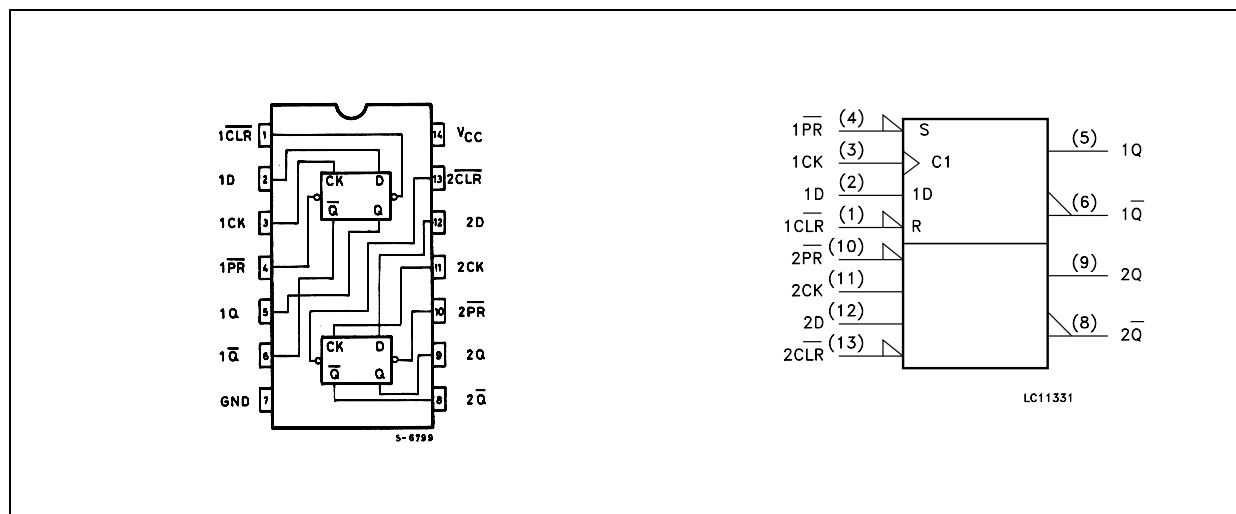
The 74VHC74 is an advanced high-speed CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. A signal on the D INPUT is transferred to the Q OUTPUTS during the positive going transition of the clock pulse.

$\overline{\text{CLR}}$  and  $\overline{\text{PR}}$  are independent of the clock and accomplished by a low setting on the appropriate input.

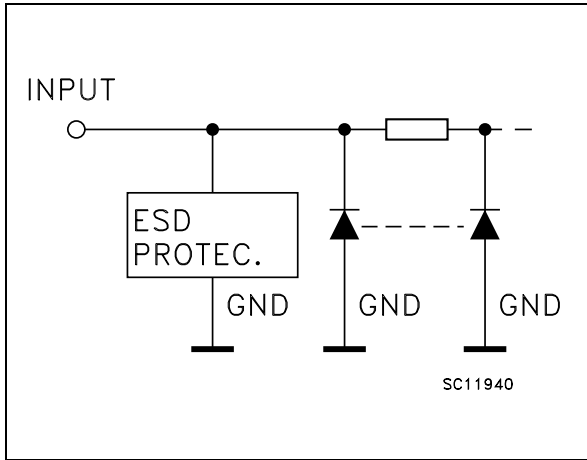
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

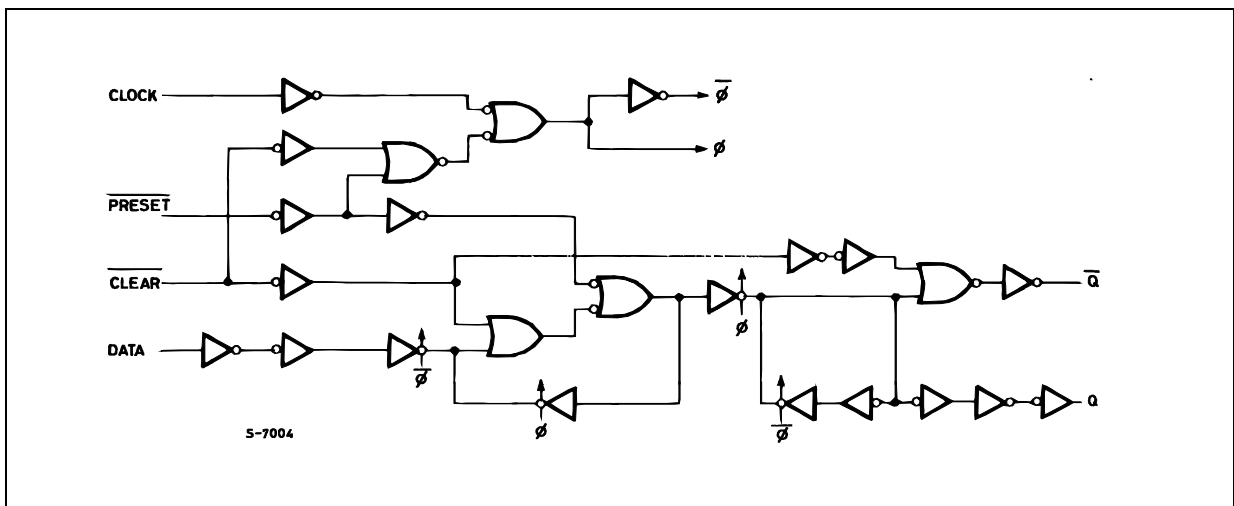
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1CLR}, \overline{2CLR}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW to HIGH, Edge Triggered)
4, 10	1PR, 2PR	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$\overline{1Q}, \overline{2Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L		L	H	
H	H	H		H	L	
H	H	X		Q <sub>n</sub>	$\overline{Q}_n$	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 1) ( $V_{CC} = 3.3 \pm 0.3V$ ) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 100 0 to 20	ns/V

1)  $V_{IN}$  from 30% to 70% of  $V_{CC}$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V <sub>CC</sub>			0.7V <sub>CC</sub>		0.7V <sub>CC</sub>		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V <sub>CC</sub>		0.3V <sub>CC</sub>		0.3V <sub>CC</sub>	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I <sub>O</sub> =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I <sub>O</sub> =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I <sub>O</sub> =-4 mA	2.58			2.48		2.4		
		4.5	I <sub>O</sub> =-8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	
		3.0	I <sub>O</sub> =4 mA			0.36		0.44		0.55	
		4.5	I <sub>O</sub> =8 mA			0.36		0.44		0.55	
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			2		20		20	μA

AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 3\text{ns}$ )

Symbol	Parameter	Test Condition			Value						Unit	
		$V_{CC}$ (V)	$C_L$ (pF)	$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time CK to Q or $\bar{Q}$	3.3 <sup>(*)</sup>	15			6.7	11.9	1.0	14.0	1.0	14.0	ns
		3.3 <sup>(*)</sup>	50			9.2	15.4	1.0	17.5	1.0	17.5	
		5.0 <sup>(**)</sup>	15			4.6	7.3	1.0	8.5	1.0	8.5	
		5.0 <sup>(**)</sup>	50			6.1	9.3	1.0	10.5	1.0	10.5	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time $\overline{\text{PR}}$ or $\overline{\text{CLR}}$ to Q or $\bar{Q}$	3.3 <sup>(*)</sup>	15			7.6	12.3	1.0	14.5	1.0	14.5	ns
		3.3 <sup>(*)</sup>	50			10.1	15.8	1.0	18.0	1.0	18.0	
		5.0 <sup>(**)</sup>	15			4.8	7.7	1.0	9.0	1.0	9.0	
		5.0 <sup>(**)</sup>	50			6.3	9.7	1.0	11.0	1.0	11.0	
$t_W$	CK Pulse Width HIGH or LOW	3.3 <sup>(*)</sup>				6.0		7.0		7.0	ns	
		5.0 <sup>(**)</sup>				5.0		5.0		5.0		
$t_W$	$\overline{\text{PR}}$ or $\overline{\text{CLR}}$ Pulse Width LOW	3.3 <sup>(*)</sup>				6.0		7.0		7.0	ns	
		5.0 <sup>(**)</sup>				5.0		5.0		5.0		
$t_S$	Setup Time D to CK HIGH or LOW	3.3 <sup>(*)</sup>				6.0		7.0		7.0	ns	
		5.0 <sup>(**)</sup>				5.0		5.0		5.0		
$t_H$	Hold Time D to CK HIGH or LOW	3.3 <sup>(*)</sup>				0.5		0.5		0.5	ns	
		5.0 <sup>(**)</sup>				0.5		0.5		0.5		
$t_{\text{REM}}$	Removal Time $\overline{\text{PR}}$ or $\overline{\text{CLR}}$ to CK	3.3 <sup>(*)</sup>				5.0		5.0		5.0	ns	
		5.0 <sup>(**)</sup>				3.0		3.0		3.0		
$f_{\text{MAX}}$	Maximum Clock Frequency	3.3 <sup>(*)</sup>	15		80	125		70		70	MHz	
		3.3 <sup>(*)</sup>	50		50	75		45		45		
		5.0 <sup>(**)</sup>	15		130	170		110		110		
		5.0 <sup>(**)</sup>	50		90	115		75		75		

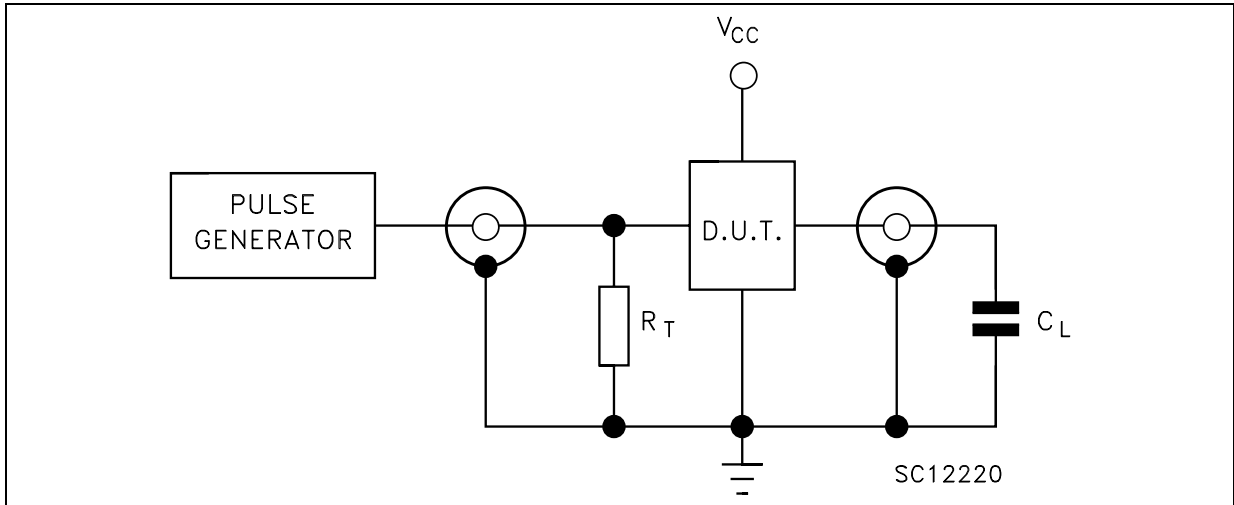
(\*) Voltage range is  $3.3\text{V} \pm 0.3\text{V}$ (\*\*) Voltage range is  $5.0\text{V} \pm 0.5\text{V}$ 

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{\text{IN}}$	Input Capacitance	5.0			7	10		10		10	pF
$C_{\text{PD}}$	Power Dissipation Capacitance (note 1)	5.0	$f_{\text{IN}} = 10\text{MHz}$		25						pF

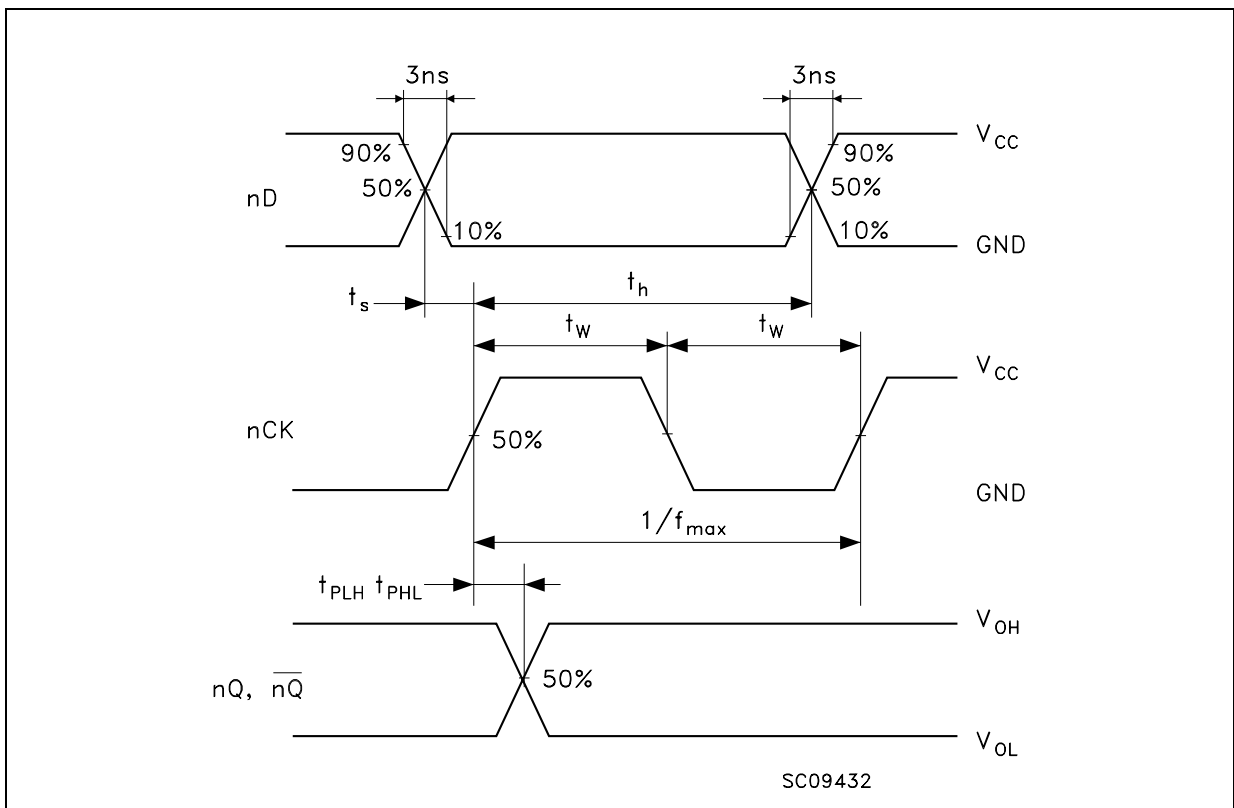
1)  $C_{\text{PD}}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{\text{CC(oper)}} = C_{\text{PD}} \times V_{\text{CC}} \times f_{\text{IN}} + I_{\text{CC}/2}$  (per flip-flop)

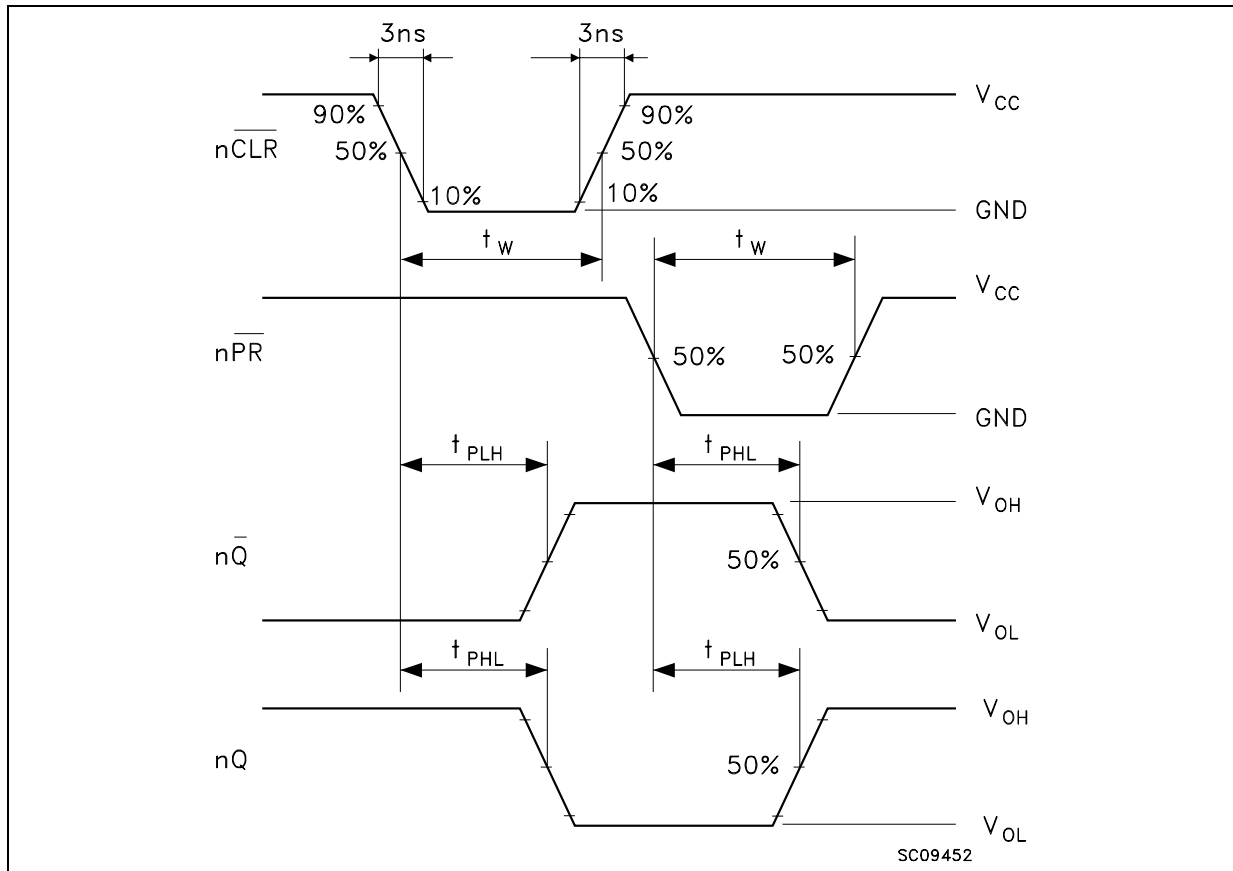
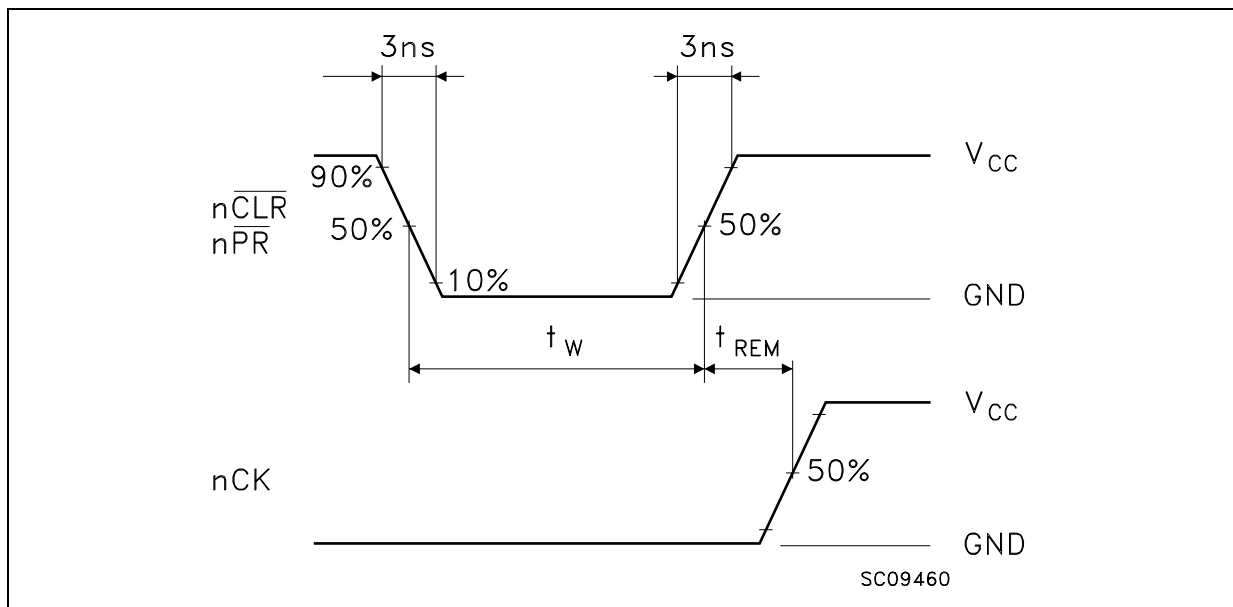
TEST CIRCUIT



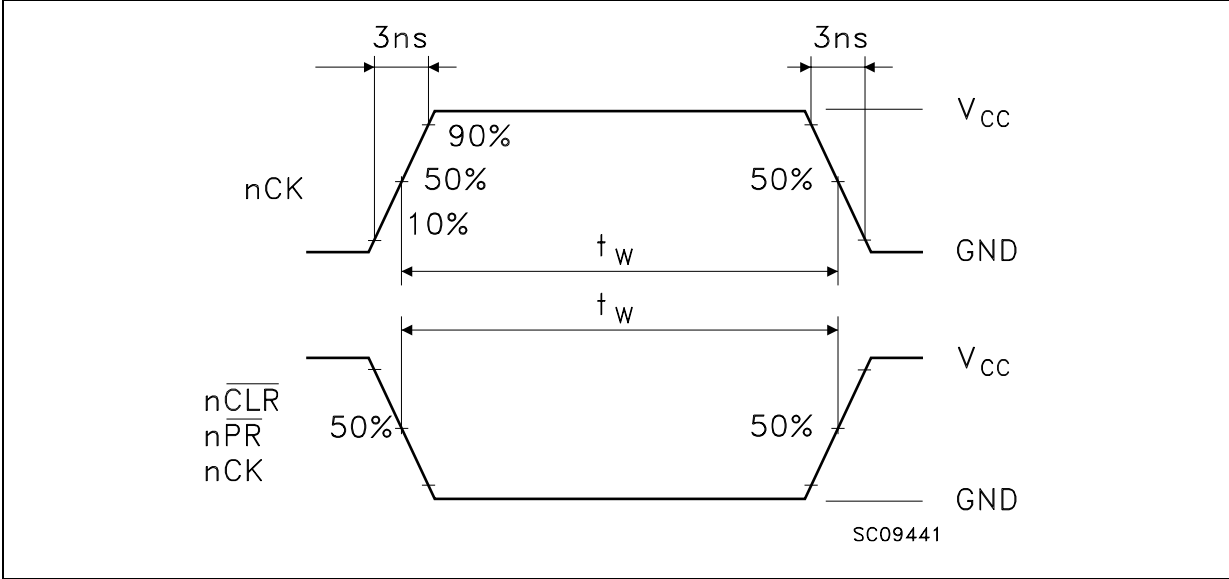
$C_L = 15/50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: PROPAGATION DELAYS** ( $f=1\text{MHz}$ ; 50% duty cycle)**WAVEFORM 3: RECOVERY TIMES** ( $f=1\text{MHz}$ ; 50% duty cycle)

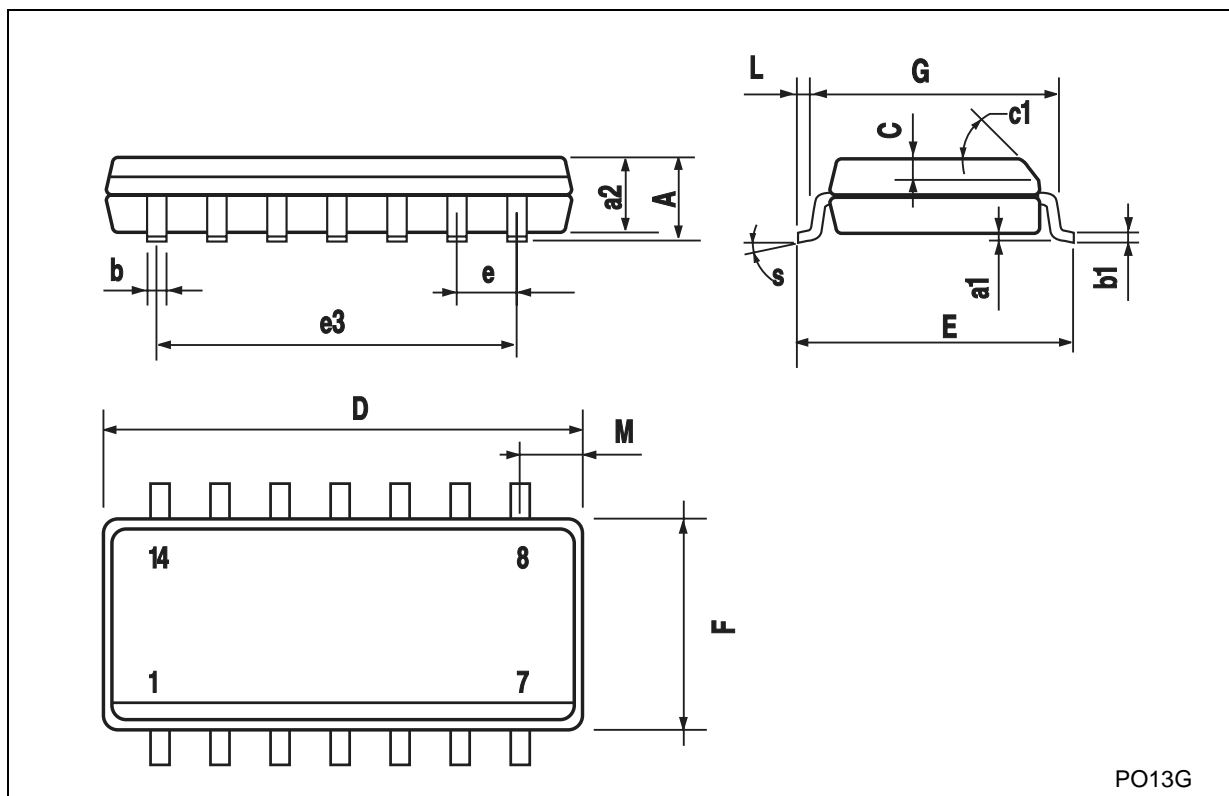
WAVEFORM 4: PULSE WIDTH





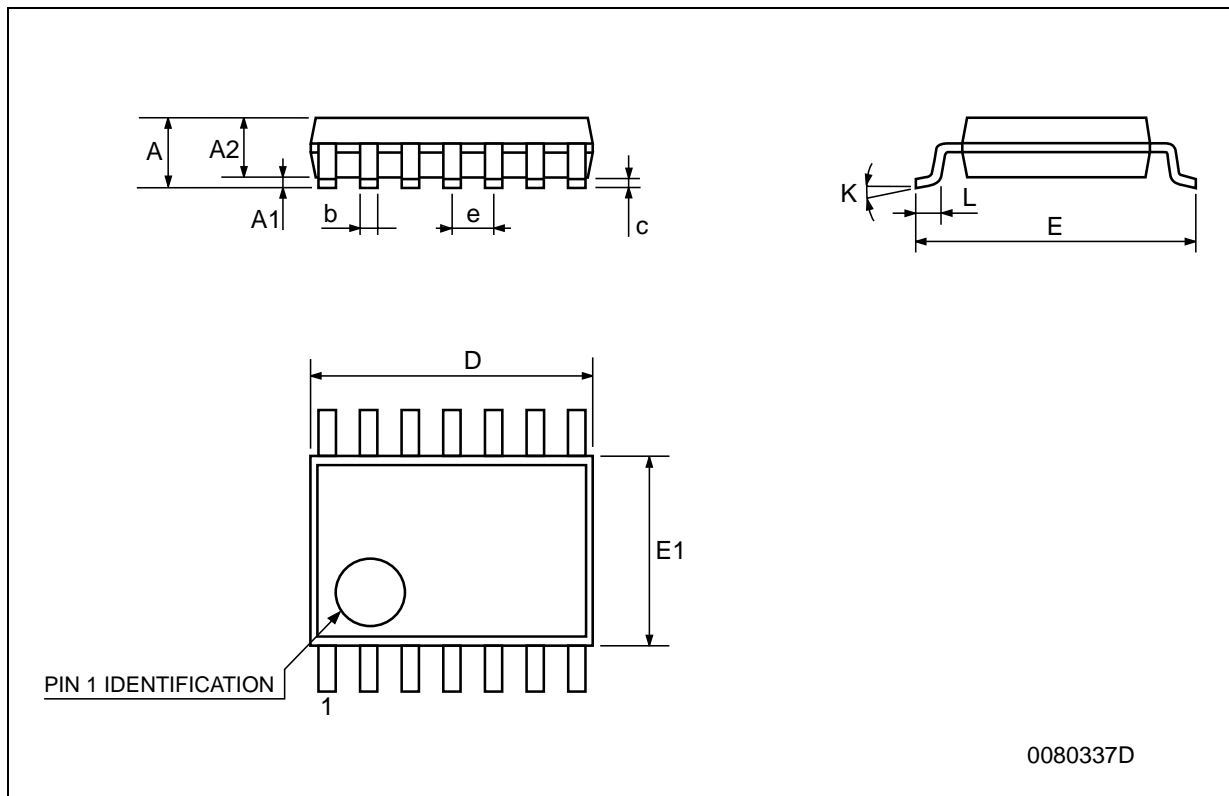
## SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



## TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

