ESDA14V2-4BF1

QUAD BIDIRECTIONAL TRANSIL™ ARRAY FOR ESD PROTECTION

A.S.D™

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals.

DESCRIPTION

The ESDA14V2-4BF1 is a monolithic array designed to protect up to 4 lines in a bidirectional way against ESD transients.

The device is ideal for situations where board space saving is requested.

FEATURES

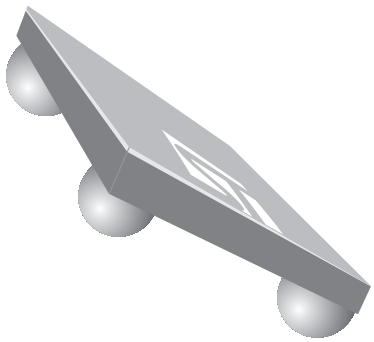
- 4 Bidirectional Transil™ functions
- ESD Protection: IEC61000-4-2 level 4
- Stand off voltage: 12 V MIN.
- Low leakage current < 1 µA
- 50W Peak pulse power (8/20)

BENEFITS

- High ESD protection level
- High integration
- Suitable for high density boards

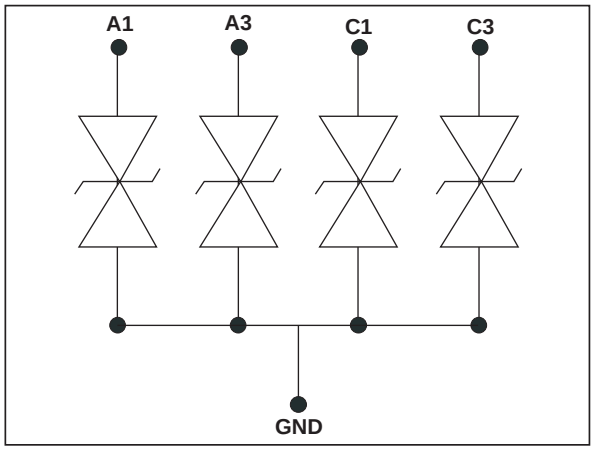
COMPLIES WITH THE FOLLOWING STANDARDS:

- IEC61000-4-2: 15 kV (air discharge)
  8 kV (contact discharge)
- MIL STD 883E-Method 3015-7: class3
  25kV (Human Body Model)

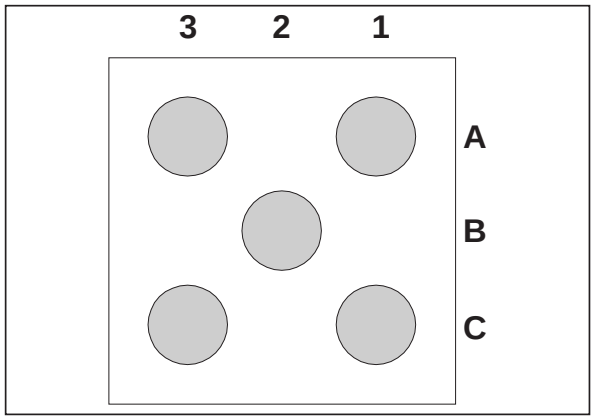


Flip Chip package

FUNCTIONAL DIAGRAM



PIN CONFIGURATION (Ball Side)



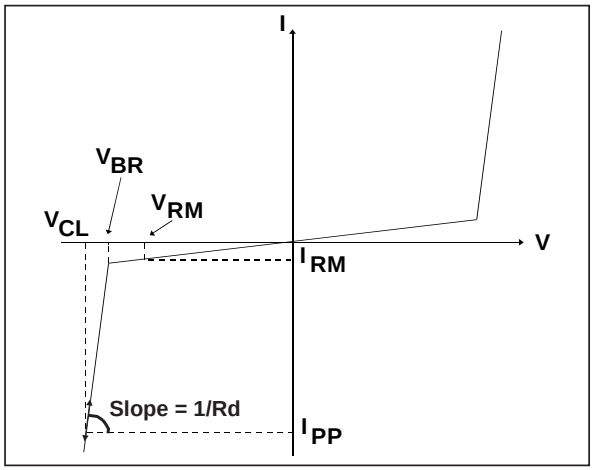
ABSOLUTE RATINGS (T_{amb} = 25°C)

Symbol	Test conditions	Value	Unit
V_{PP}	ESD discharge - MIL STD 883E - Method 3015-7 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	±25 ±15 ± 8	kV
P_{PP}	Peak pulse power (8/20µs)	50	W
T_j	Junction temperature	125	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_L	Lead solder temperature (10 seconds duration)	260	°C
T_{op}	Operating temperature range (note 1)	-40 to +125	°C

Note 1: Variation of parameters will be given in the final datasheet

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
C	Capacitance
Rd	Dynamic resistance



Type	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C
	min.	max.		max.		typ. note 1	max. note 2	max 0V bias
	V	V	mA	µA	V	Ω	10^{-4}/°C	pF
ESDA14V2- 4BF1	14.2	18	1	1	12	3.2	10	15
				0.1	3			

Note 1: Square pulse, IPP = 3A, tp = 2.5µs

Note 2: ΔVBR = αT(Tamb-25°C) x VBR(25°C)

Fig. 1: Clamping voltage versus peak pulse current (Tj initial = 25°C) Rectangular waveform tp = 2.5µs.

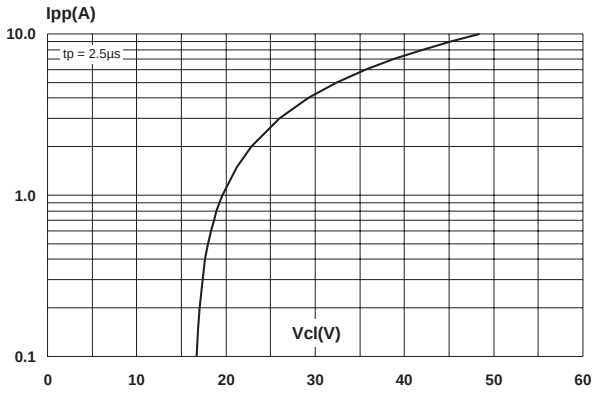


Fig. 2: Capacitance versus reverse applied voltage (typical values).

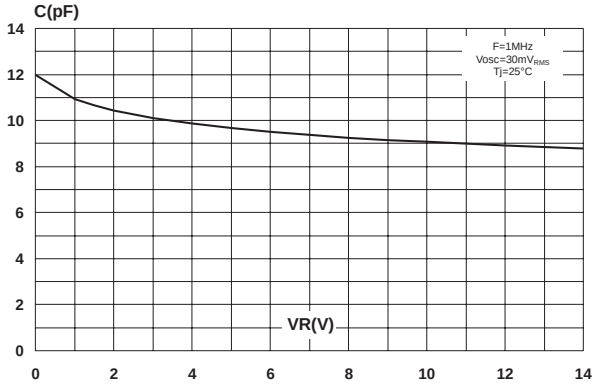
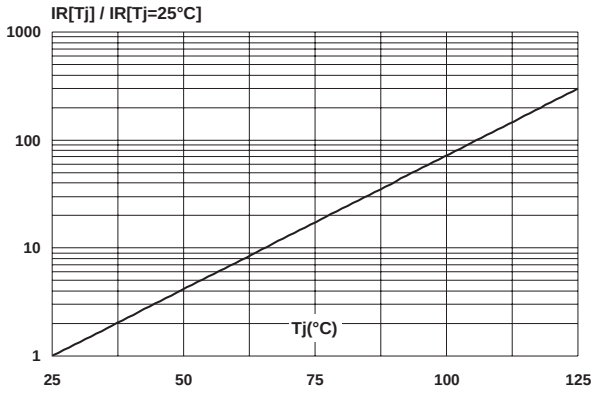
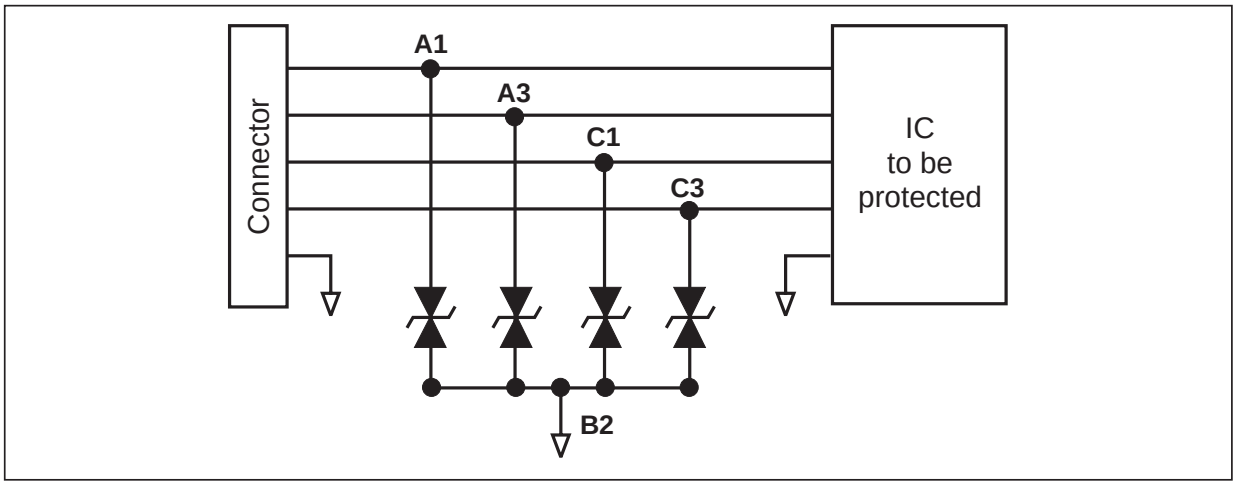


Fig. 3: Relative variation of leakage current versus junction temperature (typical values).



APPLICATION EXAMPLE



TECHNICAL INFORMATION

1. ESD protection by ESDA14V2- 4BF1

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

As a transient voltage suppressor, ESDA14V2-4BF1 is an ideal choice for ESD protection by suppressing ESD events. It is capable of clamping the incoming transient to a low enough level such that any damage is prevented on the device protected by ESDA14V2-4BF1.

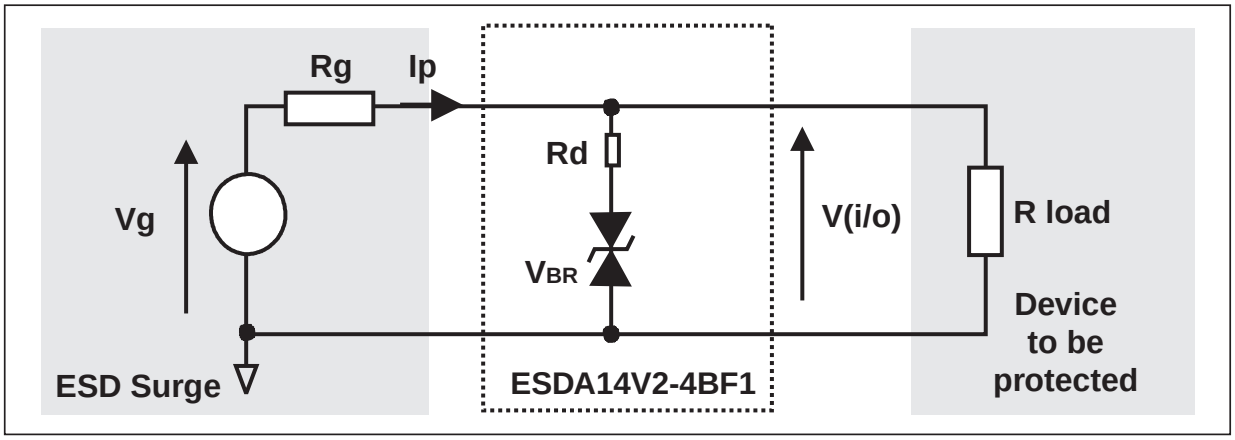
ESDA14V2-4BF1 serves as a parallel protection elements, connected between the signal line and ground. As the transient rises above the operating voltage of the device, the ESDA14V2-4BF1 becomes a low impedance path diverting the transient current to ground.

The clamping voltage is given by the following formula:

$$V_{CL} = V_{BR} + R_d.I_{pp}$$

As shown in figure A1, the ESD strikes are clamped by the transient voltage suppressor.

Fig. A1: ESD clamping behavior



To have a good approximation of the remaining voltages at both Vi/o side, we provide the typical dynamical resistance value Rd. By taking into account the following hypothesis :

$R_g > R_d$ and Rload > R_d

we have:

$$V(i/o) = V_{BR} + R_d \times \frac{V_g}{R_g}$$

The results of the calculation done for V_g = 8 kV, R_g = 330 Ω (IEC 61000-4-2 standard), V_{BR} = 14.2 V (min.) and R_d = 3.2 Ω (typ.) give:

V(i/o) = 91.8 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the Vi/o side.

V(i/o)

Fig. A2: ESD test board

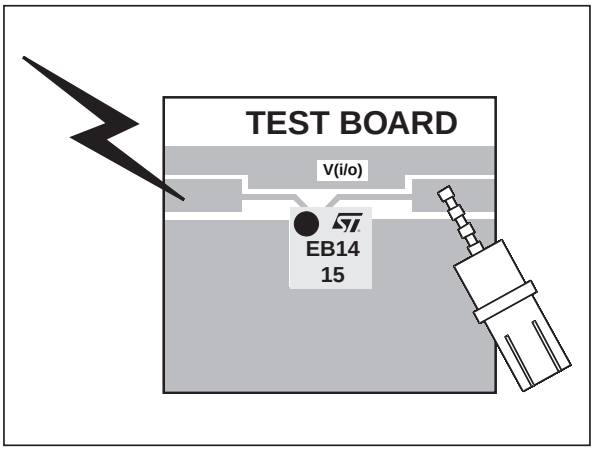
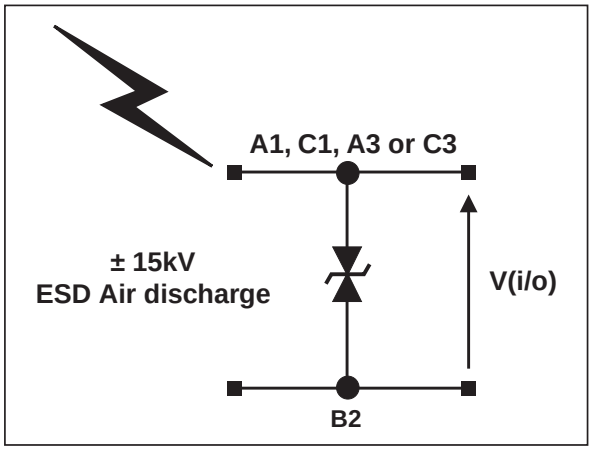
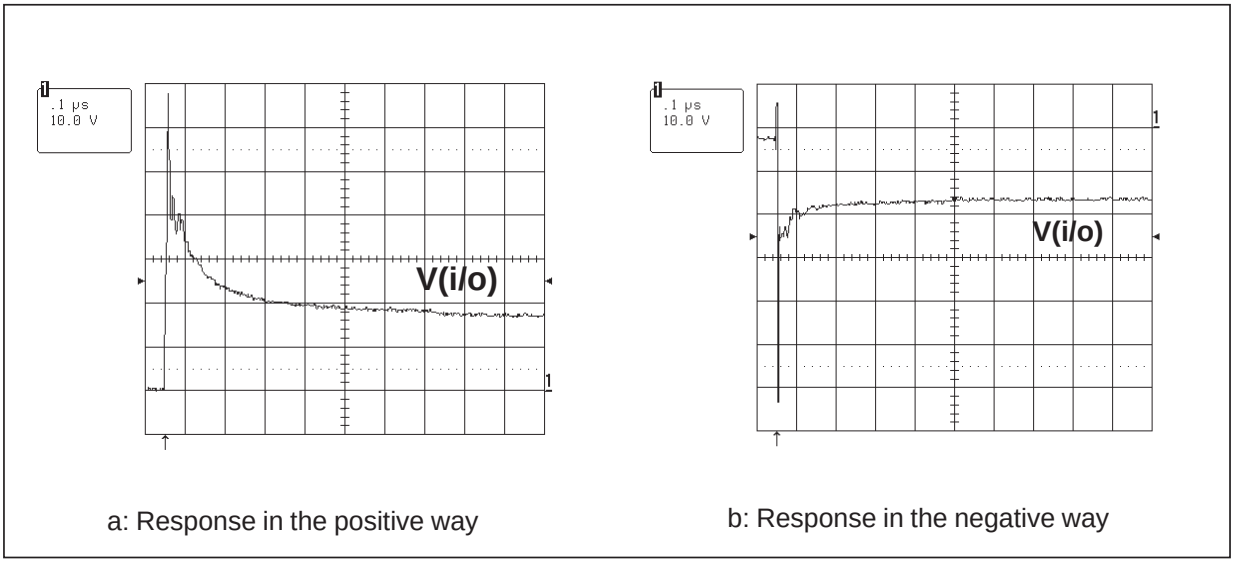


Fig. A3: ESD test configuration



The measurements done here after show very clearly (Fig. A4) the high efficiency of the ESD protection: the clamping voltage V(i/o) becomes very close to $+V_{BR}$ (positive way, Fig. A4a) and $-V_{BR}$ (negative way, Fig. A4b).

Fig. A4: Remaining voltage during ESD surge

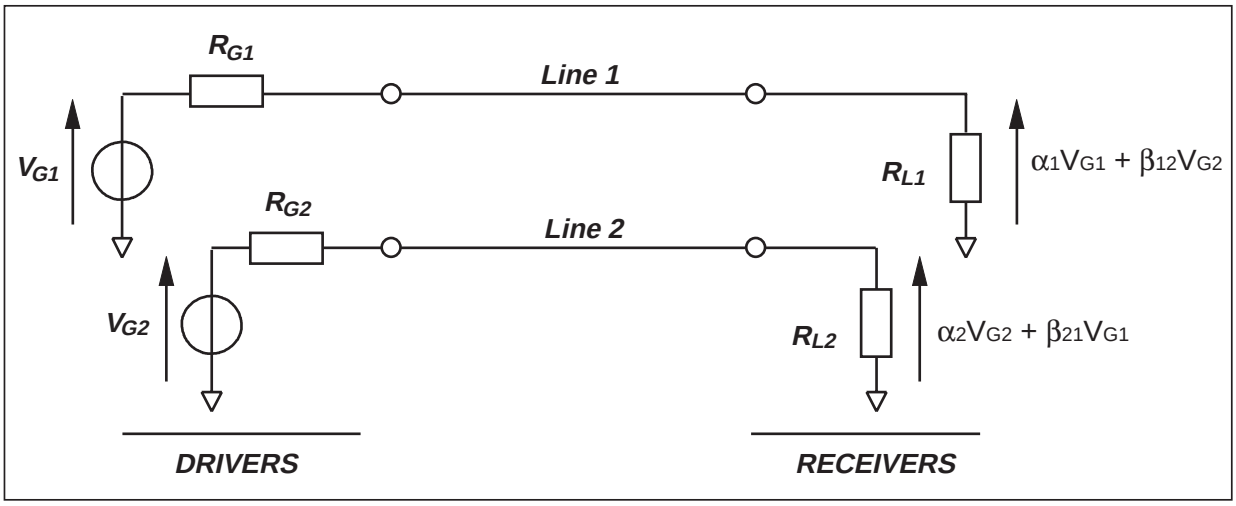


a: Response in the positive way

b: Response in the negative way

CROSSTALK BEHAVIOR

Fig. A5: Crosstalk phenomenon



The crosstalk phenomena are due to the coupling between 2 lines. Coupling factors ($\beta 12$ or $\beta 21$) increase when the gap across lines decreases, particularly in silicon dice. In the example above, the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G2}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals. The perturbed line will be more affected if it works with low voltage signal or high load

Fig. A6: Analog crosstalk measurements

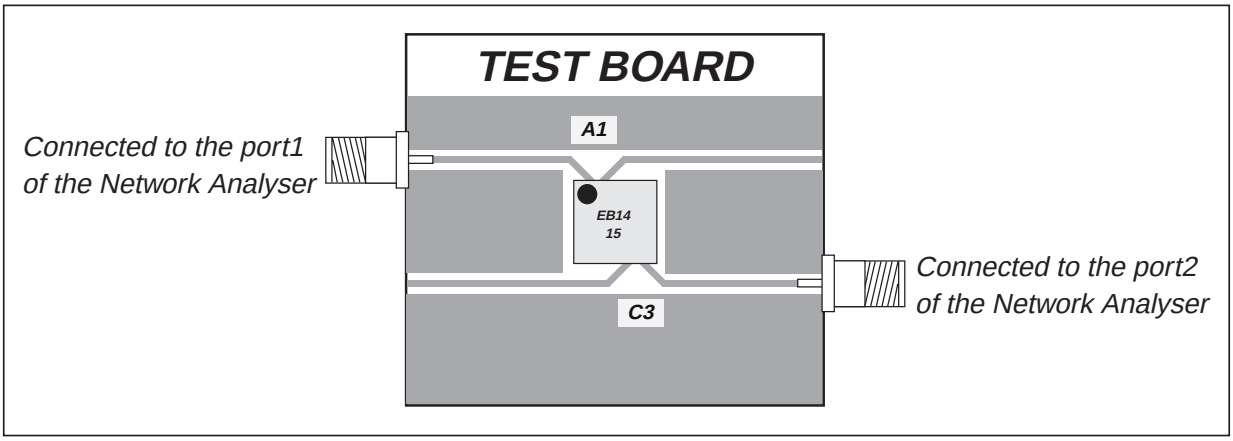


Fig. A7: Typical analog crosstalk measurements

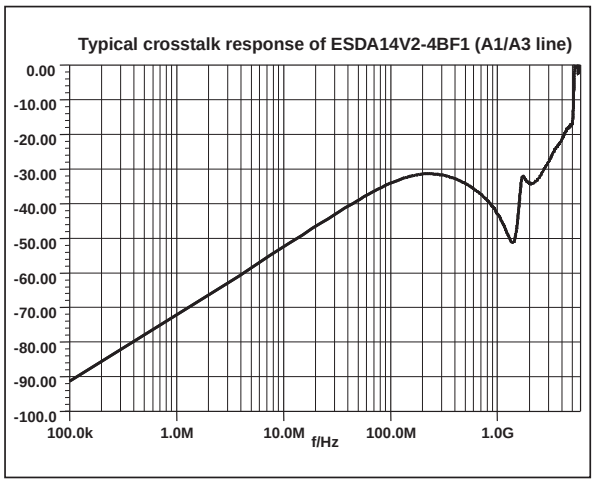


Figure A6 gives the measurement circuit for the analog crosstalk application. In figure A7, the curve shows the effect of the line A1 on the line A3. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -30dB.

Fig. A8: Digital crosstalk measurements configuration.

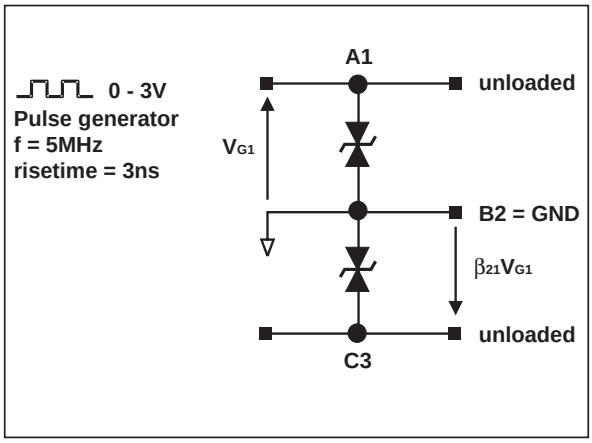


Fig. A9: Digital crosstalk results

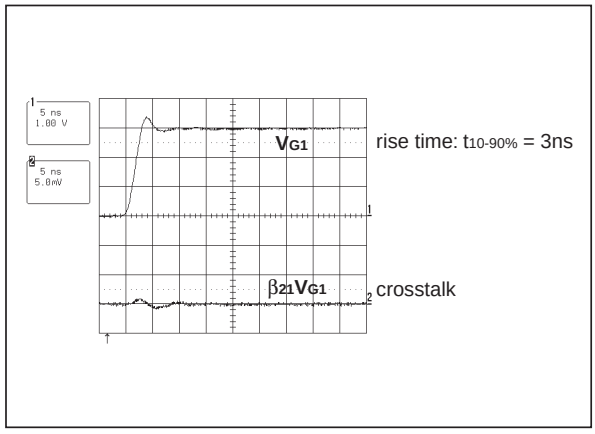
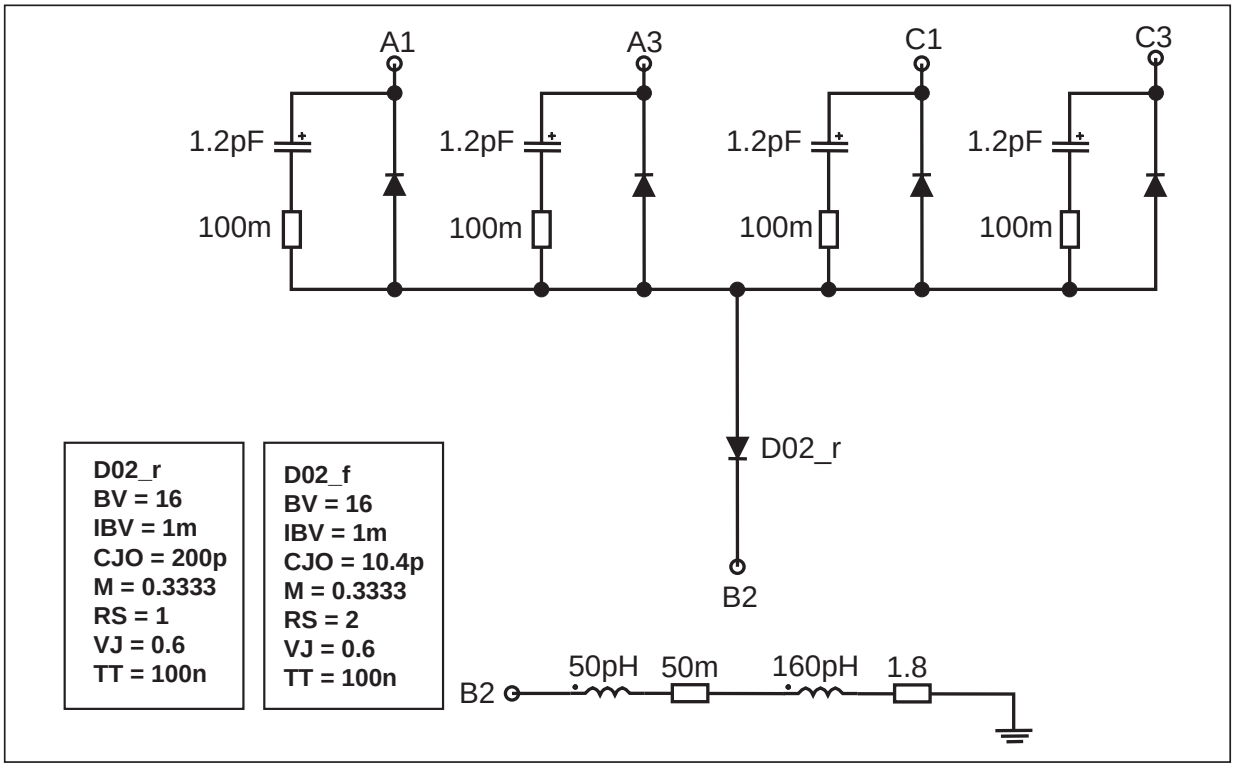
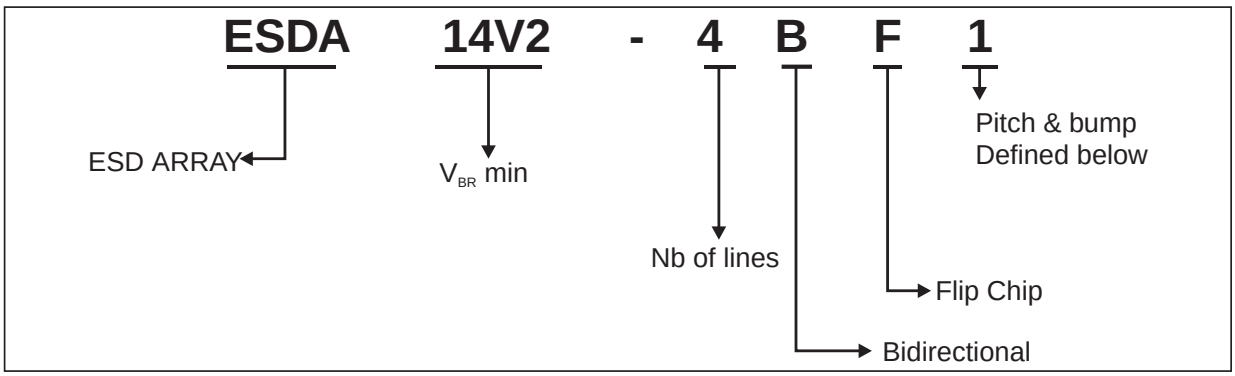


Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.
Figure A9 shows that in such a condition, the impact on the disturbed line is less than 50 mV peak to peak. No data disturbance was noted on the concerned line. The measurements performed with falling edges give an impact within the same range.

Fig. A10: Aplac model

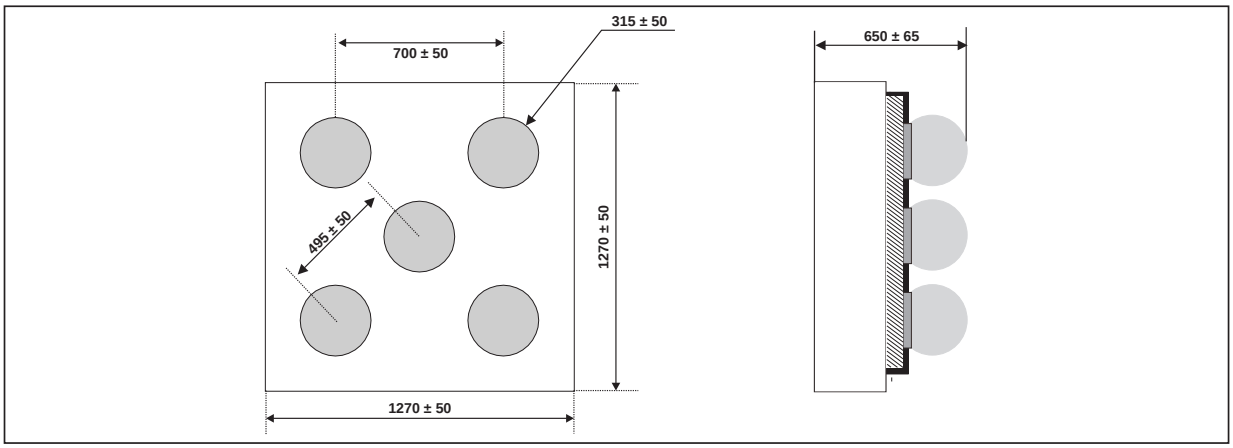


ORDER CODE

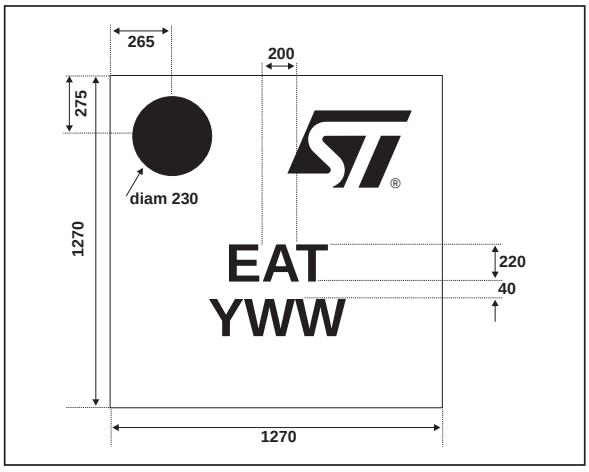


PACKAGE MECHANICAL DATA

DIE SIZE (all dimensions in µm)



MARKING



- YWW: Date code

OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
ESDA14V2-4BF1	EAT	Flip-Chip	2.1 mg	5000	Tape & reel 7”

Note: More packing informations are available in the application note AN1235: "Flip-Chip: Package description and recommandations for use"