



Application Specific Discretes  
A.S.D.

## ESDA6V1P6

### QUAD TRANSIL™ ARRAY FOR ESD PROTECTION

#### MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals.

#### FEATURES

- 4 UNIDIRECTIONAL TRANSIL™ FUNCTIONS.
- BREAKDOWN VOLTAGE  $V_{BR} = 6.1V$  MIN
- LOW LEAKAGE CURRENT  $< 500$  nA
- VERY SMALL PCB AREA  $< 2.6$  mm<sup>2</sup>

#### DESCRIPTION

The ESDA6V1P6 is a monolithic array designed to protect up to 4 lines against ESD transients.

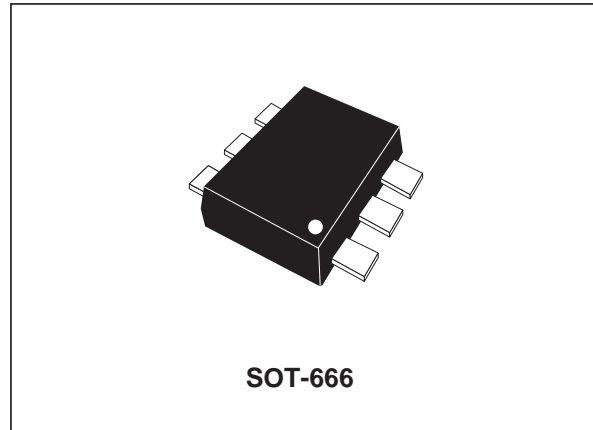
This device is ideal for applications where board space saving is required.

#### BENEFITS

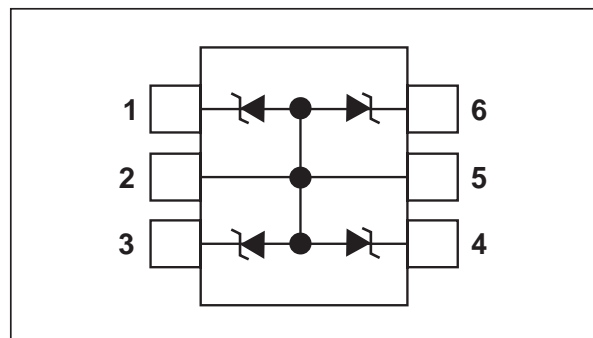
- High ESD protection level.
- High integration.
- Suitable for high density boards.

#### COMPLIES WITH THE FOLLOWING STANDARDS :

- IEC61000-4-2 level 4: 15 kV (air discharge)  
8 kV (contact discharge)
- MIL STD 883E-Method 3015-7: class 3  
25kV HBM (Human Body Model)



#### FUNCTIONAL DIAGRAM



# ESDA6V1P6

## ABSOLUTE RATINGS (T<sub>amb</sub> = 25°C)

Symbol	Parameter	Test conditions	Value	Unit
V <sub>PP</sub>	ESD discharge - IEC61000-4-2 air discharge IEC61000-4-2 contact discharge		± 15 ± 8	kV
P <sub>PP</sub>	Peak pulse power (8/20 μs) (see note 1)	T <sub>j</sub> initial = T <sub>amb</sub>	150	W
T <sub>j</sub>	Junction temperature		125	°C
T <sub>stg</sub>	Storage temperature range		- 55 to + 150	°C
T <sub>L</sub>	Maximum lead temperature for soldering during 10s at 5mm for case		260	°C
T <sub>op</sub>	Operating temperature range		- 40 to + 150	°C

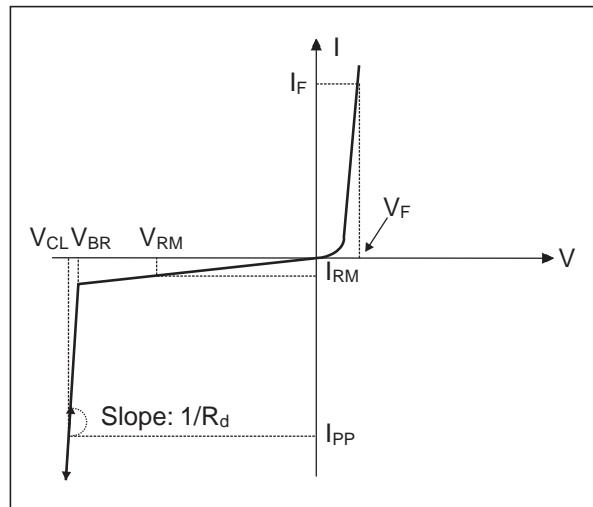
**Note 1:** for a surge greater than the maximum values, the diode will fail in short-circuit.

## THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R <sub>th(j-a)</sub>	Junction to ambient on printed circuit on recommended pad layout	220	°C/W

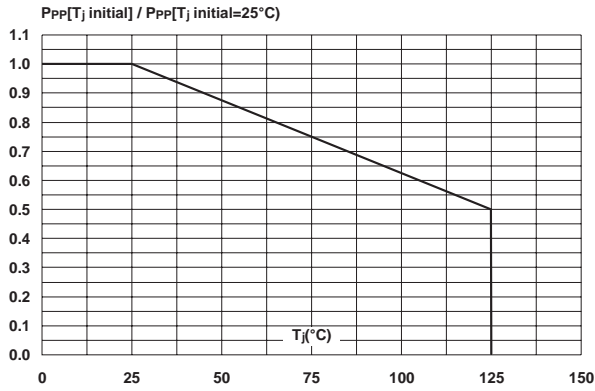
## ELECTRICAL CHARACTERISTICS (T<sub>amb</sub> = 25°C)

Symbol	Parameter
V <sub>RM</sub>	Stand-off voltage
V <sub>BR</sub>	Breakdown voltage
V <sub>CL</sub>	Clamping voltage
I <sub>RM</sub>	Leakage current
I <sub>PP</sub>	Peak pulse current
αT	Voltage temperature coefficient
V <sub>F</sub>	Forward voltage drop
C	Capacitance per line
R <sub>d</sub>	Dynamic resistance

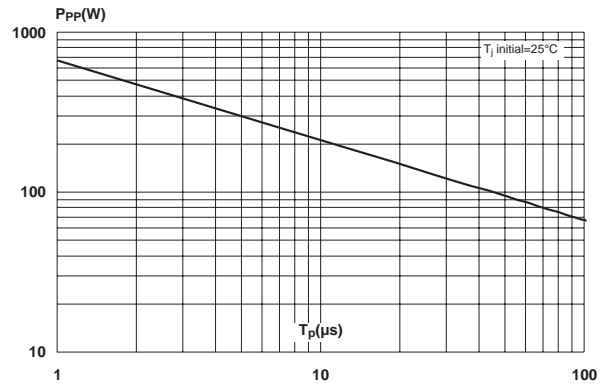


Types	V <sub>BR</sub> @		I <sub>r</sub>	I <sub>RM</sub> @		R <sub>d</sub>	αT	C
	min.	max.		max.	V <sub>RM</sub>			
	V	V	mA	μA	V	Ω	10 <sup>-4</sup> /°C	typ. @ 0V pF
ESDA6V1P6	6.1	7.2	1	0.5	3	1.5	4.5	70

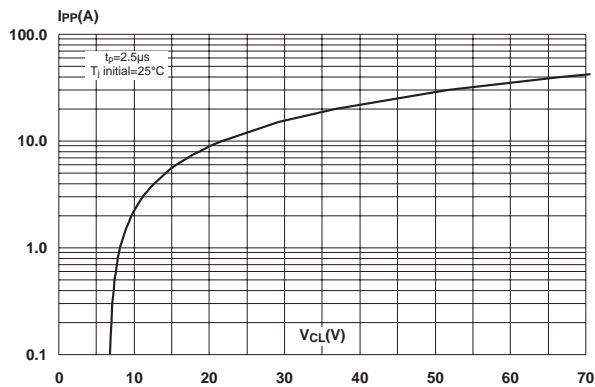
**Fig. 1:** Relative variation of peak pulse power versus initial junction temperature.



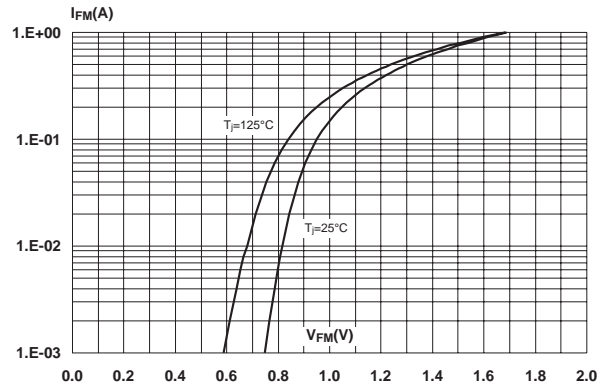
**Fig. 2:** Peak pulse power versus exponential pulse duration.



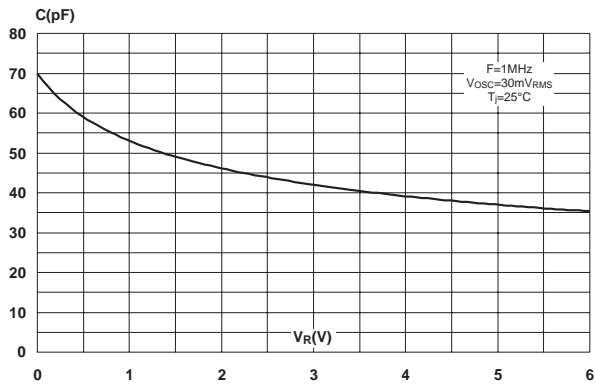
**Fig. 3:** Clamping voltage versus peak pulse current (typical values, rectangular waveform).



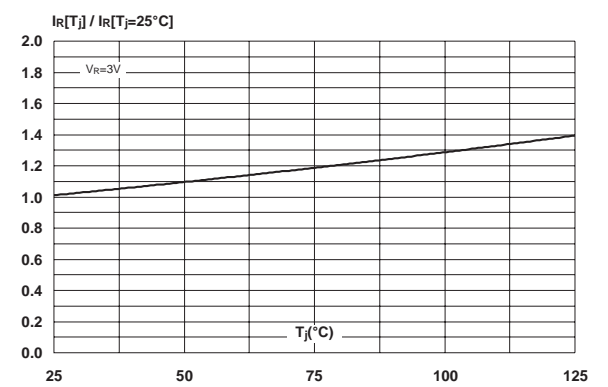
**Fig. 4:** Forward voltage drop versus peak forward current (typical values).



**Fig. 5:** Junction capacitance versus reverse voltage applied (typical values).



**Fig. 6:** Relative variation of leakage current versus junction temperature (typical values).



**TECHNICAL INFORMATION**

**1. ESD protection by ESDA6V1P6**

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

As a transient voltage suppressor, ESDA6V1P6 is an ideal choice for ESD protection by suppressing ESD events. It is capable of clamping the incoming transient to a low enough level such that any damage is prevented on the device protected by ESDA6V1P6.

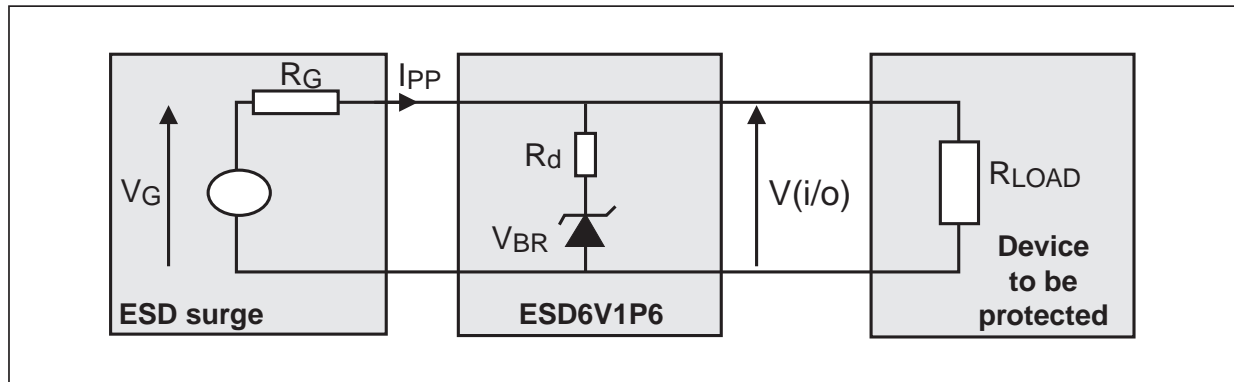
ESDA6V1P6 serves as a parallel protection elements, connected between the signal line and ground. As the transient rises above the operating voltage of the device, the ESDA6V1P6 becomes a low impedance path diverting the transient current to ground.

The clamping voltage is given by the following formula:

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

As shown in figure A2, the ESD strikes are clamped by the transient voltage suppressor.

**Fig. A2:** ESD clamping behavior.



To have a good approximation of the remaining voltages at both  $V_{i/o}$  side, we provide the typical dynamical resistance value  $R_d$ . By taking into account the following hypothesis:

$$R_G > R_d \text{ and } R_{load} > R_d$$

we have:

$$V(i/o) = V_{BR} + R_d \times \frac{V_g}{R_g}$$

The results of the calculation done  $V_G = 8kV$ ,  $R_G = 330\Omega$  (IEC61000-4-2 standard),  $V_{BR} = 6.4V$  (typ.) and  $R_d = 1.5\Omega$  (typ.) give:

$$V(i/o) = 42.8Volts$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the  $V_{i/o}$  side.

**Fig. A1:** Application example.

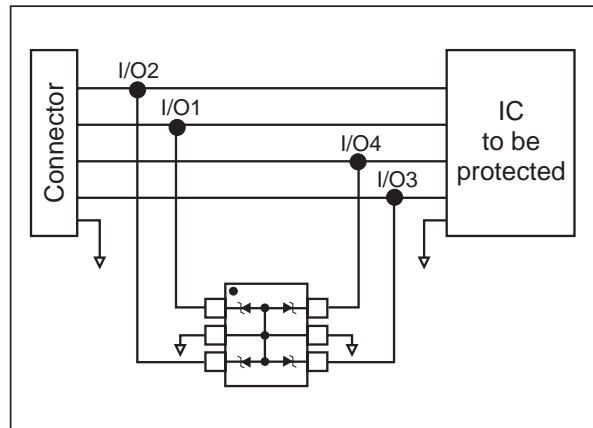


Fig. A3: ESD test board.

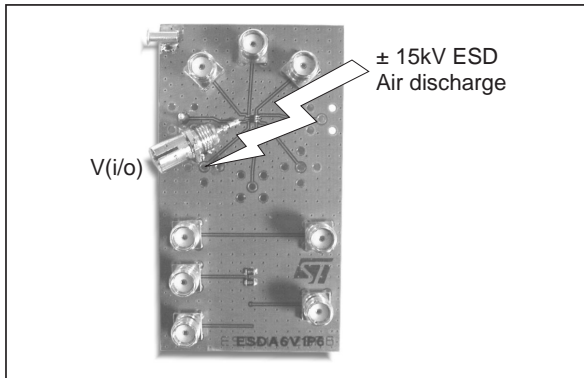


Fig. A4: ESD test configuration.

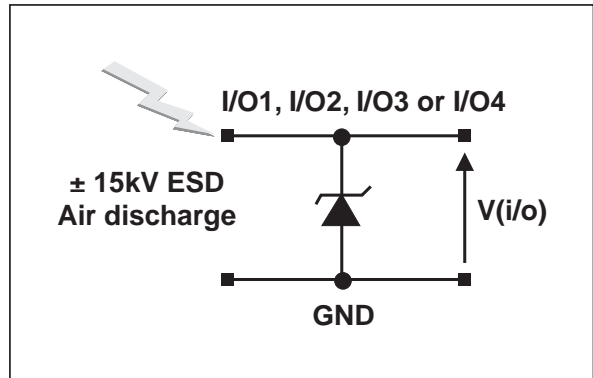
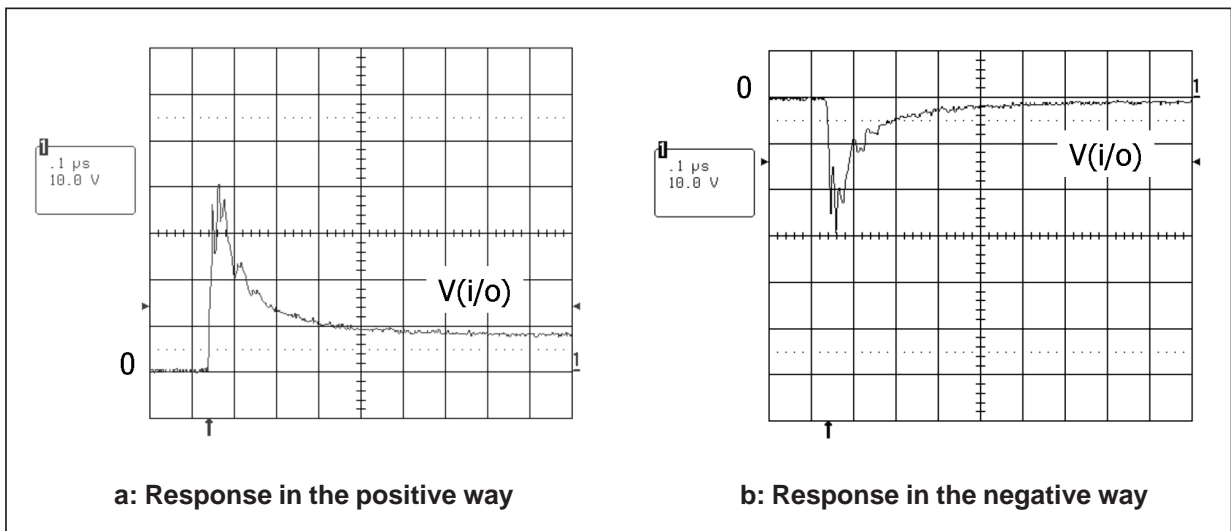
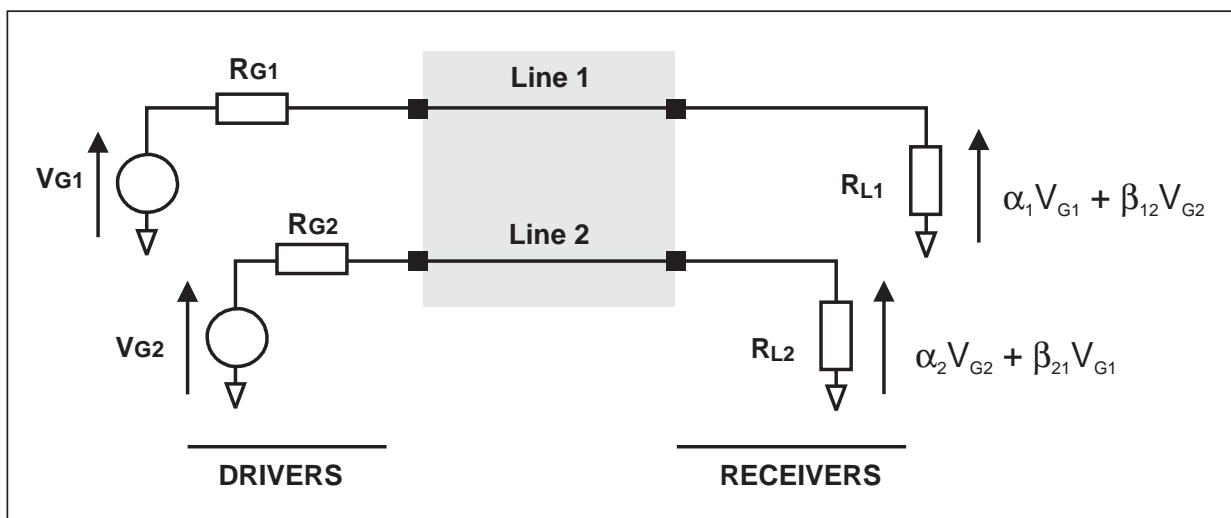


Fig. A5: Remaining voltage during ESD surge.



## 2. Crosstalk behavior

Fig. A6: Crosstalk phenomenon



The crosstalk phenomena are due to the coupling between 2 lines. Coupling factors ( $\beta_{12}$  or  $\beta_{21}$ ) increase when the gap across lines decreases, particularly in silicon dice. In the example above, the expected signal on load  $R_{L2}$  is  $\alpha_2 V_{G2}$ , in fact the real voltage at this point has got an extra value  $\beta_{21} V_{G2}$ . This part of the  $V_{G1}$  signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few  $k\Omega$ )

Fig. A7: Analog crosstalk test configuration.

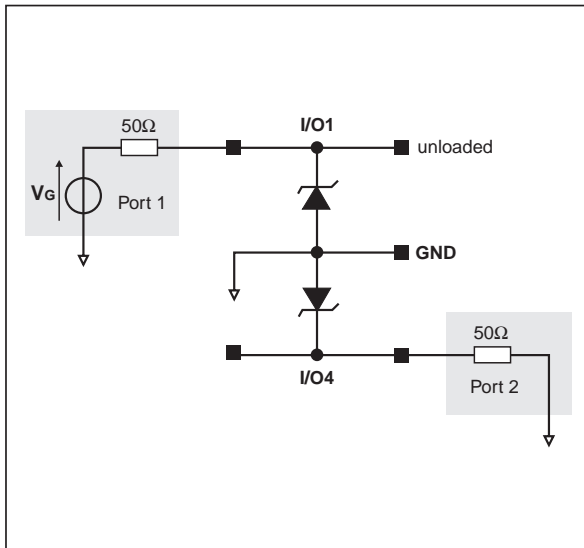


Fig. A8: Typical analog crosstalk response.

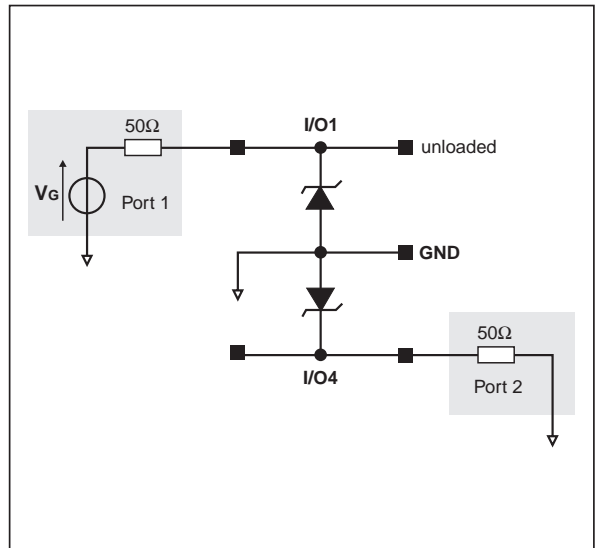


Fig. A9: Digital crosstalk test configuration.

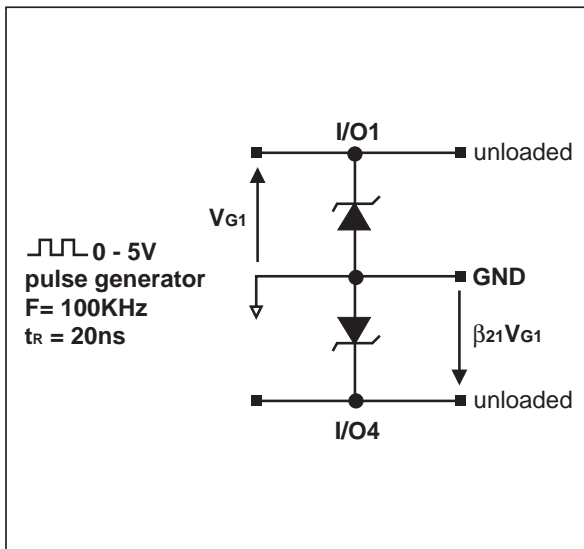
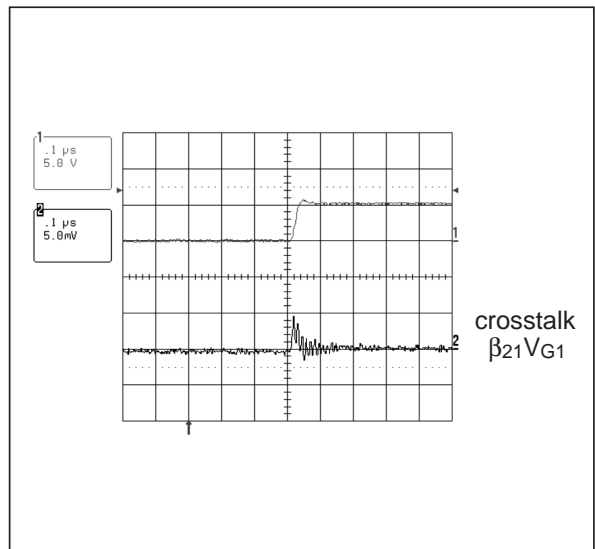


Fig. A10: Typical digital crosstalk response.



### 3. PCB layout recommendations

As ESD is a fast event, the  $di/dt$  caused by this surge is about 30A/ns (risetime=1ns,  $I_{peak}$ =30A), that means each nH causes an overvoltage of 30V.

Thus, the circuit board layout is a critical design step in the suppression of ESD induced transients by reducing parasitic inductances. To ensure that, the following guidelines are recommended :

- The ESDA6V1P6 should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.
- All conductive loops, including power and ground loops should be minimized.
- The ESD transient return path to ground should be kept as short as possible.
- The connections from the ground pins to the ground plane should be the shortest possible.

### 4. Comparison with varistors

	Varistors	TRANSIL™
Leakage current	--	+++
Protection efficiency	--	++
Ageing	--	++

#### Low leakage current for Transil™ device

- Improve the autonomy of portable equipments as mobile

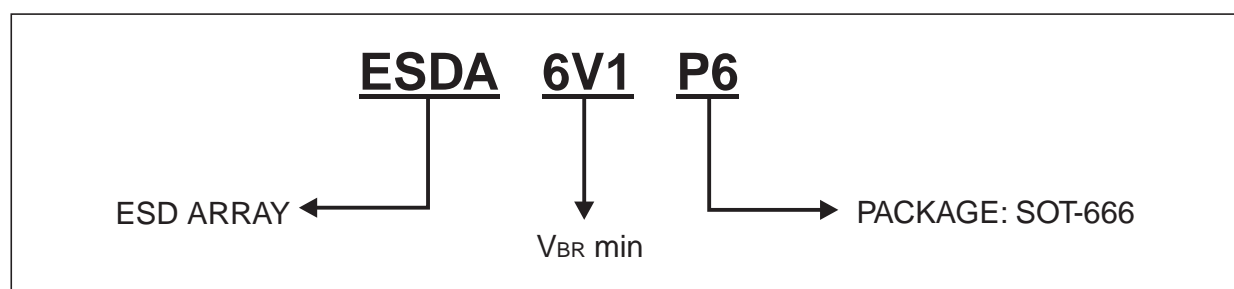
#### Better efficiency in terms of ESD protection by using Transil™ device

- Varistors are bidirectional devices and so are not suitable to protect sensitive ICs, because they will be submitted to high voltages in the negative way.
- Ratio  $V_{CL}/V_{BR}$  lower for Transil™ device
- Less dispersion in terms of  $V_{BR}$

#### No ageing phenomena regarding ESD events with Transil™ device

- Higher efficiency in terms of ESD protection

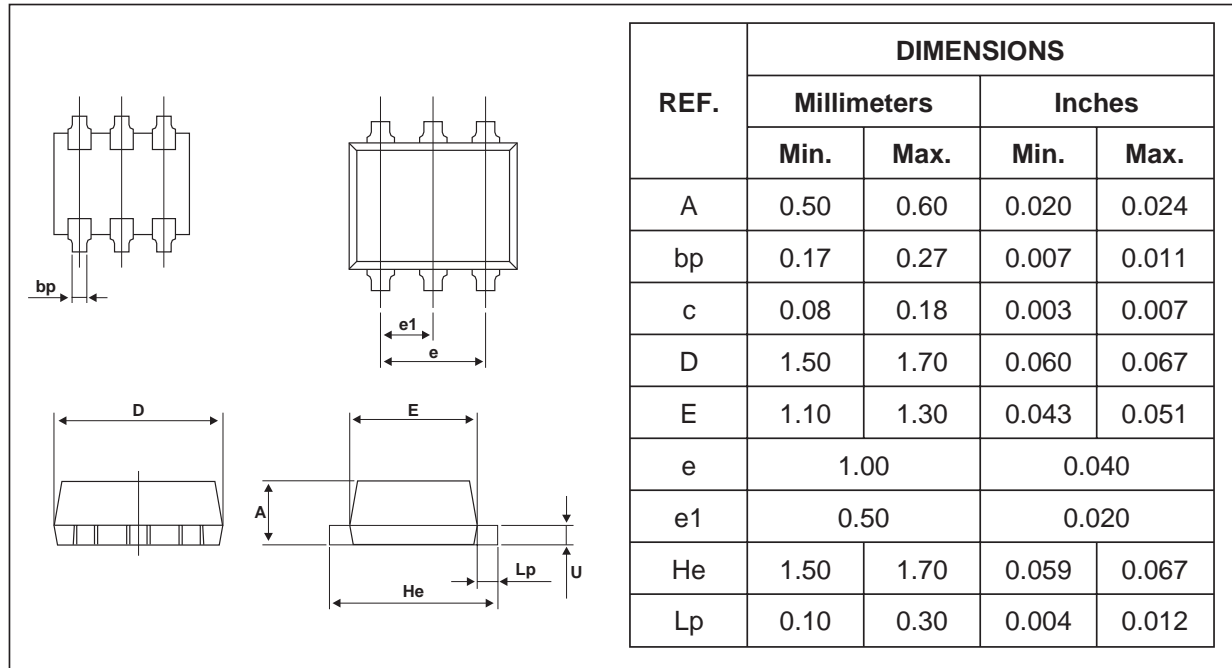
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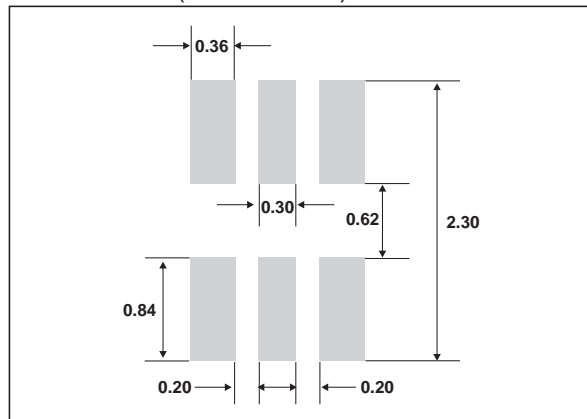
Ordering type	Marking	Package	Weight	Base qty	Delivery mode
ESDA6V1P6	B	SOT-666	2.9 mg.	3000	Tape & reel

# ESDA6V1P6

## PACKAGE MECHANICAL DATA SOT-666



### FOOT PRINT (in millimeters)



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