

**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTORS**

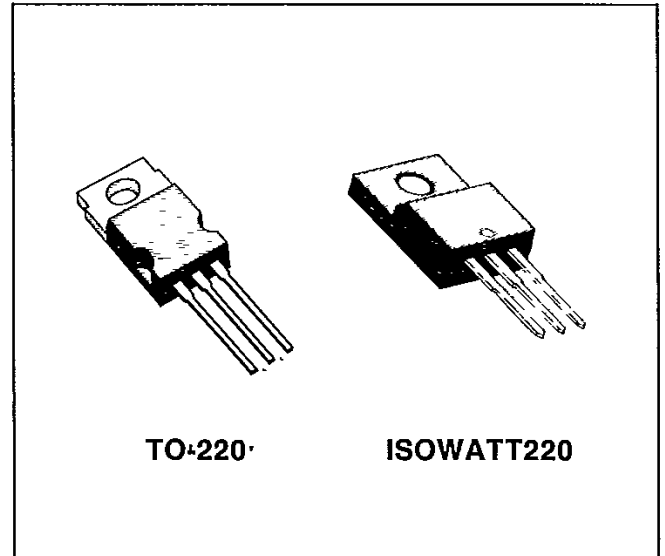
TYPE	V _{DSS}	R _{DS(on)}	I _D ■
IRF720	400 V	1.8 Ω	3.3 A
IRF720FI	400 V	1.8 Ω	2.5 A
IRF721	350 V	1.8 Ω	3.3 A
IRF721FI	350 V	1.8 Ω	2.5 A
IRF722	400 V	2.5 Ω	2.8 A
IRF722FI	400 V	2.5 Ω	2.0 A
IRF723	350 V	2.5 Ω	2.8 A
IRF723FI	350 V	2.5 Ω	2.0 A

- HIGH VOLTAGE - FOR OFF LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

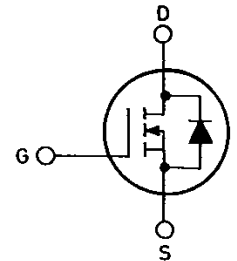
INDUSTRIAL APPLICATIONS:

- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include off-line use, constant current source, ultrasonic equipment and switching powers supplies start-up circuits.



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		IRF				
		720 720FI	721 721FI	722 722FI	723 723FI	
V _{DS} *	Drain-source voltage (V _{GS} =0)	400	350	400	350	V
V _{DGR} *	Drain-gate voltage (R _{GS} =20 KΩ)	400	350	400	350	V
V _{GS}	Gate-source voltage	±20				V
I _{DM} (●)	Drain current (pulsed)	13	13	11	11	A
I _{DLM}	Drain inductive current, clamped (L = 100 μH)	13	13	11	11	A
I _D	Drain current (cont.) at T _c = 25°C	3.3	3.3	2.8	2.8	A
I _D	Drain current (cont.) at T _c = 100°C	2.1	2.1	1.8	1.8	A
I _D ■	Drain current (cont.) at T _c = 25°C	2.5	2.5	2	2	A
I _D ■	Drain current (cont.) at T _c = 100°C	1.5	1.5	1.2	1.2	A
P _{tot} ■	Total dissipation at T _c < 25°C	TO-220		ISOWATT220		W
Derating factor		50		30		
T _{stg}	Storage temperature	0.40		0.24		W/°C
T _j	Max. operating junction temperature	-55 to 150				°C
		150				°C

* T_j = 25°C to 125°C

(●) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

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THERMAL DATA *

TO-220 | ISOWATT220

$R_{thj-case}$	Thermal resistance junction-case	max	2.50	4.16	°C/W
R_{thc-s}	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ for IRF720/722/720FI/722FI for IRF721/723/721FI/723FI	$V_{GS} = 0$	400 350		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^\circ\text{C}$		250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 500	nA

ON **

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$I_{D(on)}$	On-state drain current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ for IRF720/721/720FI/721FI for IRF722/723/722FI/723FI	$V_{GS} = 10 \text{ V}$	3.3 2.8			A A
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ for IRF720/721/720FI/721FI for IRF722/723/722FI/723FI	$I_D = 1.8 \text{ A}$			1.8 2.5	Ω Ω

DYNAMIC

$g_{fs} **$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 1.8 \text{ A}$		1.0			mho
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$	$f = 1 \text{ MHz}$			600	pF
C_{oss}	Output capacitance	$V_{GS} = 0$				200	pF
C_{rss}	Reverse transfer capacitance					40	pF

SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 175 \text{ V}$	$I_D = 1.5 \text{ A}$			40	ns
t_r	Rise time	$R_l = 50 \Omega$				50	ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)				100	ns
t_f	Fall time					50	ns
Q_g	Total Gate Charge	$V_{GS} = 10 \text{ V}$ $V_{DS} = \text{Max Rating} \times 0.8$ (see test circuit)	$I_D = 3.3 \text{ A}$			15	nC

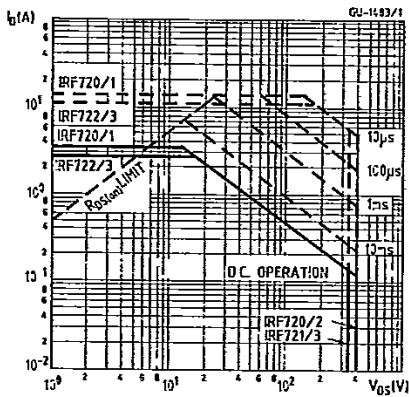
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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SOURCE DRAIN DIODE

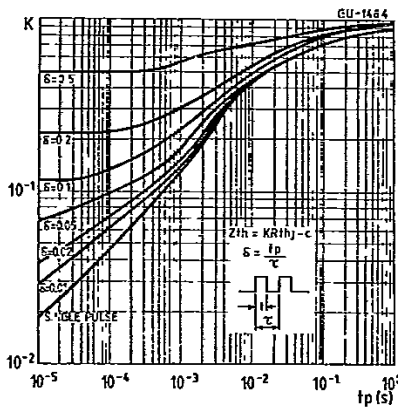
I_{SD}	Source-drain current			3.3	A
$I_{SDM} (*)$	Source-drain current (pulsed)			13	A
V_{SD}	Forward on voltage	$I_{SD} = 3.3 A$	$V_{GS} = 0$	1.6	V
t_{rr}	Reverse recovery time			450	ns
Q_{rr}	Reverse recovered charge	$I_{SD} = 3.3 A$	$di/dt = 100 A/\mu s$	3.1	μC

- ** Pulsed: Pulse duration $\leq 300 \mu s$, duty cycle $\leq 1.5\%$
- (*) Repetitive Rating: Pulse width limited by max junction temperature
- See note on ISOWATT220 in this datasheet

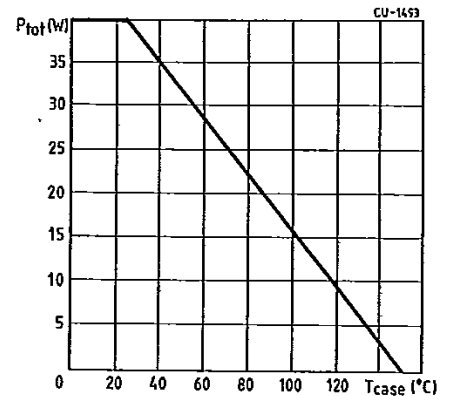
Safe operating areas (standard package)



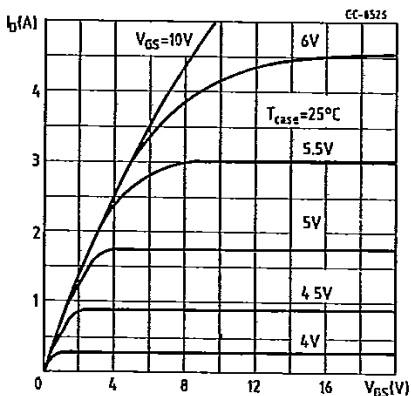
Thermal impedance (standard package)



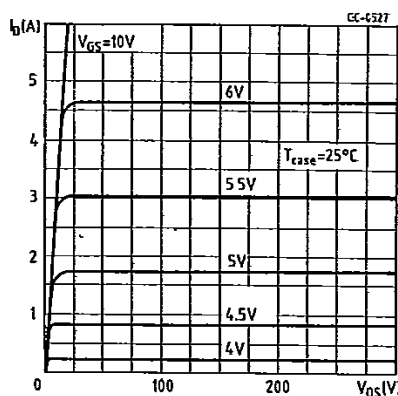
Derating curve (standard package)



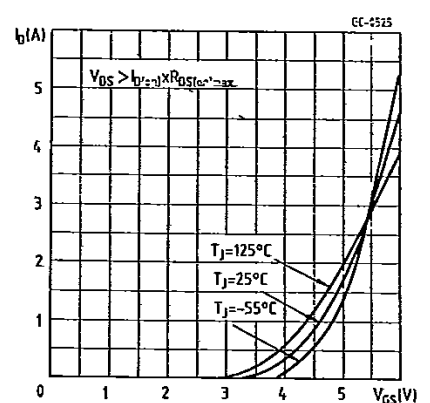
Output characteristics



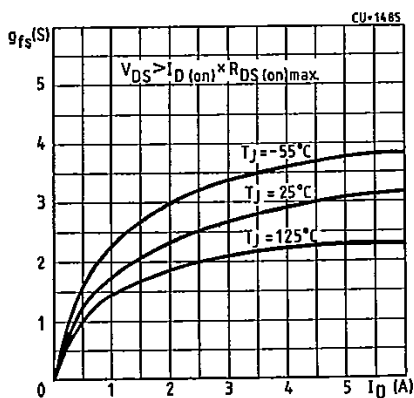
Output characteristics



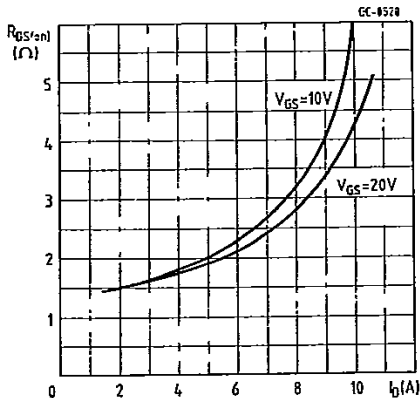
Transfer characteristics



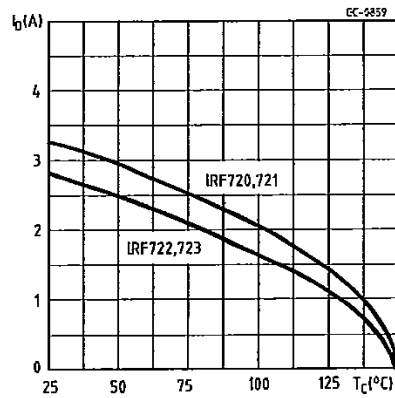
Transconductance



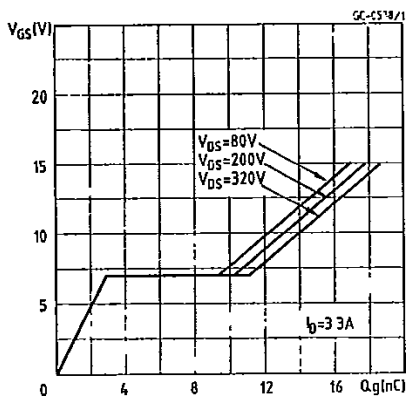
Static drain-source on resistance



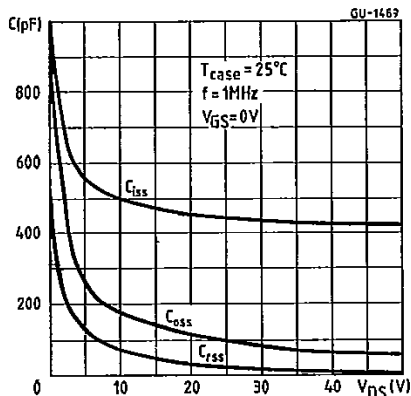
Maximum drain current vs temperature



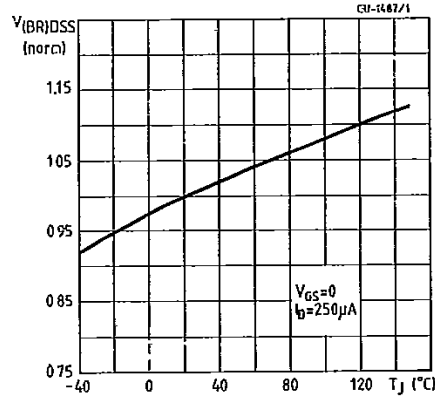
Gate charge vs gate-source voltage



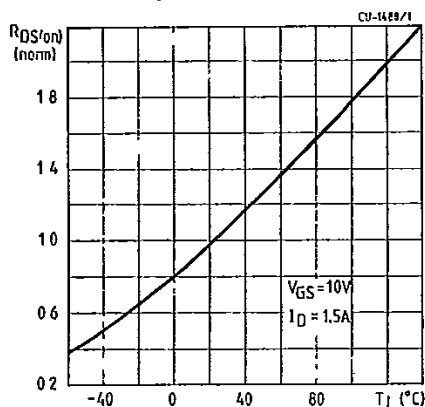
Capacitance variation



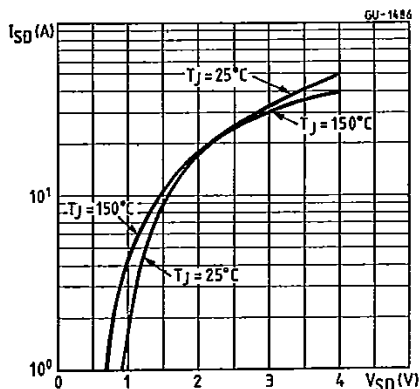
Normalized breakdown voltage vs temperature



Normalized on resistance vs temperature



Source-drain diode forward characteristics

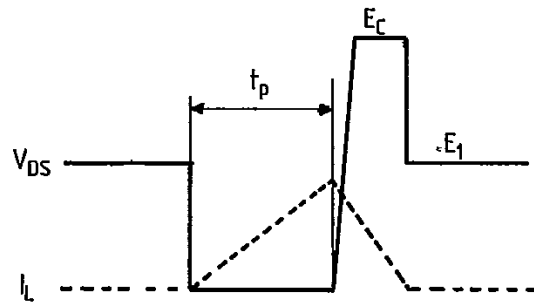
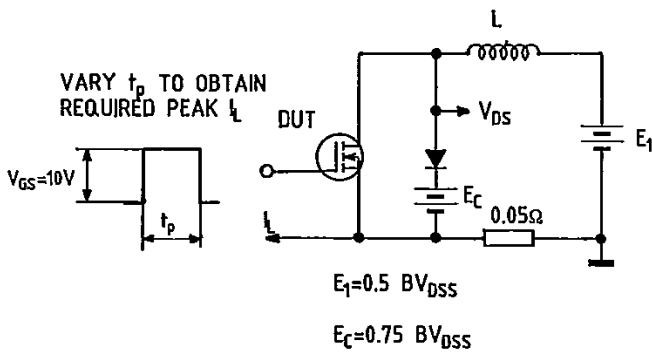


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Clamped inductive test circuit

Clamped inductive waveforms

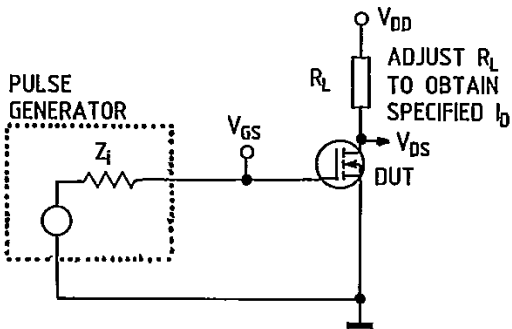


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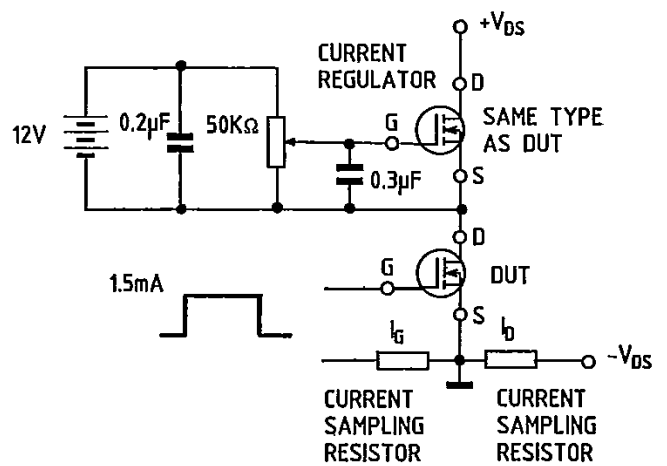
SC-0243

Switching times test circuit

Gate charge test circuit



SC-0246



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.

ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_J - T_C}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at } 150^\circ\text{C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.

The total thermal resistance $R_{th (tot)}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

- 1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

- 2 - for an intermediate power pulse of 5ms to 50ms:

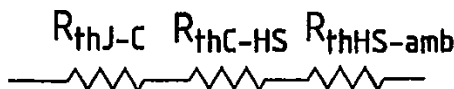
$$Z_{th} = R_{thJ-C}$$

- 3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

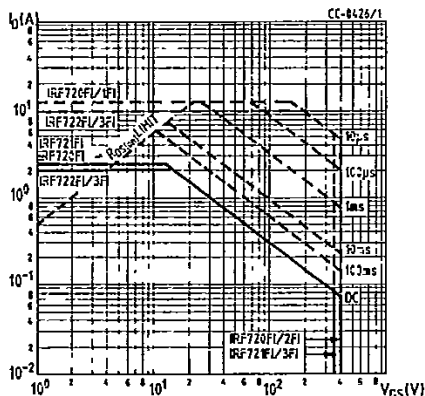
It is often possible to discern these areas on transient thermal impedance curves.

Fig. 1

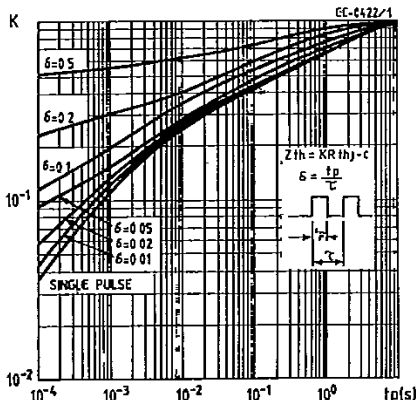


ISOWATT DATA

Safe operating areas



Thermal impedance



Derating curve

